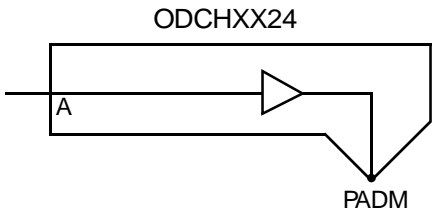


## AMI5HG 0.5 micron CMOS Gate Array

### Description

ODCHXX24 is a high performance, 24 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol	Truth Table	Pin Loading										
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> </tr> </tbody> </table>	A	PADM	L	L	H	H	<table border="1"> <thead> <tr> <th>A</th> <th>Load</th> </tr> </thead> <tbody> <tr> <td></td> <td>14.5 eqI</td> </tr> </tbody> </table>	A	Load		14.5 eqI
A	PADM											
L	L											
H	H											
A	Load											
	14.5 eqI											

### HDL Syntax

Verilog ..... ODCHXX24 *inst\_name* (PADM, A);  
 VHDL..... *inst\_name*: ODCHXX24 port map (PADM, A);

### Power Characteristics

Parameter	Value	Units
Static $I_{DD}$ ( $T_J = 85^\circ\text{C}$ )	TBD	nA
$EQL_{pd}$	249.7	Eq-load

See page 2-15 for power equation.

### Output Propagation Delays

Conditions:  $T_J = 25^\circ\text{C}$ ,  $V_{DD} = 5.0\text{V}$ , Typical Process

Delay (ns)		Parameter	Capacitive Load (pF)				
From	To		15	50	100	200	300 (max)
A	PADM	$t_{PLH}$	0.67	1.13	1.78	3.10	4.42
		$t_{PHL}$	0.70	1.05	1.49	2.35	3.22

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Pad Logic