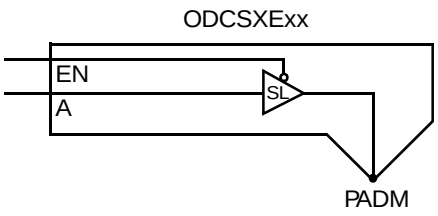
Description

ODCSXExx is a family of 4 to 16 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCSXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load			
	ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
A (eq-load)	2.3	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9	6.9
PADM (pF)	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXE04	4	TBD	218.9
ODCSXE08	8	TBD	240.3
ODCSXE12	12	TBD	261.1
ODCSXE16	16	TBD	283.9

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODCSXE04	From: A To: PADM	t_{PLH} t_{PHL}	3.23 3.03	6.83 6.71	12.02 12.06	22.08 22.73	31.52 33.29
	From: EN To: PADM	t_{ZH} t_{ZL}	2.93 2.88	6.57 6.64	11.74 11.91	21.76 22.47	31.25 33.18
ODCSXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.33 2.17	4.22 4.05	6.89 6.75	12.17 12.18	17.43 17.62
	From: EN To: PADM	t_{ZH} t_{ZL}	2.24 1.92	4.17 3.84	6.85 6.54	12.13 11.96	17.34 17.41
ODCSXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.12 1.87	3.37 3.14	5.20 4.97	8.84 8.54	12.37 12.03
	From: EN To: PADM	t_{ZH} t_{ZL}	1.82 1.68	3.11 2.96	4.89 4.74	8.45 8.28	12.08 11.85
ODCSXE16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.67 2.03	2.25 2.88	3.03 4.09	4.47 6.67	5.84 9.37
	From: EN To: PADM	t_{ZH} t_{ZL}	1.38 1.74	1.94 2.60	2.70 3.86	4.14 6.46	5.54 9.13

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODCSXE04	ODCSXE08	ODCSXE12	ODCSXE16
EN	PADM	t_{HZ} t_{LZ}	0.82 0.86	1.04 1.04	1.27 1.20	1.53 1.38