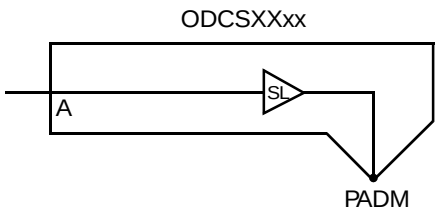
Description

ODCSXXxx is a family of 4 to 24 mA, non-inverting, CMOS-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODCSXX04	ODCSXX08	ODCSXX12	ODCSXX16	ODCSXX24
A (eq-load)	9.3	9.3	9.3	9.3	11.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCSXX04	4	TBD	198.6
ODCSXX08	8	TBD	220.0
ODCSXX12	12	TBD	240.8
ODCSXX16	16	TBD	263.6
ODCSXX24	24	TBD	282.3

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	2.46	6.09	11.15	20.96	30.46
	To: PADM	t_{PHL}	2.44	6.13	11.43	22.05	32.67
ODCSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.50	3.36	6.05	11.29	16.36
	To: PADM	t_{PHL}	1.64	3.50	6.19	11.60	17.04
ODCSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.35	2.58	4.36	7.94	11.51
	To: PADM	t_{PHL}	1.47	2.58	4.31	7.87	11.40
ODCSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.29	2.19	3.51	6.18	8.80
	To: PADM	t_{PHL}	1.44	2.30	3.56	6.13	8.75
ODCSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.31	2.20	3.50	6.12	8.76
	To: PADM	t_{PHL}	1.12	1.71	2.55	4.26	6.01

Delay will vary with input conditions. See page 2-17 for interconnect estimates.