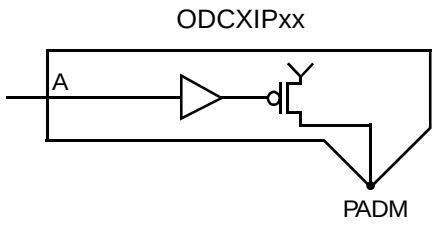
Description

ODCXIPxx is a family of 1 to 8 mA, inverting, CMOS-level, output buffer pieces with P-channel, open-drains (pull-up).

Logic Symbol



Truth Table

A	PADM
L	H
H	Z

Z = High Impedance

HDL Syntax

Verilog ..... ODCXIPxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXIPxx port map (PADM, A);

Pin Loading

Pin Name	Load			
	ODCXIP01	ODCXIP02	ODCXIP04	ODCXIP08
A (eq-load)	2.8	2.8	2.8	3.9
PADM (pF)	4.92	4.92	4.92	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static IDD (TJ = 85°C) (nA)	EQLpd (Eq-load)
ODCXIP01	1	TBD	148.8
ODCXIP02	2	TBD	153.6
ODCXIP04	4	TBD	162.0
ODCXIP08	8	TBD	178.9

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXIP01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{ZH}	4.73	6.87	8.98	12.13	17.31
ODCXIP02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{ZH}	2.54	6.19	8.78	11.38	16.61
ODCXIP04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.75	3.62	6.26	11.57	16.92
ODCXIP08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZH}	1.33	2.26	3.59	6.24	8.91

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell			
			ODCXIP01	**ODCXIP02**	**ODCXIP04**	**ODCXIP08**
APADM		t_{HZ}	1.04	0.89	1.05	1.38