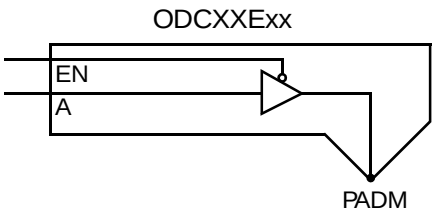
Description

ODCXXExx is a family of 1 to 24 mA, non-inverting, CMOS-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog ..... ODCXXExx *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODCXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16	ODCXXE24
A (eq-load)	5.6	7.9	7.9	2.3	2.3	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5	5.5	5.5
PADM (pF)	4.92	4.92	4.93	4.93	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXE01	1	TBD	154.9
ODCXXE02	2	TBD	164.2
ODCXXE04	4	TBD	174.8
ODCXXE08	8	TBD	223.0
ODCXXE12	12	TBD	243.9
ODCXXE16	16	TBD	268.0
ODCXXE24	24	TBD	279.9

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXXE01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	4.70 4.92	6.77 7.09	8.86 9.26	12.04 12.53	17.40 18.02
	From: EN To: PADM	t_{ZH} t_{ZL}	4.94 4.98	7.05 7.06	9.16 9.18	12.32 12.44	17.58 18.06
ODCXXE02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.53 2.55	6.22 6.27	8.83 8.94	11.42 11.60	16.58 16.89
	From: EN To: PADM	t_{ZH} t_{ZL}	2.75 2.62	6.39 6.32	8.97 8.96	11.57 11.61	16.83 16.96
ODCXXE04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.65 1.82	3.57 3.58	6.27 6.20	11.58 11.51	16.83 16.77
	From: EN To: PADM	t_{ZH} t_{ZL}	1.85 1.72	3.67 3.62	6.29 6.25	11.61 11.49	16.98 16.82
ODCXXE08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.86 1.57	2.79 2.48	4.08 3.78	6.73 6.39	9.43 8.99
	From: EN To: PADM	t_{ZH} t_{ZL}	1.51 1.40	2.48 2.31	3.83 3.58	6.49 6.17	9.14 8.83
ODCXXE12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.22 1.61	1.93 2.21	2.87 3.03	4.69 4.74	6.46 6.53
	From: EN To: PADM	t_{ZH} t_{ZL}	1.48 1.26	2.20 1.93	3.12 2.83	4.91 4.59	6.72 6.31
ODCXXE16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	2.12 1.59	2.36 2.07	3.04 2.75	4.47 4.07	5.74 5.34
	From: EN To: PADM	t_{ZH} t_{ZL}	1.53 1.33	2.13 1.86	2.86 2.56	4.23 3.89	5.55 5.18
ODCXXE24	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{PLH} t_{PHL}	1.87 1.53	2.37 1.91	3.07 2.43	4.45 3.39	5.80 4.22
	From: EN To: PADM	t_{ZH} t_{ZL}	1.42 1.26	2.04 1.71	2.78 2.26	4.14 3.22	5.48 4.09

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell					
			ODCXXE01	ODCXXE02	ODCXXE04	ODCXXE08	ODCXXE12	ODCXXE16
EN	PADM	t_{HZ}	1.45	1.20	1.59	1.24	1.62	2.01
		t_{LZ}	0.41	0.38	0.55	1.09	1.30	1.60