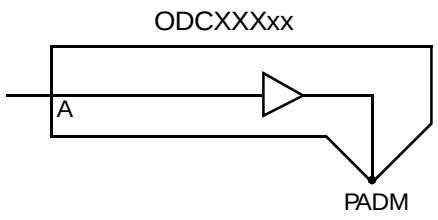
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODCXXXxx is a family of 1 to 24 mA, non-inverting, CMOS-level output buffer pieces.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog ..... ODCXXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODCXXXxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODCXXX01	ODCXXX02	ODCXXX04	ODCXXX08	ODCXXX12	ODCXXX16	ODCXXX24
A (eq-load)	4.3	4.3	6.2	8.3	8.2	8.2	10.3

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODCXXX01	1	TBD	149.5
ODCXXX02	2	TBD	155.0
ODCXXX04	4	TBD	165.6
ODCXXX08	8	TBD	189.8
ODCXXX12	12	TBD	210.7
ODCXXX16	16	TBD	234.8
ODCXXX24	24	TBD	248.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODCXXX01	**Capacitive Load (pF)**		**15**	**25**	**35**	**50**	**75 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	4.55 4.71	6.53 6.90	8.68 9.09	11.93 12.37	17.07 17.81
ODCXXX02	**Capacitive Load (pF)**		**15**	**50**	**75**	**100**	**150 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	2.46 2.77	6.13 6.39	8.76 9.02	11.37 11.68	16.53 17.05
ODCXXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.45 1.52	3.31 3.43	5.97 6.09	11.30 11.35	16.62 16.64
ODCXXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.17 1.22	2.11 2.12	3.45 3.41	6.11 6.00	8.76 8.61
ODCXXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To PADM	t_{PLH} t_{PHL}	1.15 1.20	1.85 1.86	2.80 2.74	4.61 4.47	6.36 6.19
ODCXXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.29 1.33	1.83 1.85	2.54 2.56	3.91 3.90	5.24 5.15
ODCXXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{PLH} t_{PHL}	1.27 1.09	1.80 1.51	2.51 2.02	3.87 2.94	5.17 3.81

Delay will vary with input conditions. See page 2-17 for interconnect estimates.