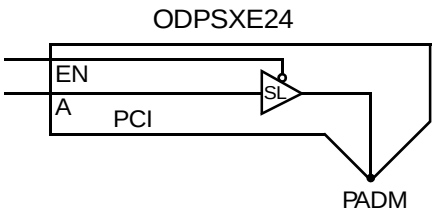
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODPSXE24 is a 33 MHz PCI, non-inverting, tristate buffer piece with active low enable and controlled slew rate output.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	8.2 pF
EN	5.5 pF
PADM	4.93 pF

HDL Syntax

Verilog ..... ODPSXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODPSXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	229.2	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	1.50 2.08	1.92 2.70	2.41 3.62	3.33 5.52	4.28 7.49
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	3.47 2.49 1.41 1.46	 1.83 2.37	 2.37 3.45	 3.42 5.46	 4.43 7.46

Delay will vary with input conditions. See page 2-17 for interconnect estimates.