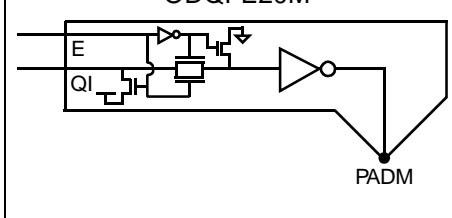
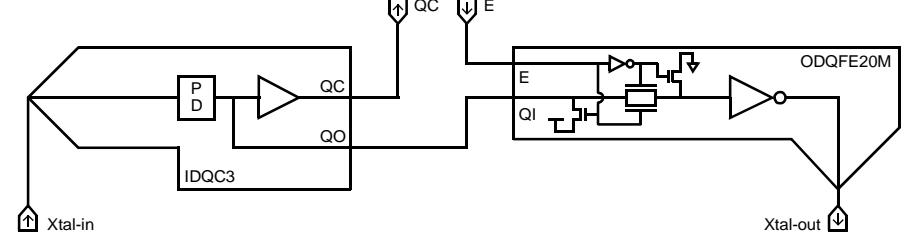


AMI5HG 0.5 micron CMOS Gate Array

Description

ODQFE20M is a fundamental mode, enabled crystal oscillator, output buffer pad piece that runs over a frequency range of 1 MHz - 20 MHz. QI is the input from IDQC3. E is the oscillator high input enable. PADM is the bond pad to the Xtal-out.

Logic Symbol	Logic Schematic																		
																			
Truth Table <table border="1"> <thead> <tr> <th>PADM</th><th>E</th><th>QI</th></tr> </thead> <tbody> <tr> <td>H</td><td>L</td><td>X</td></tr> <tr> <td>H</td><td>H</td><td>L</td></tr> <tr> <td>L</td><td>H</td><td>H</td></tr> </tbody> </table>	PADM	E	QI	H	L	X	H	H	L	L	H	H	Pin Loading <table border="1"> <thead> <tr> <th></th><th>Load</th></tr> </thead> <tbody> <tr> <td>E</td><td>6.5 eql</td></tr> <tr> <td>QI</td><td>5.5 eql</td></tr> </tbody> </table>		Load	E	6.5 eql	QI	5.5 eql
PADM	E	QI																	
H	L	X																	
H	H	L																	
L	H	H																	
	Load																		
E	6.5 eql																		
QI	5.5 eql																		

HDL Syntax

Verilog ODQFE20M *inst_name* (PADM, E, QI);
VHDL..... *inst_name*: ODQFE20M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ C$)	TBD	nA
EQL_{pd}	165.4	Eq-load

See page 2-15 for power equation.

ODQFE20M



AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

From	To	Parameter	Capacitive Load (pF)				
			15	50	75	100	150 (max)
E	PADM	t_{PLH}	3.40	7.03	9.59	12.18	17.46
		t_{PHL}	2.46	6.17	8.85	11.53	16.78
QI	PADM	t_{PLH}	2.40	6.00	8.60	11.21	16.40
		t_{PHL}	2.51	6.18	8.81	11.46	16.80

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Design Notes:

The ODQFE20M is the output cell of a two cell oscillator circuit. The QI pin is to be connected to the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.