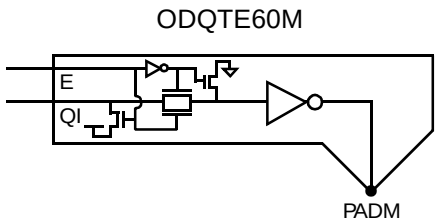
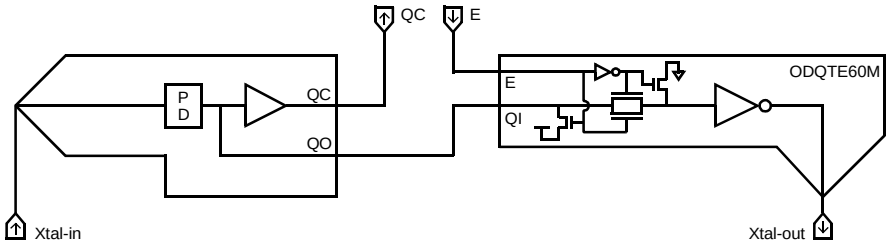
Description

ODQTE60M is an enabled crystal oscillator, output driver pad piece that runs over a frequency range of 20 - 60 MHz. QI is the input from the IDQC3. E is the oscillator high input enable. PADM is the bond pad to Xtal-out.

Logic Symbol



Logic Schematic



Truth Table

PADM	E	QI
H	L	X
H	H	L
L	H	H

Pin Loading

	Load
E	6.5 eql
QI	5.5 eql

Pad Logic

HDL Syntax

Verilog ..... ODQTE60M *inst_name* (PADM, E, QI);

VHDL..... *inst_name*: ODQTE60M port map (PADM, E, QI);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	176.1	Eq-load

See page 2-15 for power equation.

AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF)				
			15	50	100	200	300 (max)
E	PADM	t_{PLH} t_{PHL}	2.78 1.53	4.63 3.37	7.29 6.01	12.61 11.28	17.93 16.57
QI	PADM	t_{PLH} t_{PHL}	1.53 1.54	3.38 3.43	6.03 6.06	11.33 11.30	16.64 16.60

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Design Notes:

The ODQTE60M is the output cell of a two cell oscillator circuit. The QI pin is to be connected the QO pin of the IDQC3 oscillator input receiver piece. Two package pins are required to create a complete oscillator.