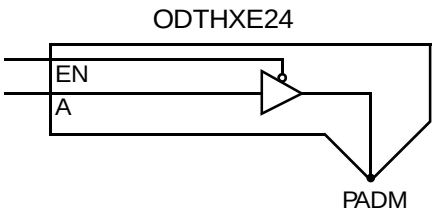
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODTHXE24 is a high performance, 24 mA, non-inverting, TTL-level, tristate output buffer piece with active low enable.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Pin Loading

	Load
A	3.5 eql
EN	6.5 eql
PADM	4.93 pF

HDL Syntax

Verilog **.....** ODTHXE24 *inst_name* (PADM, A, EN);

VHDL..... *inst_name*: ODTHXE24 port map (PADM, A, EN);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	297.0	Eq-load

See page 2-15 for power equation.

Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH} t_{PHL}	0.89 1.19	1.17 1.64	1.55 2.30	2.26 3.60	2.94 4.91
EN	PADM	t_{HZ} t_{LZ} t_{ZH} t_{ZL}	1.06 1.02 0.70 1.10	 0.96 1.59	 1.32 2.27	 2.03 3.59	 2.74 4.88

Delay will vary with input conditions. See page 2-17 for interconnect estimates.