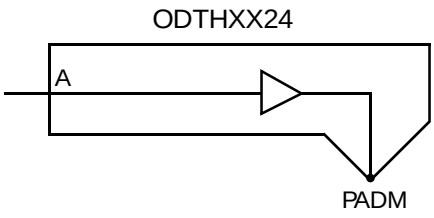
Description

ODTHXX24 is a high performance,24 mA, non-inverting, TTL-level output buffer piece.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

Pin Loading

	Load
A	14.5 eql

HDL Syntax

Verilog **.....** ODTHXX24 *inst_name* (PADM, A);

VHDL*.....* *inst_name*: ODTHXX24 port map (PADM, A);

Power Characteristics

Parameter	Value	Units
Static I_{DD} (T_J = 85°C)	TBD	nA
EQL_{pd}	249.7	Eq-load

See page 2-15 for power equation.

Output Propagation Delays

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Capacitive Load (pF) 15	50	100	200	300 (max)
A	PADM	t_{PLH}	0.54	0.81	1.16	1.84	2.57
		t_{PHL}	0.84	1.30	1.95	3.25	4.56

Delay will vary with input conditions. See page 2-17 for interconnect estimates.