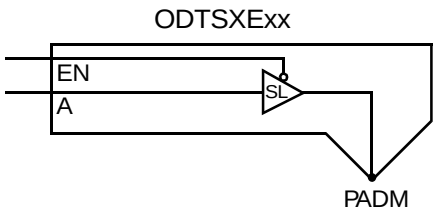
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODTSXExx is a family of 4 to 24 mA, non-inverting, TTL-level, tristate output buffer pieces with active low enables and controlled slew rate outputs.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

HDL Syntax

Verilog **.....** ODTSXExx *inst_name* (PADM, A, EN);

VHDL*.....* *inst_name*: ODTSXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load				
	ODTSXE04	ODTSXE08	ODTSXE12	ODTSXE16	ODTSXE24
A (eq-load)	2.3	2.3	2.3	2.3	2.3
EN (eq-load)	6.9	6.9	6.9	6.9	6.9
PADM (pF)	4.94	4.94	4.94	4.94	4.94

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXE04	4	TBD	218.9
ODTSXE08	8	TBD	240.3
ODTSXE12	12	TBD	261.1
ODTSXE16	16	TBD	283.9
ODTSXE24	24	TBD	302.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXE04	From: A To: PADM	t_{PLH} t_{PHL}	2.53 4.24	4.23 9.70	7.00 17.28	12.66 32.07	18.22 46.58
	From: EN To: PADM	t_{ZH} t_{ZL}	1.65 3.99	3.91 9.44	6.79 16.99	12.31 31.78	18.00 46.36
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.82 2.62	2.84 5.68	4.27 9.82	7.12 17.67	9.98 25.18
	From: EN To: PADM	t_{ZH} t_{ZL}	1.46 2.53	2.51 5.45	3.97 9.54	6.83 17.43	9.65 24.94
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.71 2.61	2.43 4.23	3.40 6.93	5.32 12.29	7.25 17.32
	From: EN To: PADM	t_{ZH} t_{ZL}	1.42 1.96	2.14 3.96	3.11 6.72	5.03 12.01	6.96 17.11
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.73 2.15	2.28 3.52	3.02 5.54	4.45 9.49	5.85 13.31
	From: EN To: PADM	t_{ZH} t_{ZL}	1.39 1.91	1.96 3.36	2.70 5.34	4.13 9.23	5.55 13.16
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTSXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.72 1.96	2.26 2.90	3.01 4.22	4.45 6.84	5.87 9.47
	From: EN To: PADM	t_{ZH} t_{ZL}	1.48 1.63	2.04 2.59	2.78 3.94	4.22 6.58	5.63 9.19

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell ODTSXE04	ODTSXE08	ODTSXE12	ODTSXE16	ODTSXE24
EN	PADM	t_{HZ} t_{LZ}	0.82 0.86	1.04 1.04	1.27 1.20	1.53 1.38	1.42 1.46