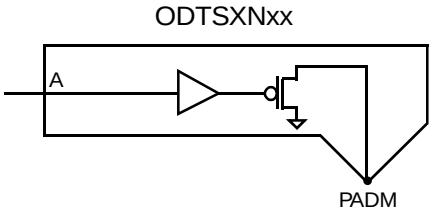
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODTSXNxx is a family of 4 to 24 mA, non-inverting, TTL-level, output buffer pieces with N-channel open-drains (pull-down) and controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	Z

Z = High Impedance

HDL Syntax

Verilog **.....** ODTSXNxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXNxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTSXN04	ODTSXN08	ODTSXN12	ODTSXN16	ODTSXN24
A (eq-load)	8.1	8.1	8.1	8.1	8.1
PADM (pF)	4.90	4.90	4.90	4.90	4.90

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXN04	4	TBD	164.3
ODTSXN08	8	TBD	172.6
ODTSXN12	12	TBD	180.2
ODTSXN16	16	TBD	188.3
ODTSXN24	24	TBD	200.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	50	100	200	300 (max)
ODTSXN04	From: A To: PADM	t_{ZL}	3.28	8.54	15.91	30.44	44.81

ODTSXN08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	2.02	4.79	8.62	16.16	23.65
ODTSXN12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.45	3.36	5.94	10.94	15.84
ODTSXN16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.16	2.62	4.58	8.31	11.90
ODTSXN24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A To: PADM	t_{ZL}	1.03	2.00	3.34	5.92	8.40

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns)		Parameter	Cell				
From	**To**		**ODTSXN04**	**ODTSXN08**	**ODTSXN12**	**ODTSXN16**	**ODTSXN24**
A	PADM	t_{LZ}	0.80	0.93	1.05	1.19	1.37