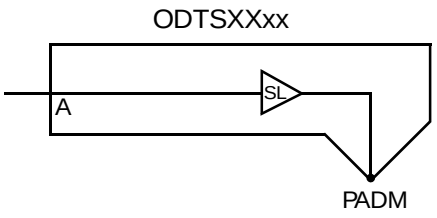
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODTSXXxx is a family of 4 to 24 mA, non-inverting, TTL-level, output buffer pieces with controlled slew rate outputs.

Logic Symbol



Truth Table

A	PADM
L	L
H	H

HDL Syntax

Verilog **.....** ODTSXXxx *inst_name* (PADM, A);

VHDL..... *inst_name*: ODTSXXxx port map (PADM, A);

Pin Loading

Pin Name	Load				
	ODTSXX04	ODTSXX08	ODTSXX12	ODTSXX16	ODTSXX24
A (eq-load)	9.3	9.3	9.3	9.3	11.4

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTSXX04	4	TBD	198.6
ODTSXX08	8	TBD	220.0
ODTSXX12	12	TBD	240.8
ODTSXX16	16	TBD	263.6
ODTSXX24	24	TBD	282.3

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ODTSXX04	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.51	3.44	6.21	11.80	17.44
	To: PADM	t_{PLH}	3.60	8.97	16.46	31.17	45.68
ODTSXX08	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.01	2.03	3.46	6.29	9.16
	To: PADM	t_{PLH}	2.19	5.12	9.13	16.85	24.39
ODTSXX12	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	0.97	1.63	2.58	4.49	6.41
	To: PADM	t_{PLH}	1.82	3.72	6.37	11.54	16.57
ODTSXX16	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.01	1.52	2.22	3.62	5.05
	To: PADM	t_{PLH}	1.60	2.98	4.96	8.83	12.60
ODTSXX24	**Capacitive Load (pF)**		**15**	**50**	**100**	**200**	**300 (max)**
	From: A	t_{PLH}	1.07	1.55	2.25	3.65	5.05
	To: PADM	t_{PLH}	1.31	2.20	3.52	6.14	8.73

Delay will vary with input conditions. See page 2-17 for interconnect estimates.