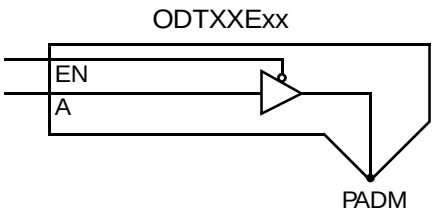
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

ODTXXExx is a family of 1 to 24 mA, non-inverting, TTL-level, tristate output buffer pieces with active low enables.

Logic Symbol



Truth Table

EN	A	PADM
L	L	L
L	H	H
H	X	Z

Z = High Impedance

HDL Syntax

Verilog **.....** ODTXXExx *inst_name* (PADM, A, EN);

VHDL*.....* *inst_name*: ODTXXExx port map (PADM, A, EN);

Pin Loading

Pin Name	Load						
	ODTXXE01	ODTXXE02	ODTXXE04	ODTXXE08	ODTXXE12	ODTXXE16	ODTXXE24
A (eq-load)	5.6	7.9	7.9	2.3	2.3	2.3	2.3
EN (eq-load)	4.0	5.3	5.3	5.5	5.5	5.5	5.5
PADM (pF)	4.92	4.92	4.93	4.93	4.93	4.93	4.93

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ODTXXE01	1	TBD	154.9
ODTXXE02	2	TBD	164.2
ODTXXE04	4	TBD	174.8
ODTXXE08	8	TBD	223.0
ODTXXE12	12	TBD	243.9
ODTXXE16	16	TBD	268.0
ODTXXE24	24	TBD	279.9

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Capacitive Load (pF)		15	25	35	50	75 (max)
ODTXXE01	From: A To: PADM	t_{PLH} t_{PHL}	2.85 7.15	3.95 10.42	5.07 13.74	6.76 18.76	9.64 27.24
	From: EN To: PADM	t_{ZH} t_{ZL}	2.85 7.28	4.03 10.47	5.21 13.71	6.93 18.69	9.67 27.25
	Capacitive Load (pF)		**15**	**50**	**75**	**100**	**150 (max)**
ODTXXE02	From: A To: PADM	t_{PLH} t_{PHL}	1.59 3.67	3.57 9.28	4.97 13.29	6.37 17.31	9.18 25.37
	From: EN To: PADM	t_{ZH} t_{ZL}	1.75 3.62	3.77 9.32	5.18 13.36	6.57 17.37	9.31 25.36
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE04	From: A To: PADM	t_{PLH} t_{PHL}	1.02 2.27	2.19 5.06	3.66 9.01	6.47 17.01	9.36 24.98
	From: EN To: PADM	t_{ZH} t_{ZL}	1.33 2.68	2.36 5.09	3.81 9.03	6.68 17.08	9.52 25.00
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE08	From: A To: PADM	t_{PLH} t_{PHL}	1.47 1.55	2.02 2.90	2.76 4.87	4.19 8.83	5.61 12.75
	From: EN To: PADM	t_{ZH} t_{ZL}	1.32 1.64	1.82 3.05	2.53 5.01	3.96 8.94	5.39 12.91
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE12	From: A To: PADM	t_{PLH} t_{PHL}	1.53 1.73	1.96 2.65	2.48 3.98	3.46 6.62	4.43 9.22
	From: EN To: PADM	t_{ZH} t_{ZL}	1.23 1.48	1.67 2.45	2.22 3.77	3.22 6.42	4.14 9.05
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE16	From: A To: PADM	t_{PLH} t_{PHL}	1.55 1.87	1.91 2.58	2.36 3.57	3.14 5.52	3.85 7.48
	From: EN To: PADM	t_{ZH} t_{ZL}	1.25 1.44	1.64 2.23	2.09 3.27	2.87 5.27	3.59 7.22
	Capacitive Load (pF)		**15**	**50**	**100**	**200**	**300 (max)**
ODTXXE24	From: A To: PADM	t_{PLH} t_{PHL}	1.70 1.70	2.00 2.26	2.39 2.99	3.15 4.34	3.89 5.61
	From: EN To: PADM	t_{ZH} t_{ZL}	1.31 0.69	1.68 2.03	2.13 2.78	2.91 4.11	3.60 5.47

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

Delay (ns) From	To	Parameter	Cell						
			ODTXXE01	ODTXXE02	ODTXXE04	ODTXXE08	ODTXXE12	ODTXXE16	ODTXXE24
EN	PADM	t_{HZ}	1.45	1.20	1.59	1.24	1.62	2.01	2.01
		t_{LZ}	0.41	0.38	0.55	1.09	1.30	1.60	1.96