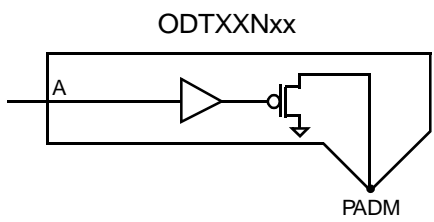


AMI5HG 0.5 micron CMOS Gate Array

Description

ODTXXNxx is a family of 1 to 24 mA, non-inverting, TTL-level, output buffer pieces with N-channel, open-drains (pull-down).

Logic Symbol	Truth Table						
	<table border="1"> <thead> <tr> <th>A</th> <th>PADM</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>Z</td> </tr> </tbody> </table> <p>Z = High Impedance</p>	A	PADM	L	L	H	Z
A	PADM						
L	L						
H	Z						

HDL Syntax

Verilog ODTXXNxx *inst_name* (PADM, A);

VHDL *inst_name*: ODTXXNxx port map (PADM, A);

Pin Loading

Pin Name	Load						
	ODTXXN01	ODTXXN02	ODTXXN04	ODTXXN08	ODTXXN12	ODTXXN16	ODTXXN24
A (eq-load)	4.3	4.3	4.3	8.3	8.3	8.3	8.3
PADM (pF)	4.90	4.90	4.91	4.90	4.91	4.91	4.91

Power Characteristics

Cell	Output Drive (mA)	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ODTXXN01	1	TBD	141.7
ODTXXN02	2	TBD	143.5
ODTXXN04	4	TBD	147.6
ODTXXN08	8	TBD	156.9
ODTXXN12	12	TBD	163.7
ODTXXN16	16	TBD	173.1
ODTXXN24	24	TBD	184.9

a. See page 2-15 for power equation.

Pad Logic

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

ODTXXN01	Capacitive Load (pF)		15	25	35	50	75 (max)
	From: A To: PADM	t_{ZL}	6.55	9.90	13.24	18.24	26.55
ODTXXN02	Capacitive Load (pF)		15	50	75	100	150 (max)
	From: A To: PADM	t_{ZL}	3.25	9.06	13.05	17.03	25.12
ODTXXN04	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	1.93	4.75	8.75	16.74	24.70
ODTXXN08	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	1.17	2.55	4.52	8.47	12.40
ODTXXN12	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	0.99	1.95	3.28	5.92	8.56
ODTXXN16	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	0.96	1.73	2.74	4.72	6.70
ODTXXN24	Capacitive Load (pF)		15	50	100	200	300 (max)
	From: A To: PADM	t_{ZL}	0.84	1.49	2.23	3.56	4.90

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Tristate Timing

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

From	Delay (ns) To	Parameter	Cell						
			ODTXXN01	ODTXXN02	ODTXXN04	ODTXXN08	ODTXXN12	ODTXXN16	ODTXXN24
A	PADM	t_{LZ}	0.23	0.31	0.48	0.56	0.74	1.02	1.35

Pad Logic