SPECIFICATION

PART NO. : OEL9M1002-L4-E

This specification may be changed without any notice in order to improve performance or quality etc.
Please contact OLED R&D department TRULY Semiconductors LTD. for updated specification and product status before designing for this product or releasing the order.

PRODUCT CONTENTS

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REVISION HISTORY

Rev.	Contents	Date
1.0	First release.	2012-09-18

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	1.12	Inch
2	Resolution	128(W)*RGB * 36(H)	Dots
3	Active Area	27.24(W) x 7.76(H)	mm^2
4	Outline Dimension (Panel)	33.36(W) x 18.00(H)	mm^2
5	Pixel Pitch	0.213(W) x 0.216(H)	mm^2
6	Pixel Size	0.183(W) x 0.186(H)	mm^2
7	Driver IC	SSD1351Z	-
8	Display Color	65K / 262K	-
9	Interface	8/16/18-bit Parallel / 3,4wire-SPI	-
10	IC package type	COG	-
11	Thickness	1.45±0.1	mm
12	Weight	≦2.0	g
13	Duty	1/36	-

■ ABSOLUTE MAXIMUM RATINGS

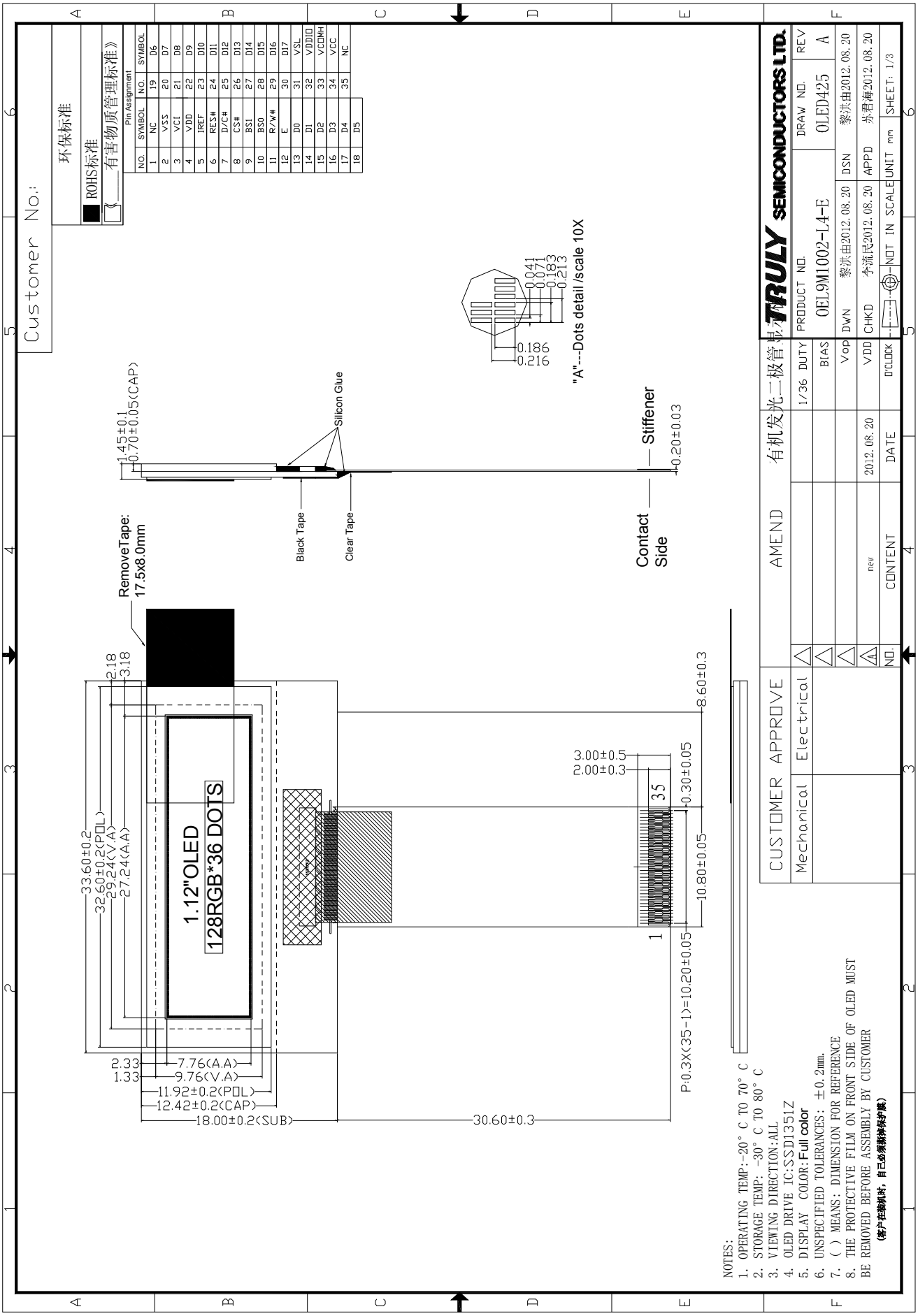
Voltage Referenced to VSS

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	I/O Power	VDDIO	-0.5	-	V_{CI}	V
	Low Power	VCI	-0.3	-	4.0	V
	Driving	VCC	-0.5	-	19.0	V
SEG Output Voltage		V_{SEG}	0	-	VCC	V
COM Output Voltage		V_{COM}	0	-	$0.9*V_{CC}$	V
Operating Temperature		Top	-20	-	70	℃
Storage Temperature		Tst	-30	-	80	℃
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

◆ DC Characteristics

Unless otherwise specified, V_{SS} = 0V ,V_{CI}=2.4V to 3.5V (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Operating	VCC	10.0	12.0	18.0	V
	I/O Power	VDDIO	1.65	-	VCI	V
	Low Power	VCI	2.4	-	3.5	V
Input Voltage	High Voltage	V_{IH}	0.8 x VDDIO	-	VDDIO	V
	Low Voltage	V_{IL}	0	-	0.2 x VDDIO	V
Output Voltage	High Voltage	V_{OH}	0.9 x VDDIO	-	VDDIO	V
	Low Voltage	V_{OL}	0	-	0.1 x VDDIO	V

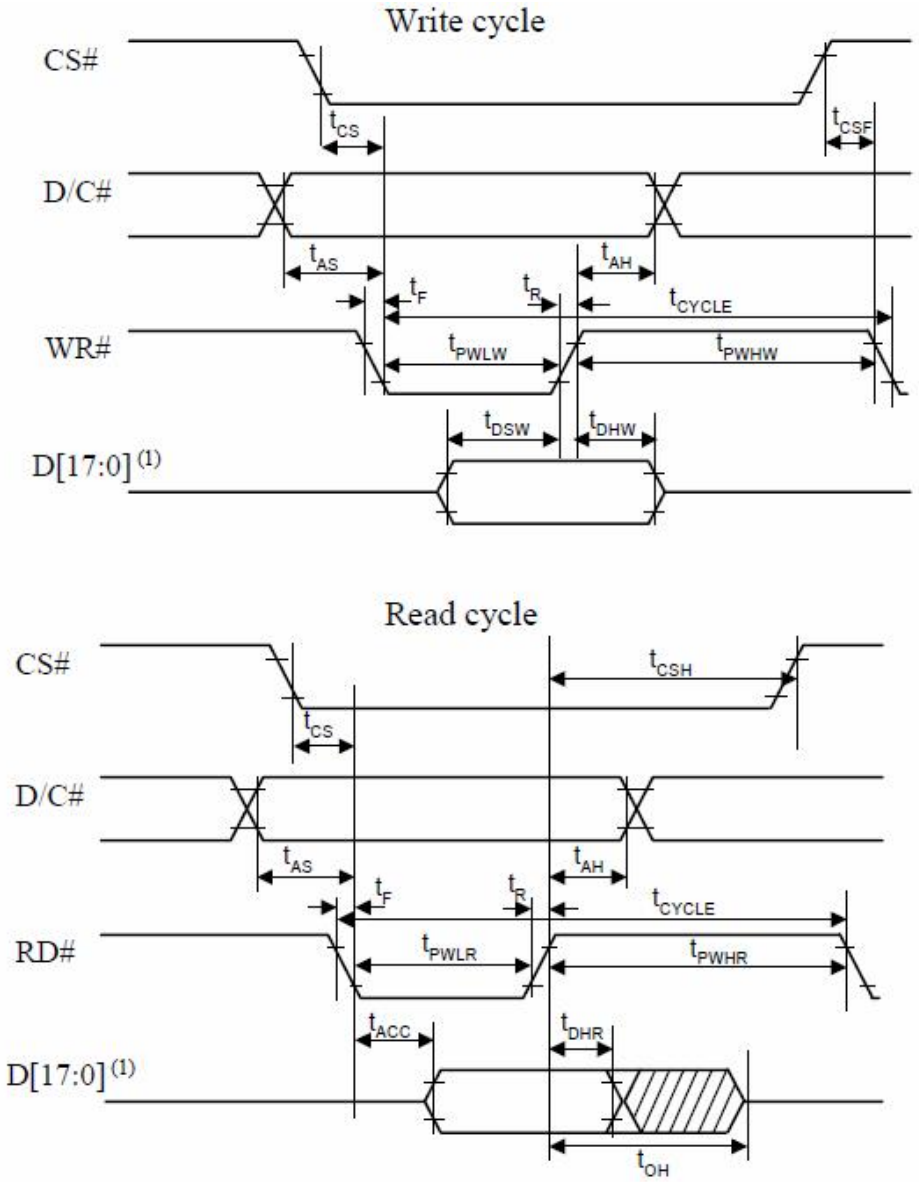
◆AC Characteristics

◆ 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DDIO}- V_{SS} =1.65V- V_{CI}, V_{CI} - V_{SS} = 2.4-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	46	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics



Note

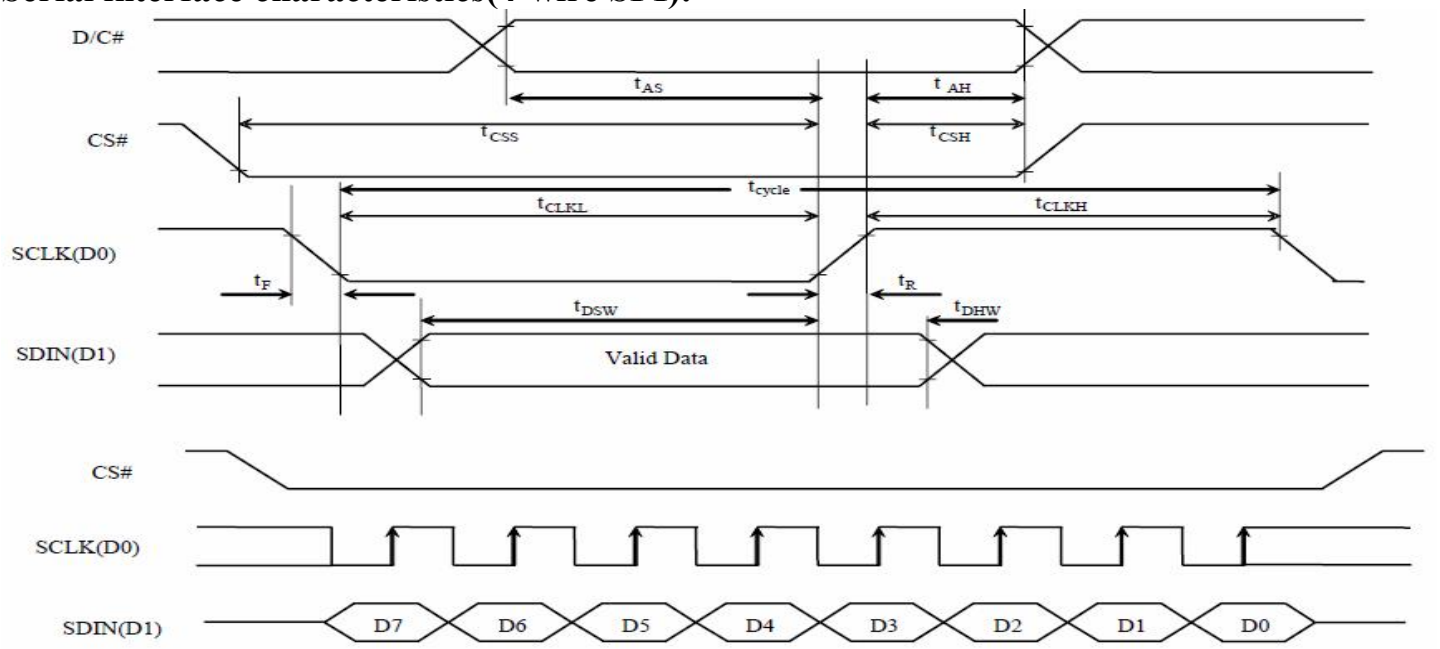
(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

◆Serial Interface Timing Characteristics(4-wire SPI)

(V_{DDIO}- V_{SS} =1.65V- V_{CI}, V_{CI} - V_{SS} = 2.4-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	42	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics(4-wire SPI):

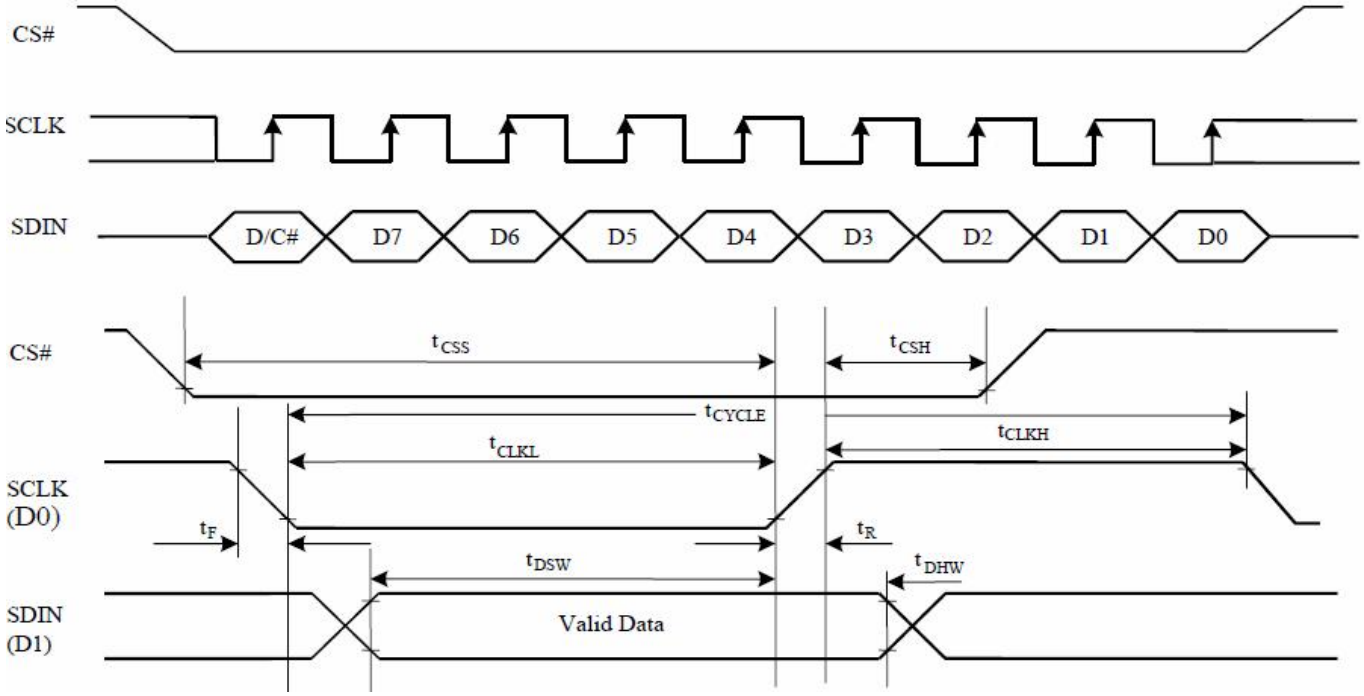


Serial Interface Timing Characteristics (3-wire SPI):

(V_{DDIO}- V_{SS} =1.65V- V_{CI}, V_{CI} - V_{SS} = 2.4-3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	44	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial interface characteristics(3-wire SPI)



◆Data bus to Driver IC RAM mapping under different input mode

Write Data bus usage under different bus width and color depth mode:

Write Data			Data bus																	
Bus width	Color Depth	Input order	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits/Serial	65k	1st	X	X	X	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits/Serial	262k	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	X	X	X	X	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0
		3rd	X	X	X	X	X	X	X	X	X	X	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	65k		X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 1	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 2	1st	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$
		3rd	X	X	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$
18 bits	262k		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

Read Data bus usage under different bus width and color depth mode:

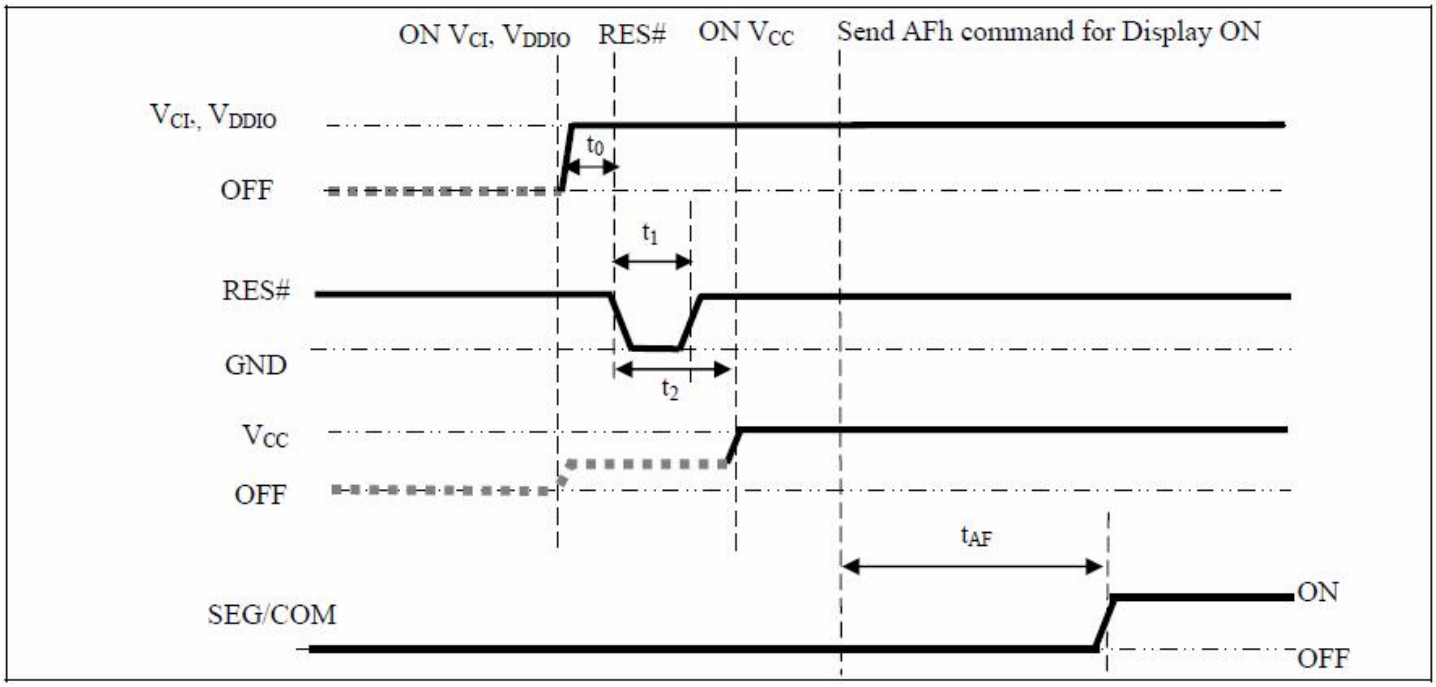
Read Data			Data bus																	
Bus width	Color Depth	Input order	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	65k	1st	X	X	X	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits	262k	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	X	X	X	X	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0
		3rd	X	X	X	X	X	X	X	X	X	X	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	65k		X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 1	1st	X	X	X	X	X	X	X	X	X	X	X	X	C_5	C_4	C_3	C_2	C_1	C_0
		2nd	X	X	X	X	B_5	B_4	B_3	B_2	B_1	B_0	X	X	A_5	A_4	A_3	A_2	A_1	A_0
16 bits	262k format 2	1st	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$
		2nd	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$
		3rd	X	X	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$
18 bits	262k		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

■ TIMING OF POWER SUPPLY

The following figures illustrate the recommended power ON and power OFF sequence of SSD1351 (assume VCI and VDDIO are at the same voltage level).

◆***Power ON sequence***:

1. Power ON VCI, VDDIO.
2. After VCI, VDDIO become stable, set wait time at least 1ms (t0) for internal VDD become stable. Then set RES# pin LOW (logic low) for at least 2us (t1) (4) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t2). Then Power ON VCC(1).
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (tAF).
5. After VCI become stable, wait for at least 300ms to send command.

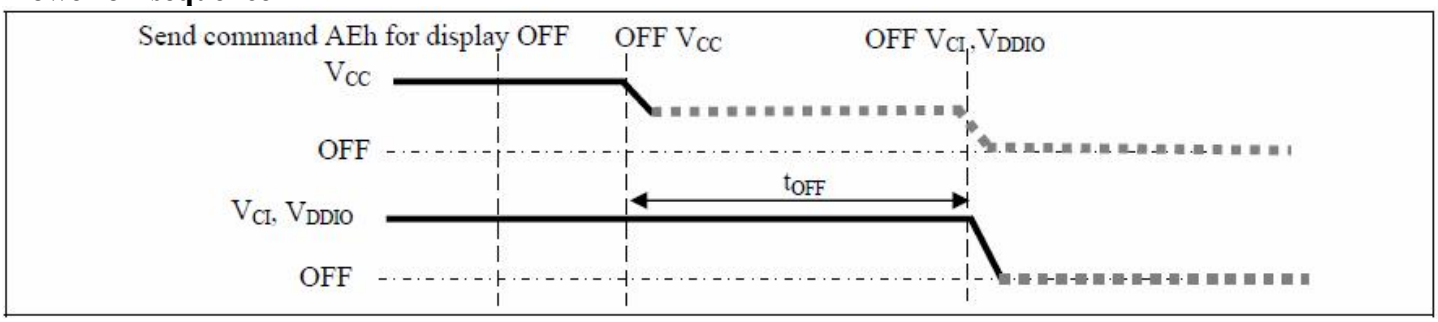


◆***Power OFF sequence***:

1. Send command AEh for display OFF.
2. Power OFF VCC.(1), (2)
3. Wait for tOFF. Power OFF VCI, VDDIO.

(where Minimum tOFF=0ms (3), Typical tOFF=100ms)

Power off sequence



Note:

(1) Since an ESD protection circuit is connected between VCI, VDDIO and VCC, VCC becomes lower than VCI whenever VCI,
VDDIO is ON and VCC is OFF as shown in the dotted line of VCC in Figure above.
(2)VCC should be kept float (disable) when it is OFF.
(3) VCI, VDDIO should not be Power OFF before VCC Power OFF.
(4) The register values are reset after t1.
(5) Power pins (VCI, VDDIO and VCC) can never be pulled to ground under any circumstance.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Luminance		L	75	90*	-	cd /m^2	With Polarizer All pixels on
Power Consumption		P	-	70	95	mW	40% pixels On
Frame Frequency		Fr	-	120	-	Hz	-
Color Coordinate		CIE x CIE y	0.26 0.29	0.30 0.33	0.34 0.37	CIE1931	White
		CIE x CIE y	0.60 0.31	0.64 0.35	0.68 0.39		Red
		CIE x CIE y	0.27 0.56	0.31 0.60	0.35 0.64		Green
		CIE x CIE y	0.11 0.11	0.15 0.15	0.19 0.19		Blue
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	5000:1	-	-	-	With Polarizer
Viewing Angle		△ θ	170	-	-	Degree	-
Operating Life Time*		Top	10,000	-	-	Hours	-

Note:

1. **90cd/m^2** test condition:
   Voltage driving: VCI=3.0V, VCC=12.0V;
   Contrast Setting:
   Master contrast register value is 0x02;
   Blue contrast register value is 0xA4;
   Green contrast register value is 0x71;
   Red contrast register value is 0x5F;
2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternatively displayed)
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No	Symbol	Description
1	NC(GND)	No connection or connected to GND
2	VSS	Ground
3	VCI	Low voltage power supply VCI must always be equal to or higher than VDDIO.
4	VDD	Power supply for core logic operation. A capacitor is necessary to connected between
5	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.
6	RES#	reset signal input, low active
7	D/C#	Data/Command control pin connecting to the MCU..
8	CS#	The chip select pin. Active low.
9	BS1	MCU bus interface selection pins.
10	BS0	
11	WR#	When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#)selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to VSS.
12	RD#	When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to VSS.
13-30	D0-D17	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode)
31	VSL	This is segment output current reference pin. A resistor should be connected between this pin and VSS to maintain the IREF current at 10uA.
32	VDDIO	Power supply for interface logic level. It should match with the MCU interface
33	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
34	VCC	Power supply for panel driving voltage. This is also the most positive power voltage
35	VSS	Ground

MCU Bus Interface Pin Selection:

Select appropriate logic setting as described in the following table. BS3 and BS2 are command programmable (by command ABh). [reset = 00]. BS1 and BS0 are Pin select.

BS[3:0]	INTTERFACE
XX00	4 line SPI
XX01	3 line SPI
0011	8-bit 6800 parallel
0010	8-bit 8080 parallel
0111	16-bit 6800 parallel
0110	16-bit 8080 parallel
1111	18-bit 6800 parallel
1110	18-bit 8080 parallel

Note

(1) 0 is connected to VSS

(2) 1 is connected to VDDIO

■ COMMAND TABLE

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1 1	15 A[6:0] B[6:0]	0 * *	0 A_6 B_6	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0 1 1	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row Address	A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0 1	A0 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 127 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Reserved A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b / 01b: 65k color [reset] 10b: 262k color 11b 262k color, 16-bit format 2 Refer to Table 8-8 for details

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~127. [reset=00h]
0 1	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-127. [reset=60h] **Note** (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0 1	AB A[7:0]	1 A_7	0 A_6	1 0	0 0	1 0	0 0	1 0	1 A_0	Function Selection	A[0]=0b, Disable internal V_{DD} regulator (for power save during sleep mode only) A[0]=1b, Enable internal V_{DD} regulator [reset] A[7:6]=00b, Select 8-bit parallel interface [reset] A[7:6]=01b, Select 16-bit parallel interface A[7:6]=11b, Select 18-bit parallel interface
0	AD	1	0	1	0	1	1	0	1	NOP	Command for no operation.
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 5~31 DCLK(s) clocks [reset=0010b] A[3:0]: 0-1 invalid 2 = 5 DCLKs 3 = 7 DCLKs : 15 = 31DCLKs A[7:4] Phase 2 period of 3~15 DCLK(s) clocks [reset=1000b] A[7:4]: 0-2 invalid 3 = 3 DCLKs 4 = 4 DCLKs : 15 =15DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2 (2)This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B2	1	0	1	1	0	0	1	0	Display Enhancement	A[7:0] = 00h, B[7:0] = 00h, C[7:0] = 00h normal [reset] A[7:0] = A4h, B[7:0] = 00h, C[7:0] = 00h enhance display performance
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	0	0	0	0	0	0	0	0		
1	C[7:0]	0	0	0	0	0	0	0	0		
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0001], divide by DIVSET where A[3:0] DIVSET: 0000 divide by 1; 0001 divide by 2; 0010 divide by 4; 0011 divide by 8; 0100 divide by 16; 0101 divide by 32; 0110 divide by 64; 0111 divide by 128; 1000 divide by 256; 1001 divide by 512; 1010 divide by 1024; >=1011 invalid A[7:4] Oscillator frequency, frequency increases as level increases [reset=1101b] **Note** (1) This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B4	1	0	1	1	0	1	0	0	Set Segment Low Voltage (VSL)	A[1:0]=00 External VSL [reset] A[1:0]=01,10,11 are invalid **Note** (1) When external VSL is enabled, in order to avoid distortion in display pattern, an external circuit is needed to connect between VSL and V_{SS} as shown in Figure 14-1.
1	A[7:0]	1	0	1	0	0	0	A_1	A_0		
1	B[7:0]	1	0	1	1	0	1	0	1		
1	C[7:0]	0	1	0	1	0	1	0	1		
0	B5	1	0	1	1	0	1	0	1	Set GPIO	A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	B8	1	0	1	1	1	0	0	0	Look Up Table for Gray Scale Pulse width	The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS62 < Setting of GS63 (2) GS0 has only pre-charge but no current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A62[7:0]	$A62_7$	$A62_6$	$A62_5$	$A62_4$	$A62_3$	$A62_2$	$A62_1$	$A62_0$		
1	A63[7:0]	$A63_7$	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: GS1 = 0 DCLK GS2 = 2 DCLK GS3 = 4 DCLK GS4 = 6 DCLK ... GS62 = 122 DCLK GS63 = 124 DCLK
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 17h]
1	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		

A[4:0]	Hex code	pre-charge voltage
00000	00h	0.20 x V_{CC}
:	:	:
11111	1Fh	0.60 x V_{CC}

Note
(1)This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 05h]
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		

A[2:0]	Hex code	V_{COMH}
000	00h	0.72 x V_{CC}
:	:	:
101	05h	0.82 x V_{CC} [reset]
:	:	:
111	07h	0.86 x V_{CC}

Note
(1)This command is locked by Command FDh by default. To unlock it, please refer to Command FDh.

Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0 1 1 1	C1 A[7:0] B[7:0] C[7:0]	1 A_7 B_7 C_7	1 A_6 B_6 C_6	0 A_5 B_5 C_5	0 A_4 B_4 C_4	0 A_3 B_3 C_3	0 A_2 B_2 C_2	0 A_1 B_1 C_1	1 A_0 B_0 C_0	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=10001010b] B[7:0] Contrast Value Color B [reset=01010001b] C[7:0] Contrast Value Color C [reset=10001010b]
0 1	C7 A[3:0]	1 *	1 *	0 *	0 *	0 A_3	1 A_2	1 A_1	1 A_0	Master Contrast Current Control	A[3:0] : 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
0 1	CA A[6:0]	1 0	1 A_6	0 A_5	0 A_4	1 A_3	0 A_2	1 A_1	0 A_0	Set MUX Ratio	A[6:0] MUX ratio 16MUX ~ 128MUX, [reset=127], (Range from 15 to 127)
0	D1	1	0	1	0	1	1	0	1	NOP	Command for No Operation
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation
0 1	FD A[7:0]	1 A_7	1 A_6	1 A_5	1 A_4	1 A_3	1 A_2	0 A_1	1 A_0	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12b, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16b, Lock OLED driver IC MCU interface from entering command A[7:0] = B0b, Command A2,B1,B3,BB,BE,C1 inaccessible in both lock and unlock state [reset] A[7:0] = B1b, Command A2,B1,B3,BB,BE,C1 accessible if in unlock state **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.

Graphic Acceleration Command List

Graphic acceleration command											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D2	D0	Command	Description
0	96	1	0	0	1	0	1	1	0	Horizontal Scroll	A[7:0] = 00000000b No scrolling A[7:0] = 00000001b to 00111111b Scroll towards SEG127 with 1 column offset A[7:0] = 01000000b to 11111111b Scroll towards SEG0 with 1 column offset B[6:0] : start row address C[7:0] : number of rows to be H-scrolled B+C <= 128 D[6:0] : Reserved (reset=00h) E[1:0] : scrolling time interval 00b test mode 01b normal 10b slow 11b slowest **Note** (1) Operates during display ON.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[6:0]	0	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
1	D[6:0]	0	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
1	E[1:0]	0	0	0	0	0	0	E_1	E_0		
0	9E	1	0	0	1	1	1	1	0	Stop Moving	Stop horizontal scroll **Note** (1) After sending 9Eh command to stop the scrolling action, the ram data needs to be rewritten
0	9F	1	0	0	1	1	1	1	1	Start Moving	Start horizontal scroll

Note

(1) After executed the graphic command, waiting time is required for update GDDRAM content. VCI =2.4~3.5V, waiting time = 500ns/pixel.

(2) "*" stands for "Don't care".

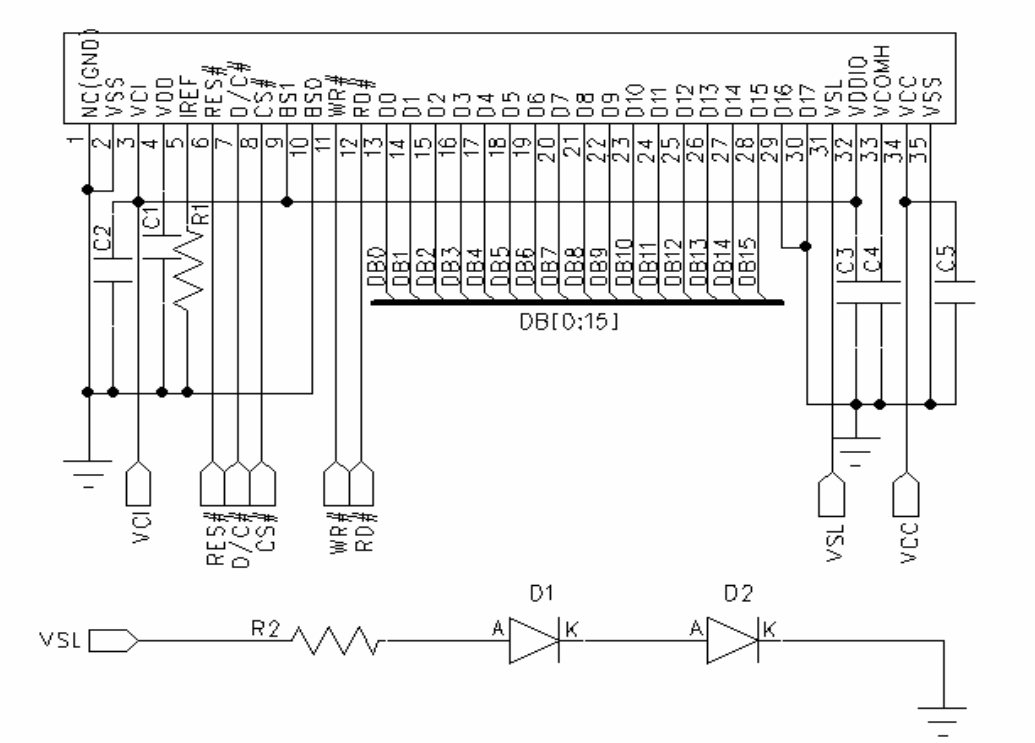
■ INITIALIZATION CODE

```
    void InitOLED_SSD1351()
{
 WMOLED_COM(0xFD); WMOLED_DATA(0xB1); //SET COMMAND LOCK
 WMOLED_COM(0xAE);                    //SET DISPLAY OFF

 WMOLED_COM(0x15); WMOLED_DATA(0x00);  // Set column address
                   WMOLED_DATA(0x7F);
 WMOLED_COM(0x75); WMOLED_DATA(0x00);  // Set row address
                   WMOLED_DATA(0x23);

 WMOLED_COM(0xA0); WMOLED_DATA(0x20);  // Re_map&Depth color
 WMOLED_COM(0xA1); WMOLED_DATA(0x00);  // Set display start line
 WMOLED_COM(0xA2); WMOLED_DATA(0x00);  // Set display offset
 WMOLED_COM(0xA6);                     // Set display mode
 WMOLED_COM(0xCA); WMOLED_DATA(0x23);  // Set multiplex ratio
 WMOLED_COM(0xB2); WMOLED_DATA(0x00);   //Display Enhancement
                   WMOLED_DATA(0x00);
                   WMOLED_DATA(0x00);

  WMOLED_COM(0xC7); WMOLED_DATA(0x02);  //Master ContrastCurrent Control
  WMOLED_COM(0xC1); WMOLED_DATA(0xA4);  //Contrast Current for Color A,B,C
                    WMOLED_DATA(0x71);
                    WMOLED_DATA(0x5F);

 WMOLED_COM(0xAB); WMOLED_DATA(0x41); //Function selection:VDD mode(Internal VDD)&
                                      //Interface select(16 Bit Parallel)
  WMOLED_COM(0xB1); WMOLED_DATA(0x82);  // Set phase 1 and 2 preiod
  WMOLED_COM(0xB6); WMOLED_DATA(0x06);   // Set Second Pre_charge Period
  WMOLED_COM(0xB3); WMOLED_DATA(0x11);  // Clock divider/ Oscilator Frequency
  WMOLED_COM(0xB4); WMOLED_DATA(0xA0);  //Set Segment Low Voltage (VSL)
                    WMOLED_DATA(0xE5);
                    WMOLED_DATA(0x55);
  WMOLED_COM(0xBE); WMOLED_DATA(0x05);  //Set VCOMH=0.82 x VCC
  WMOLED_COM(0xBB); WMOLED_DATA(0x13);  // Set Pre-charge voltage

  //WMOLED_COM(0xB9);                    //Enable liner gray scale table
            WMOLED_COM(0xB8);           //Set gray scale table
            WMOLED_DATA(0x00);
            WMOLED_DATA(0x01);
            WMOLED_DATA(0x03);
            WMOLED_DATA(0x05);
            WMOLED_DATA(0x07);
            WMOLED_DATA(0x09);
            WMOLED_DATA(0x0B);
            WMOLED_DATA(0x0D);
            WMOLED_DATA(0x0F);
            WMOLED_DATA(0x11);
            WMOLED_DATA(0x13);
            WMOLED_DATA(0x15);
            WMOLED_DATA(0x17);
            WMOLED_DATA(0x19);
```

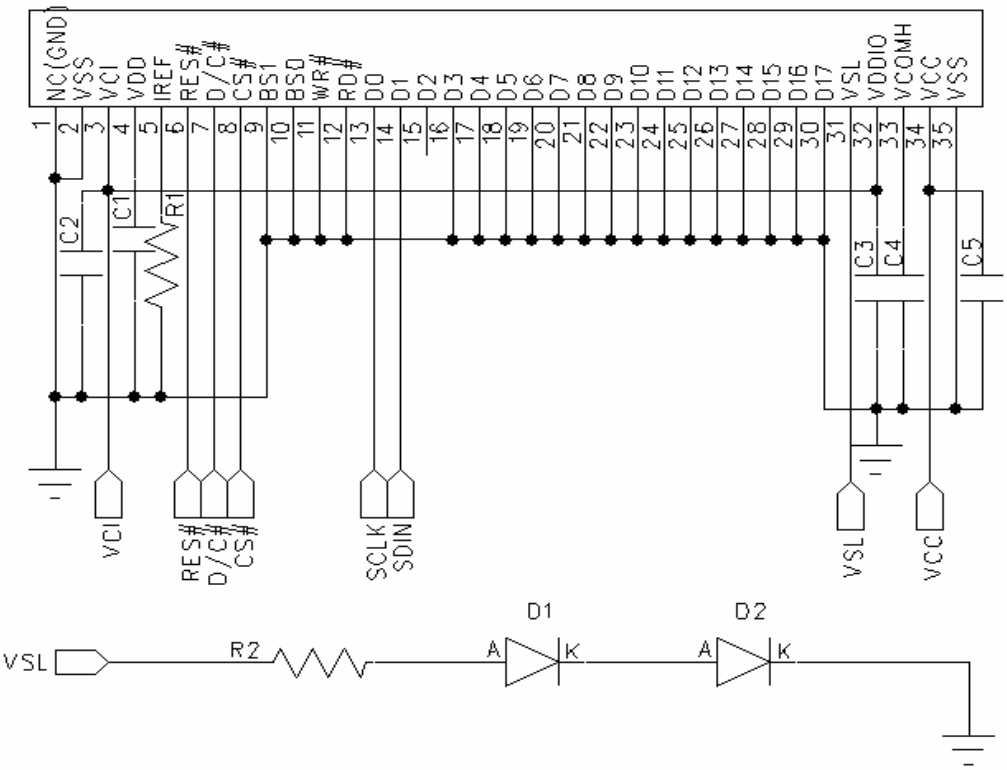
```
        WMOLED_DATA(0x1B);
        WMOLED_DATA(0x1D);
        WMOLED_DATA(0x1F);
        WMOLED_DATA(0x21);
        WMOLED_DATA(0x23);
        WMOLED_DATA(0x25);
        WMOLED_DATA(0x27);
        WMOLED_DATA(0x29);
        WMOLED_DATA(0x2B);
        WMOLED_DATA(0x2D);
        WMOLED_DATA(0x2F);
        WMOLED_DATA(0x31);
        WMOLED_DATA(0x33);
        WMOLED_DATA(0x33);
        WMOLED_DATA(0x35);
        WMOLED_DATA(0x37);
        WMOLED_DATA(0x39);
        WMOLED_DATA(0x3A);
        WMOLED_DATA(0x3C);
        WMOLED_DATA(0x3E);
        WMOLED_DATA(0x41);
        WMOLED_DATA(0x43);
        WMOLED_DATA(0x45);
        WMOLED_DATA(0x47);
        WMOLED_DATA(0x49);
        WMOLED_DATA(0x4B);
        WMOLED_DATA(0x4D);
        WMOLED_DATA(0x4F);
        WMOLED_DATA(0x51);
        WMOLED_DATA(0x53);
        WMOLED_DATA(0x55);
        WMOLED_DATA(0x57);
        WMOLED_DATA(0x59);
        WMOLED_DATA(0x5B);
        WMOLED_DATA(0x5D);
        WMOLED_DATA(0x5F);
        WMOLED_DATA(0x61);
        WMOLED_DATA(0x63);
        WMOLED_DATA(0x65);
        WMOLED_DATA(0x67);
        WMOLED_DATA(0x69);
        WMOLED_DATA(0x6B);
        WMOLED_DATA(0x6D);
        WMOLED_DATA(0x6F);
        WMOLED_DATA(0x71);
        WMOLED_DATA(0x73);
        WMOLED_DATA(0x75);
        WMOLED_DATA(0x77);
        WMOLED_DATA(0x79);
        WMOLED_DATA(0x7C);
 WMOLED_COM(0xAF);              //SET DISPLAY ON
Delayms(5);
}
```

■ SCHEMATIC EXAMPLE

◆16-bit 8080 parallel Interface Application Circuit:



◆4-wire SPI Application Circuit:



C1，C2，C3:1uF/6V;
C4, C5: 4.7 uF / 25V, tantalum type recommended;
R1:560Kohm/ 1%; R2: 50ohm/ 1%
D1, D2: MBR0530T1G

■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		80±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 96 hours	
Low Temperature Storage (LTS)		-30±2℃, 200 hours	
Low Temperature Operating (LTO)		-20±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

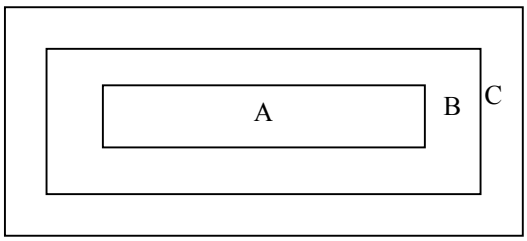
■ OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

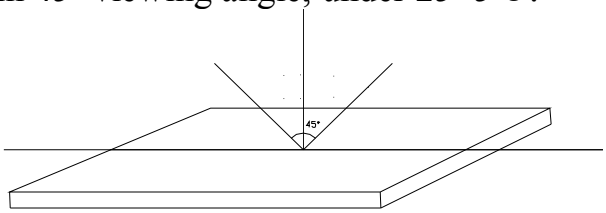
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



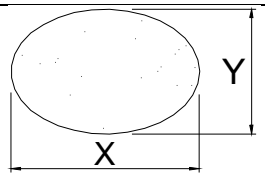
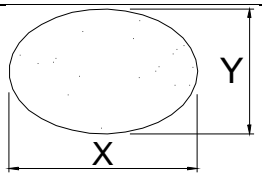
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

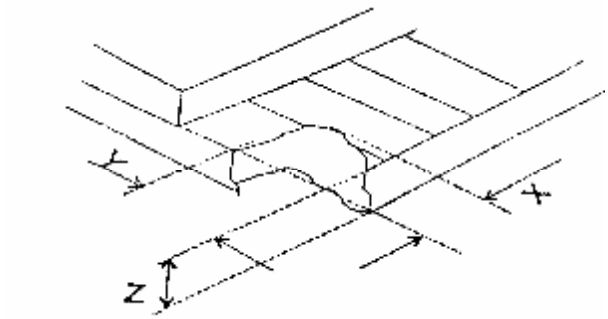
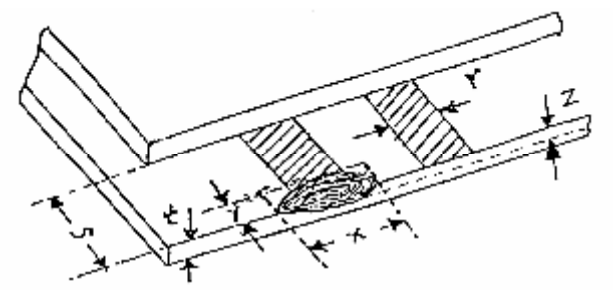
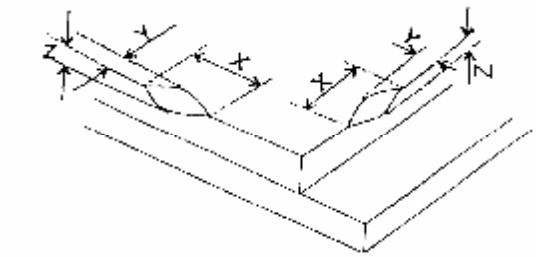
◆Inspection Criteria

1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="6">Spot Defect (dimming and lighting spot)</td><td colspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td colspan="2"></td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td>0.15＜Φ</td><td>0</td></tr>
<tr><td colspan="4">Note : Φ= (x + y) / 2</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="6">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4">  </td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
 
(mm)
<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
 
(mm)
<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
 
(mm)
<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module' s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.