

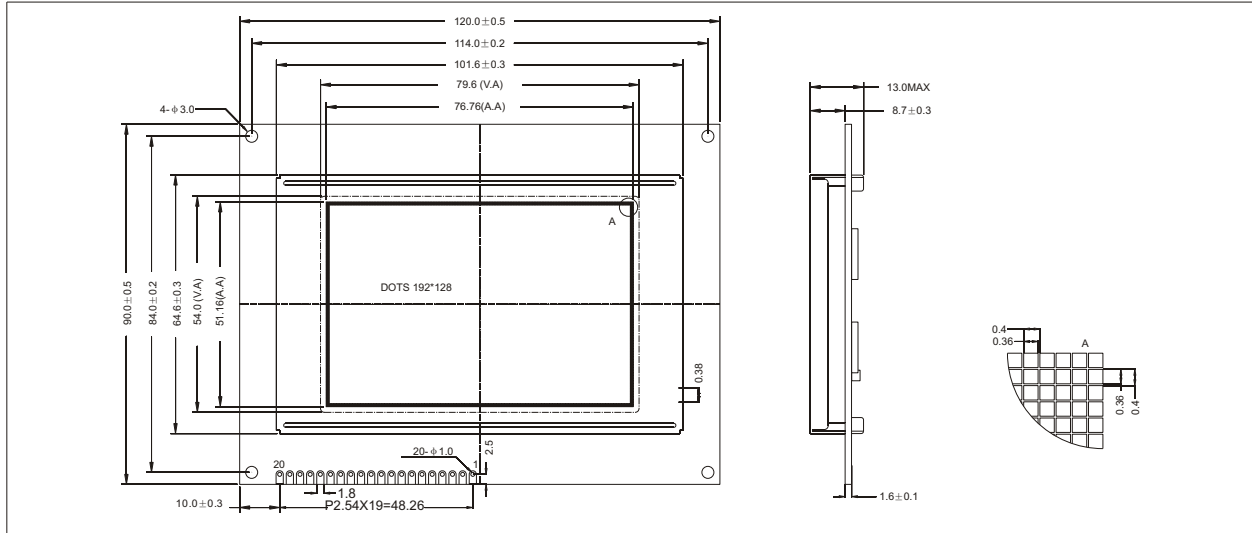


STANDARD GRAPHIC MODULES

OLG192128AY01

192 x 128 DOTS
1/128 DUTY, 1/12 BIAS

1 EXTERNAL DIMENSION AND DISPLAY PATTERN



2 MECHANICAL DATA

ITEM	SPECIFICATION	UNIT
Module Size(W*H*T)	98.0×86.0×13.0	mm
Viewing Area(W*H)	77.5×54.0	mm
Number of Dots	192×128	mm
Dot Pitch (W*H)	0.4×0.4	mm
Dot Size (W*H)	0.36×0.36	mm

3

PIN No.	SYMBOL	FUNCTION
1,2	DB3, DB2	Data Bit3, Data Bit2
3	FLM	First Line Marker
4	M	AC Signal For LCD Driver Output
5	CL1	Data Latch Clock
6	CL2	Data Shift Clock
7,8	DB1, DB0	Data Bit1, Data Bit0
9	V _{DD}	Logical High Input Port
10	V _{SS}	GND(0v)
11	V ₀	LCD Drive Output Voltage Level
12	FGND	Frame Ground
13	EL1	ELBacklight
14	EL2	ELBacklight

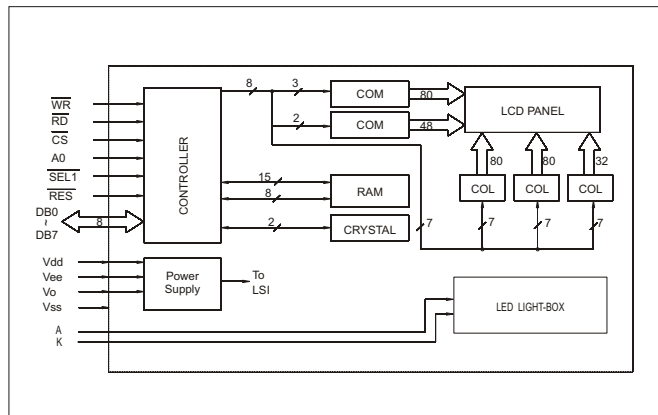
4 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage Logic	V _{DD} -V _{SS}	-0.3	7.0	V
Supply Voltage Driver	V _{DD} -V _{EE}	0	30.0	V
Intut Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Operating Temp		See page 9		
Storage Temp		See page 9		

5 ELECTRICAL CHARACTERISTICS(Ta=25 °C)

ITEM	SYMBOL	CONDITION	SPEC.VALUE			UNIT
			MIN.	TYP.	MAX.	
Supply Voltage (Logic)	V _{DD} -V _{SS}		2.7	5.0	5.5	V
Supply Current (Logic)	I _{DD}	V _{DD} =5V	-	1.2	1.6	mA
Input Voltage	HIGH	V _{HI}	0.8V _{DD}	-	V _{DD}	V
	LOW	V _{LI}	-	-	0.2V _{DD}	V
Output Voltage	HIGH	V _{OHI}	V _{DD} -0.4	-	-	V
	LOW	V _{OL}	-	-	0.4	V
LCD Operating Voltage	V _{DD} -V _{EE}	V _{DD} =5V Ta=25 °C	6	17.6	28	v
Supply Voltage LCD Drive	I _{EE}			1.0	1.1	mA

6 BLOCK DIAGRAM



7 BACKLIGHTING CHARACTERISTICS(Ta=25 °C)

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIX
Supply Voltage	V _{LED}			110(AC)		V
Power Consumption	P _{LED}					mW
Luminous						cd/m ²

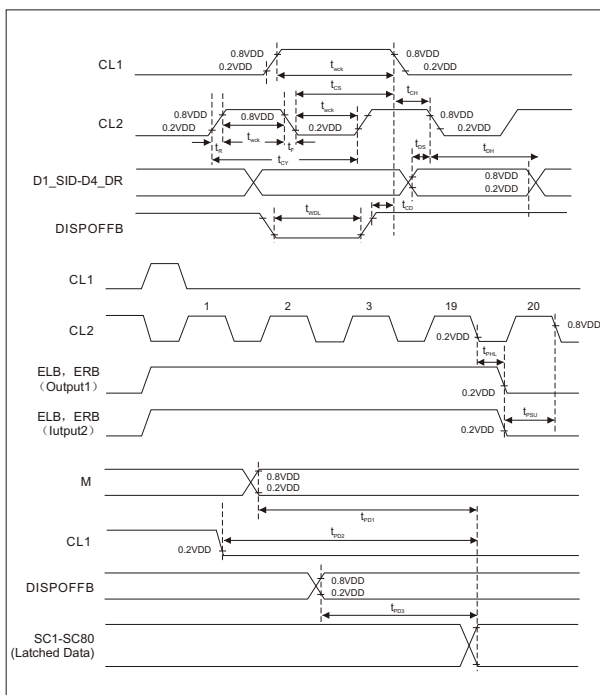


STANDARD GRAPHIC MODULES

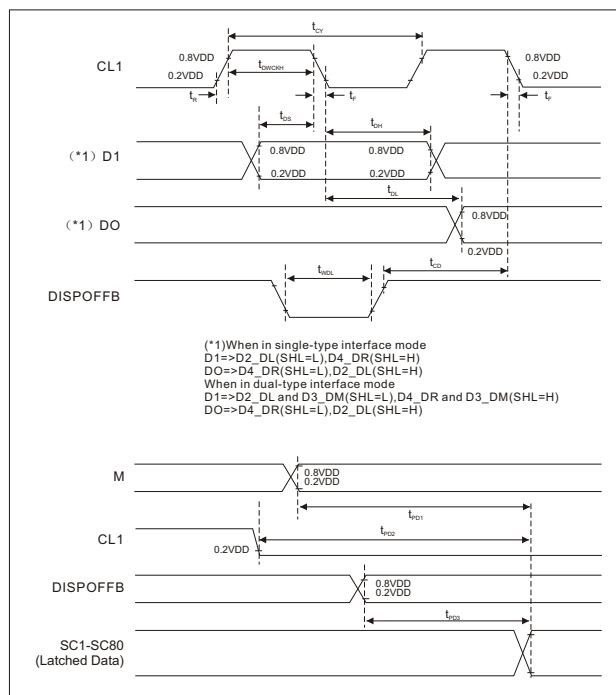
YMS192128-01

192x128DOTS
1/128DUTY, 1/12BIAS

8 SEGMENT DRIVER APPLICATION TIMING



9 COMMON DRIVER APPLICATION TIMING



10 AC CHARACTERISTICS

(1) Segment Driver Application

(V_{SS}=0V, T_a=-30~+85°C)

Characteristic	Symbol	Test Condition	(1)V _{DD} =5V±10%			(2)V _{DD} =3V±10%			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Clock cycle time	t _{CY}	Duty=50%	125	-	-	250	-	-	ns	
Clock pulse width	t _{WCK}	-	45	-	-	95	-	-		
Clock rise/fall time	t _{RIF}	-	-	-	-	-	-	30		
Data set-up time	t _{DS}	-	30	-	-	65	-	-		
Data hold time	t _{DH}	-	30	-	-	65	-	-		
Clock set-up time	t _{CS}	-	80	-	-	120	-	-		
Clock hold time	t _{CH}	-	80	-	-	120	-	-		
Propagation delay time	t _{PHL}	ELB Output	-	-	60	-	-	125		
		ERB Output	-	-	60	-	-	125		
ELB ERB set-up time	t _{PSU}	ELB Input	30	-	-	65	-	-		
		ERB Input	30	-	-	65	-	-		
DISPOFFB low pulse width	t _{WDL}	-	1.2	-	-	1.2	-	-		μs
DISPOFFB clear time	t _{CD}	-	100	-	-	100	-	-		ns
M-OUT propagation delay time	t _{PD1}	C _L =15pF	-	-	1.0	-	-	1.2	μs	
CLI-OUT propagation delay time	t _{PD2}		-	-	1.0	-	-	1.2		
DISPOFFB-OUT propagation delay time	t _{PD3}		-	-	1.0	-	-	-		

(2) Common Driver Application

(V_{SS}=0V, T_a=-30~+85°C)

Characteristic	Symbol	Test Condition	(1)V _{DD} =5V±10%			(2)V _{DD} =3V±10%			Unit	
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Clock cycle time	t _{CY}	Duty=50%	250	-	-	500	-	-	ns	
Clock pulse width	t _{WCK}	-	45	-	-	95	-	-		
Clock rise/fall time	t _{RIF}	-	-	-	50	-	-	50		
Data set-up time	t _{DS}	-	30	-	-	65	-	-		
Data hold time	t _{DH}	-	30	-	-	65	-	-		
DISPOFFB low pulse width	t _{WDL}	-	1.2	-	-	1.2	-	-		μs
DISPOFFB clear time	t _{CD}	-	100	-	-	100	-	-		ns
Output delay time	t _{DL}	C _L =15pF	-	-	200	-	-	250		μs
M-OUT propagation delay time	t _{PD1}		-	-	1.0	-	-	1.2		
CLI-OUT propagation delay time	t _{PD2}		-	-	1.0	-	-	1.2		
DISPOFFB-OUT propagation delay time	t _{PD3}		-	-	1.0	-	-	1.2		