PULSE DIALLER WITH REDIAL

The OM1036C is a single chip silicon-gate C-MOS integrated circuit. It is intended to convert pushbutton keyboard entries into streams of correctly-timed line current interruptions. The input data is derived from a telephone keyboard with a 3 x 4 pushbutton matrix. Numbers with up to 23 digits can be retained in a RAM for redial. A delayed reset is built-in for line power breaks.

The OM1036C can regenerate access pauses during redial. During the original entry, access pauses are stored via the keyboard. A regenerated access pause can be terminated during redial in two ways: via the keyboard, or with an external dial tone recogniser circuit. This makes the circuit very suitable for redial in PABX (Private Automatic Branch Exchange) systems.

The circuit has the following features:

- Operation from 2,0 V to 6 V supply.
- Static standby operation down to 1,5 V.
- Low current consumption; typ. 20 μA.
- Low static standby current; typ. 0,65 μA.
- Low-cost RC oscillator; 13,8 kHz.
- Fully decoded and debounced inputs for 3 x 4 matrix keyboard.
- 23-digit capacity, including access pauses, for redial operation.
- Memory overflow possibility (with internally disabled redial).
- Selectable dialling pulse frequency: 10 Hz and 20 Hz.
- Selectable dialling pulse mark/space ratios; 2 : 1 or 3 : 2.
- Hold facility for lengthening the inter-digit period.
- Circuit reset for line power breaks; > 160 ms (10 Hz dialling pulse frequency).
- Access pause generation via the keyboard.
- Access pause reset:
  via the keyboard,
  with external tone recogniser.
- All inputs with pull-up/pull-down (except CE and RC1).
- All inputs are internally protected against electrostatic charges.
- High input noise immunity.

PACKAGE OUTLINE

OM1036CP: 18-lead DIL; plastic (SOT102G,N,PE).

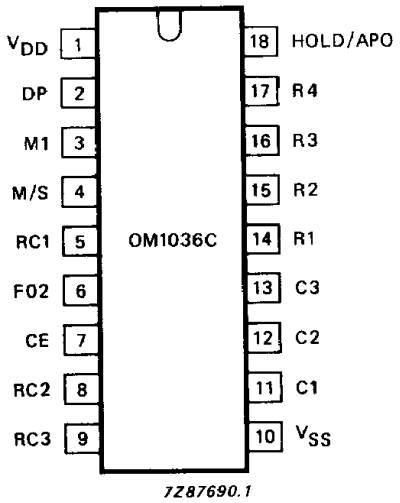


Fig. 1 Pinning diagram.

PINNING

1	V_{DD}	positive supply
10	V_{SS}	negative supply

Inputs

4	M/S	controls the mark-to-space ratio of the line pulses
6	F02	the dialling pulse frequency is defined by the logic state of this input
7	CE	Chip Enable; used to initialize the system; to select between the operational mode and the static standby mode; to handle line power breaks
11	C1	column keyboard inputs with pull-up on chip
12	C2	
13	C3	
14	R1	row keyboard outputs with pull-down on chip
15	R2	
16	R3	
17	R4	

Outputs

2	DP	Dialling Pulse; drive of the external line switching transistor or relay
3	M1	Muting; normally used for muting during the dialling sequence

Input/output

18	HOLD/APO	This pin will go HIGH when an access pause code is read from the memory during pulsing and will interrupt dialling. It can also be externally controlled; it will interrupt dialling after completion of the current digit or immediately during an inter-digit pause (t_{id}); further keyboard data will be accepted.

Oscillator

5	RC1	input/output of the RC on-chip oscillator
8	RC2	
9	RC3	

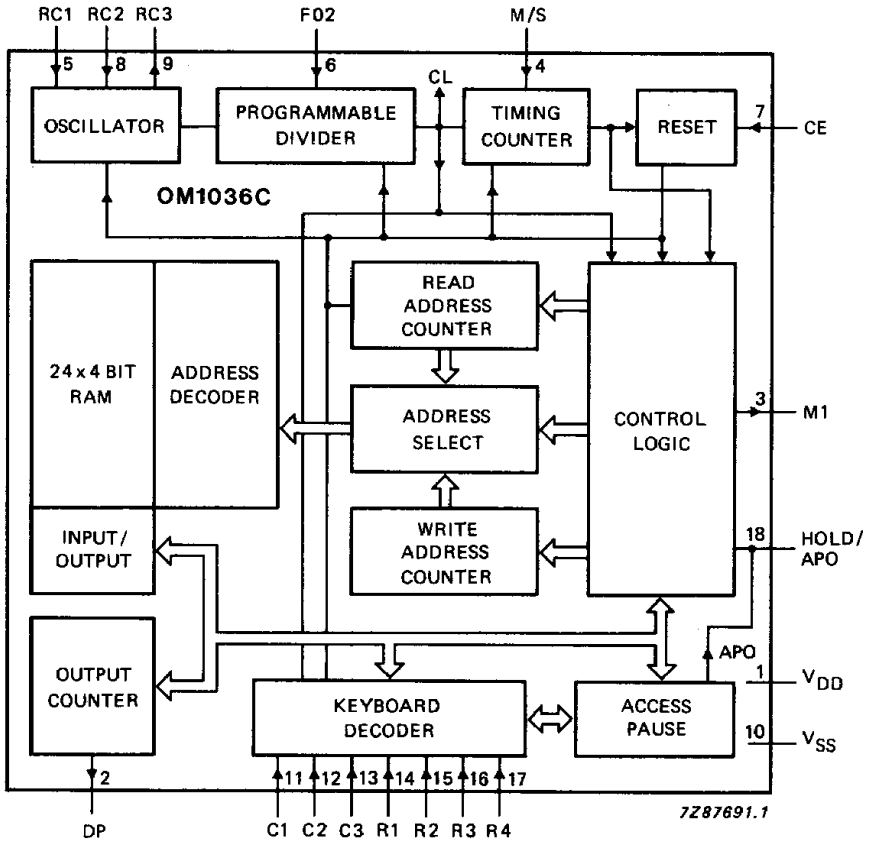


Fig. 2 Block diagram.

FUNCTIONAL DESCRIPTION (see also Fig. 2)

Clock oscillator (RC1, RC2, RC3)

The time base for the OM1036C is an RC controlled on-chip oscillator which is completed by connecting two resistors and a capacitor between the RC1, RC2 and RC3 pins (see Fig. 5). The oscillator is followed by a frequency divider of which the division ratio can be externally set (F02) to provide one of two chip system clocks (10 Hz or 20 Hz pulse frequencies).

Chip Enable (CE)

The CE input is used to initialize the chip system.

CE = LOW provides the static standby condition. In this mode the clock oscillator is off and internal registers are clamped reset with the exception of the WRITE ADDRESS COUNTER (WAC). The keyboard input is inhibited, but data previously entered is saved in the RAM.

When CE = HIGH the clock oscillator is operating, the internal registers are enabled and data can be entered from the keyboard.

If the CE input is taken to a LOW level for more than the time t_{rd} (see Figs 6 and 7 and timing data) an internal reset pulse will be generated at the end of the t_{rd} period. The system is then in the static standby mode. Short CE pulses of $< t_{rd}$ will not affect the operation of the circuit. No reset pulses are then produced.

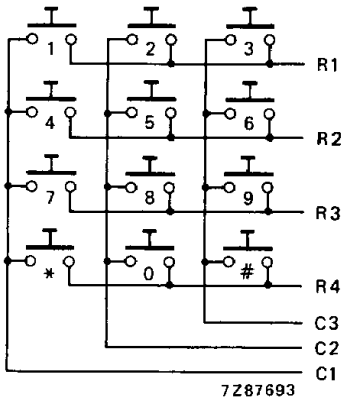
Debouncing keyboard entries (C1 to C3; R1 to R4)

The column keyboard inputs to the integrated circuits (C_n) and the row keyboard outputs (R_n) are for direct connection to a 3 x 4 single contact keyboard matrix (with or without common contact) as shown in Fig.3, or to a double contact keyboard with a common left open contact (see Fig.4). An entry is decoded into a 4-bit binary keycode by the keyboard decoder when one column input is connected to one row input. Any other input combinations are not valid and will not be accepted. Valid inputs are debounced on the leading and trailing edges as shown in Fig.6. Keyboard entries are only decoded into 4-bit binary keycodes and written into the RAM if the keyboard contact remains closed for five or six clock pulse periods (entry period t_e). The next keyboard entry will not be accepted until the previously closed contact has been left open for four or five clock pulse periods. The one clock pulse period of uncertainty in the debouncing process arises because keyboard entries are not detected until the leading edge of the first clock pulse after the entry.

Data entry

After each keyboard entry has been debounced and decoded, the keycode is written into the RAM, and the WAC is incremented by one to select the next RAM location where the next keycode will be stored. As each keycode is recalled from the RAM for line pulsing, the READ ADDRESS COUNTER (RAC) is incremented by one to select the RAM location of the next keycode to be recalled. Consequently, the difference between the contents of the WAC and of the RAC represents the number of keycodes that have been written into the RAM but not yet converted into line pulses. If more than 23 keycodes are written into the RAM, memory overflow results and the excess keycode replace the data in the lower numbered RAM locations. In this event, since an erroneous number is stored, automatic redialling is inhibited until the WAC has been reset by the first digit entry of the next telephone call.

If the first pushbutton to be pressed is not redial (#), the WAC is reset during entry time t_e, the corresponding keycode is written into the first RAM location, and the WAC is then incremented by one. If the first pushbutton to be pressed is redial (#), the WAC is not reset and the keycodes stored in the RAM are sequentially recalled and converted into correctly timed dialling pulses at output DP. If the redial pushbutton (#) is operated again during the redialling sequence it will be decoded as an Access Pause Reset. This function will be described later during the description of the access pause system of the OM1036C. During redial no keyboard entry will be accepted and stored in the RAM. But, when all in the RAM stored numbers have been pulsed out, new keyboard entry will be accepted, stored at the RAM position after the last digit code of the original entry and converted into correctly timed dialling pulses.



★ Access pause set.

Redial or Access Pause Reset.

Fig. 3 Single contact keyboard.

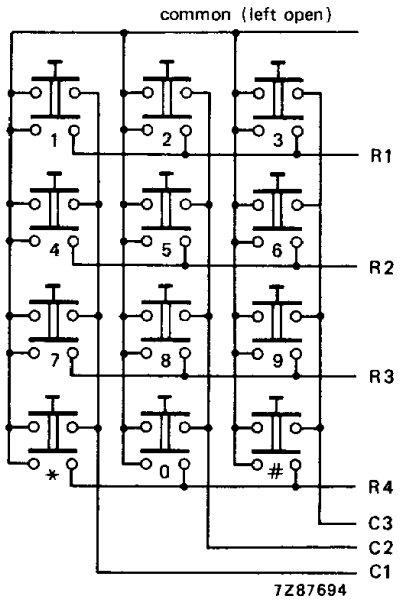


Fig. 4 Double contact keyboard.

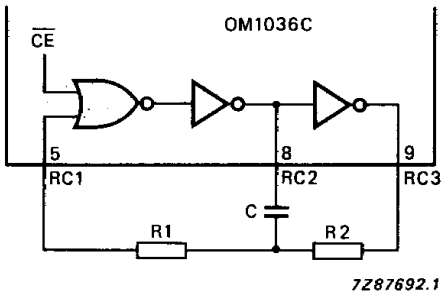


Fig. 5 Oscillator configuration.

$$f_{osc} \approx \frac{1}{2{,}7 \times R2 \times C} \text{ for } R1 \gg R2$$

with:

R1 = 560 kΩ
R2 = 220 kΩ
C = 120 pF
} f_{osc} = 13,8 kHz

C = ceramic capacitor (type NP0)

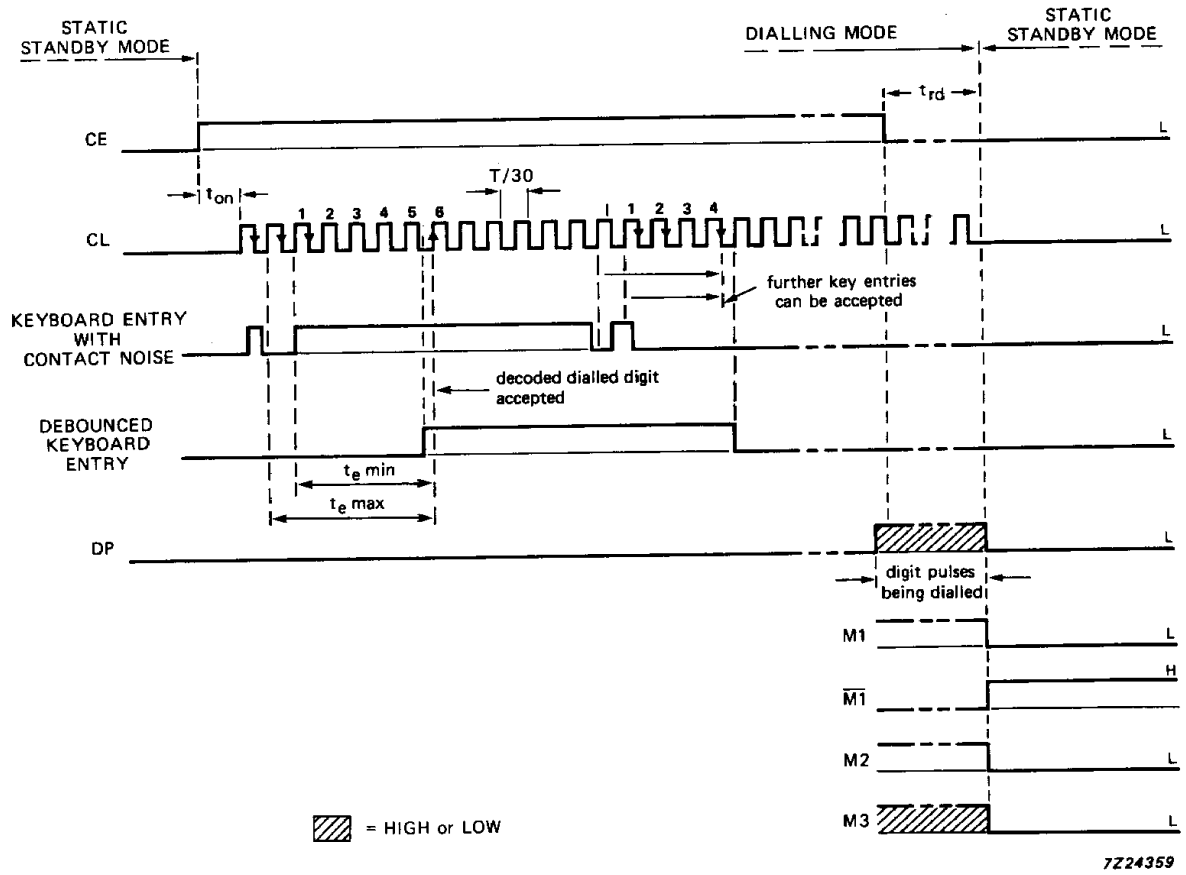


Fig.6 Timing diagram showing clock start-up, keyboard entry debouncing and the effect of interrupting the supply to CE during the transmission of dialling pulses.

N.B.: CL is an internal signal.

Dialling sequence

The dialling sequence can be initiated under either of the following two conditions:

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts (power supply before keyboard entry); see Fig. 7.

Ten clock pulse periods (t_d) after CE goes HIGH, a prepulse with a duration of ten clock pulse periods (t_d) appears at output M1. This prepulse ensures that, if a polarized muting relay with two stable positions is used, it switches to the de-muted position so that the circuit is then in the conversation mode whilst the subscriber awaits the dialling tone. When the first digit of the required number is entered at the keyboard, data entry period t_e commences.

- The supply to the integrated circuit is derived from the telephone lines via the cradle contacts in series with a common keyboard contact (Fig. 8).

When the first digit of the required number is entered at the keyboard, the common keyboard contact connects the line voltage to V_{DD} and CE becomes HIGH. After CE goes HIGH, the clock pulse generator starts and data entry period t_e commences. After period t_e, M1 goes HIGH and the push-button can be released. The supply to V_{DD} and CE is then maintained via the muting circuit controlled by M1.

The further dialling sequence will be described with the aid of Fig. 7. When the keyboard entry has been decoded and written into the RAM, M1 goes HIGH to mute the telephone and an inter-digit pause (t_{id}) ensues. M2 then goes HIGH (M2 is an internally generated signal, used for explanation only), the RAC addresses the RAM and the first keycode is loaded into the register of the output counter which generates the appropriate number of correctly-timed dialling pulses at output DP. When the digit has been pulsed out, M2 goes LOW, the RAC is incremented by one and the procedure repeats until the WAC and RAC contents are equal (all digits pulsed out). Output M1 then goes LOW, the circuit assumes the conversation mode. The circuit reverts to the static standby mode if CE goes LOW for more than the reset delay time (t_{rd} = 1,6 dialling pulse periods) at any time during the conversation or dialling mode (e.g. because the handset is replaced). CE remains LOW although V_{DD} is maintained by a back-up supply (e.g. because an external diode isolates CE from the back-up supply connected to V_{DD}). The RAM retains its contents for subsequent automatic redialling as long as the back-up supply maintains V_{DD} above V_{DDO} = 1,5 V.

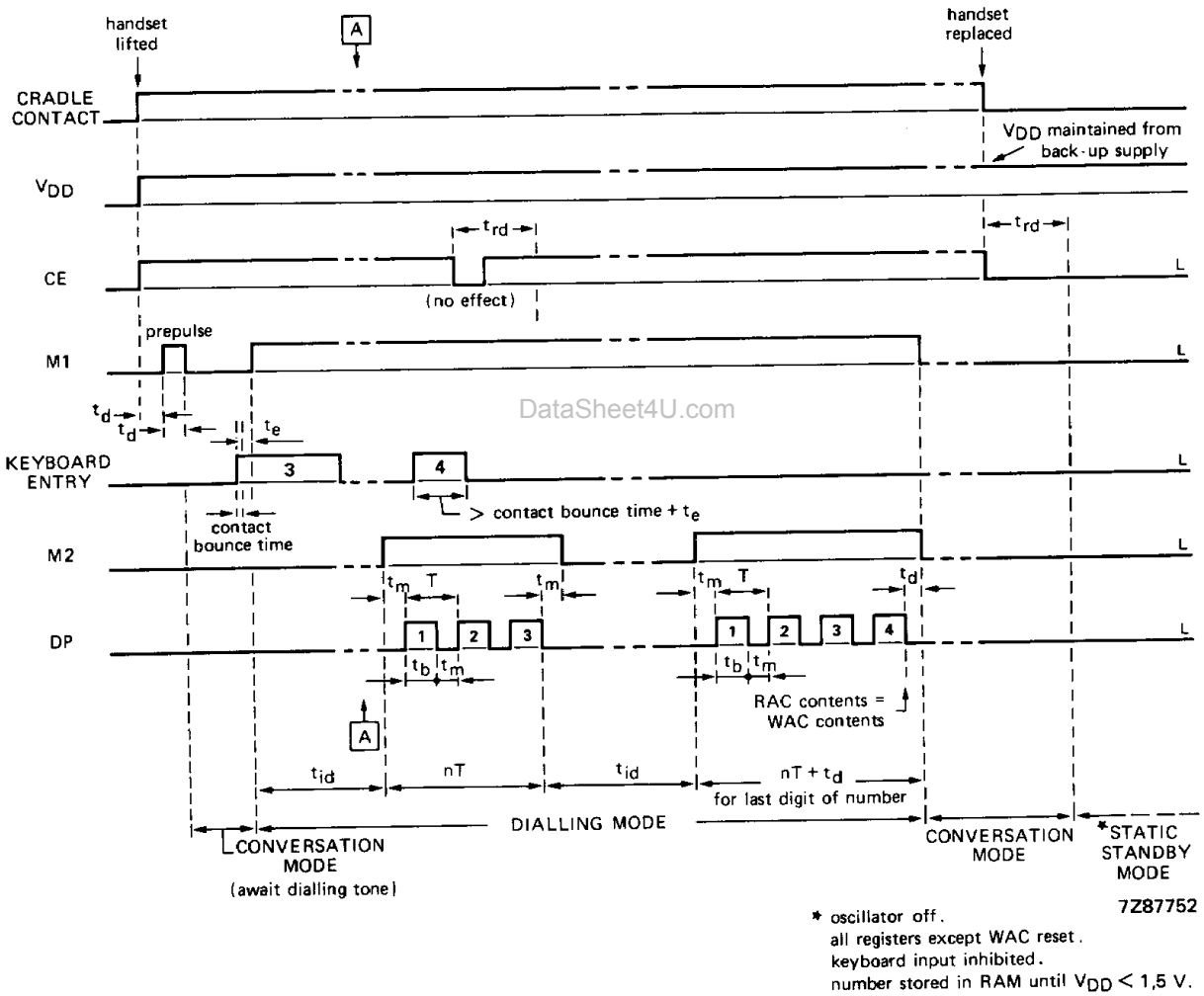


Fig. 7 Timing diagram of dialling sequence with V_{DD} and CE HIGH before keyboard entry (e.g. supply via the cradle contacts). M2 is an internal signal.

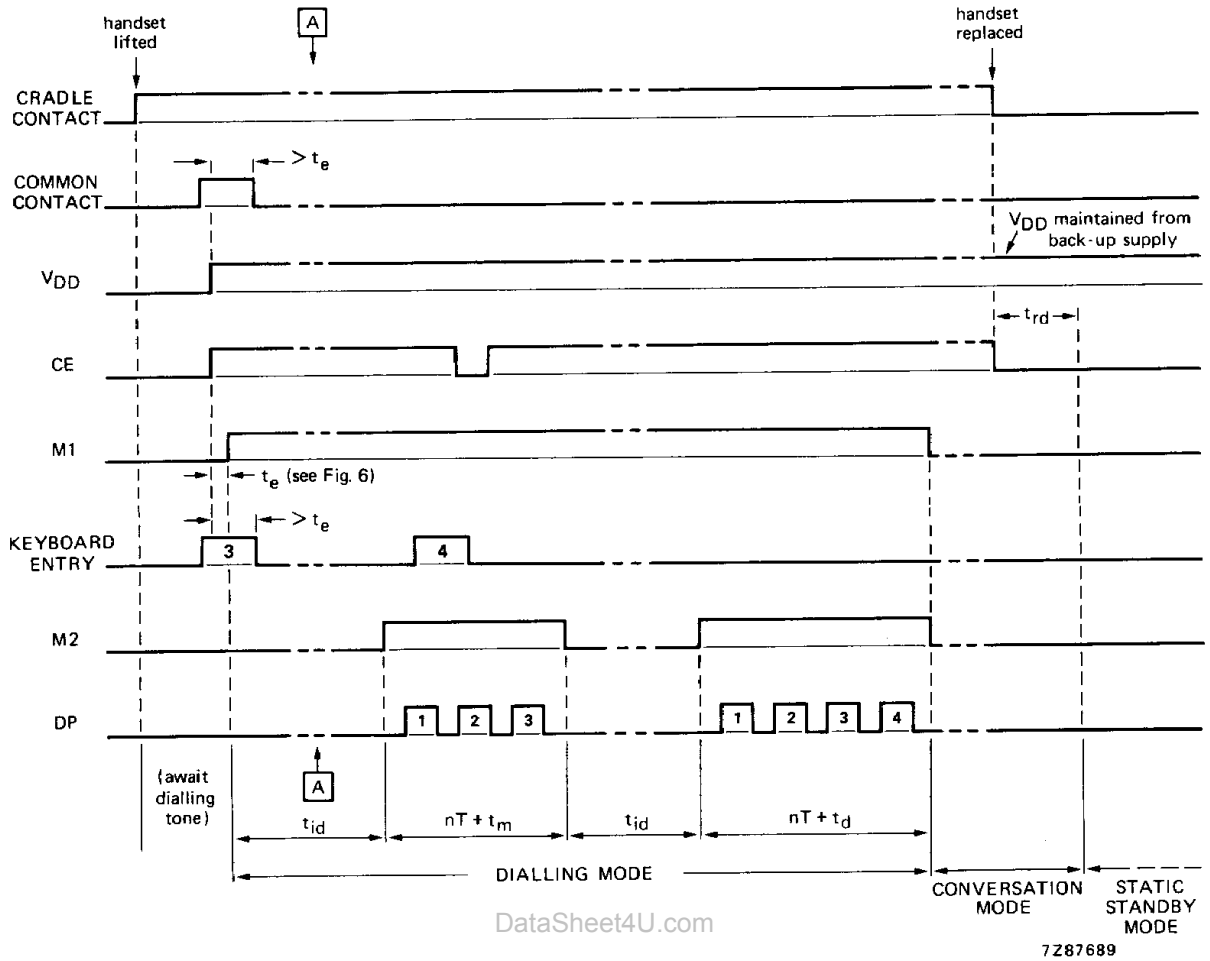


Fig. 8 Timing diagram for initiating the dialling mode with V_{DD} and CE initially supplied via the cradle contacts in series with a common contact on the keyboard. See Fig. 7 for pulse timings after point A. M2 is an internal signal.

Hold function

As shown in Fig. 9, the hold function allows the interval between consecutive pulsed digits to be prolonged under the control of external equipment. When the HOLD/APO is set HIGH, the dialling pulse-train is interrupted as soon as M2 goes LOW to signal that the current digit has been pulsed out. In the hold condition, further keyboard entries will be accepted, debounced, decoded and stored in that RAM. No further keycodes will be read from the RAM and converted into dialling pulses on DP until the HOLD/APO is set LOW again and an inter-digit pause has elapsed.

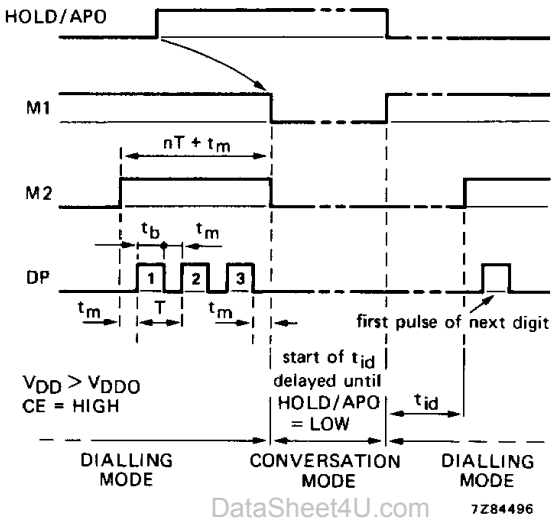


Fig. 9 Timing diagram showing the effect of activating the HOLD/APO during the transmission of dialling pulses. M2 is an internal signal.

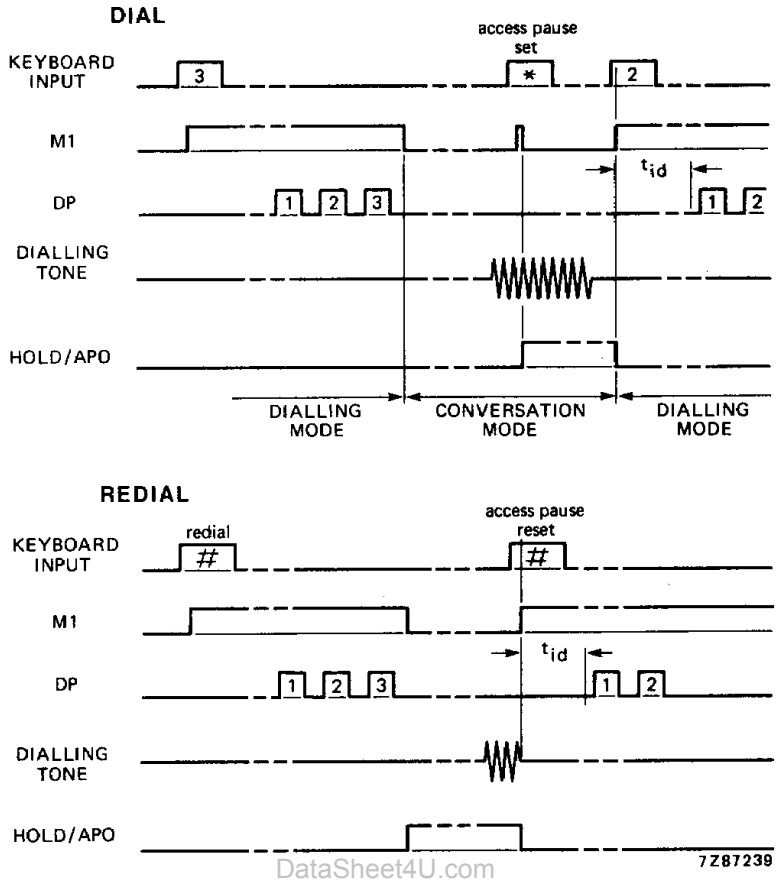


Fig. 10 Dialling sequence showing how an access pause code is stored in the RAM (DIAL) and how the access pause code is reset during the REDIAL.

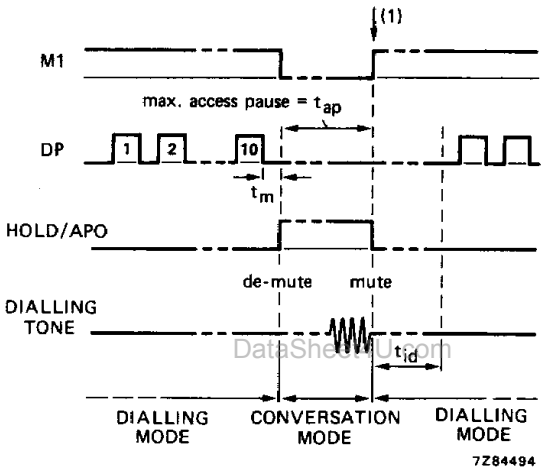
Note: access pause can be reset by pressing any key.

Access pause regeneration during redial

During original entry, access pause codes can be stored at the appropriate positions in the RAM. During redial the Access Pause Output (HOLD/APO) will go HIGH as soon as an access pause code is read from the RAM, thereby interrupting dialling until HOLD/APO is made LOW again as described above. In this way the normal inter-digit pause with a duration t_{id} can be replaced by a proper access pause. An access pause code is stored in the RAM during original entry by pressing the access pause key (*) between entering the trunk exchange code and the subscriber code, or at any other moment an access pause is required. The number of access pauses that can be inserted in this manner is only limited by the capacity of the RAM (digits + access pauses $\leqslant$ 23).

During redial, access pauses will be automatically regenerated.
Two methods of terminating an access pause:

1. Manually, by pressing the redial key (#)
2. With an external tone recogniser, by forcing HOLD/APO to LOW.



(1) a. Access pause reset by pressing redial key (#).
b. HOLD/APO controlled by tone recogniser:
HOLD/APO forced to LOW.

Fig. 11 Timing diagram showing Access Pause Reset, during redial.

Note: access pause can be reset by pressing any key.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to 8 V
Voltage on any pin	V_I	V_{SS} −0,3 to V_{DD} + 0,3 V
Operating ambient temperature range	T_{amb}	−25 to +70 °C
Storage temperature range	T_{stg}	−55 to +125 °C

CHARACTERISTICS

V_{DD} = 3 V; V_{SS} = 0 V; f_{osc} = 13,8 kHz (R1, R2 and C see Fig. 5); T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit	conditions
Operating supply voltage	V_{DD}	2,0	3	6	V	T_{amb} = −25 to +70 °C
Standby supply voltage (note 1)	V_{DDO}	1,5	–	6	V	T_{amb} = −25 to +70 °C
Operating supply current	I_{DD}	–	20	40	μA	CE = V_{DD}; note 2
	I_{DD}	–	75	150	μA	CE = V_{DD}; V_{DD} = 6 V; note 2
Standby supply current	I_{DDO}	–	0,65	2,0	μA	CE = V_{SS}; note 2
Input voltage LOW	V_{IL}	–	–	0,3 V_{DD}		1,8 V ⩽ V_{DD} ⩽ 6 V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	–		1,8 V ⩽ V_{DD} ⩽ 6 V
Input leakage current; CE LOW	$-I_{IL}$	–	–	50	nA	CE = V_{SS}
HIGH	I_{IH}	–	–	50	nA	CE = V_{DD}
Pull-up input current M/S	$-I_{IL}$	30	100	300	nA	V_I = V_{SS}
Pull-down input current F02	I_{IH}	30	100	300	nA	V_I = V_{DD}
Matrix keyboard operation						
Keyboard current	I_K	–	30	–	μA	X connected to Y, CE = V_{DD}
Keyboard 'ON' resistance	R_{KON}	–	–	2	kΩ	contact ON; note 3
Keyboard 'OFF' resistance	R_{KOFF}	1	–	–	MΩ	contact OFF; note 3
Outputs R1 to R4						
sink current	I_{OL}	–	3	–	μA	V_{OL} = 0,5 V
source current	$-I_{OH}$	–	40	–	μA	V_{OH} = 2,5 V

Notes

1. V_{DDO} = 1,5 V only for redial.
2. All other inputs and outputs open.
3. Guarantees correct keyboard operation.

parameter	symbol	min.	typ.	max.	unit	conditions
Outputs M1, DP						
sink current	I_{OL}	0,7	2,0	4,0	mA	V_{OL} = 0,5 V
source current	$-I_{OH}$	0,65	1,8	3,6	mA	V_{OH} = 2,5 V
Latch output HOLD/APO						
source current	$-I_{OH}$	0,7	2,0	4,0	mA	V_{OH} = 2,5 V

TIMING DATA

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; f_{osc} = 13,8 kHz

input levels of F02 (V_{SS} = LOW; V_{DD} = HIGH)		V_{F02}	LOW	HIGH		conditions (note 3)
		symbol			unit	
Dialling pulse frequency	$1/T_{DP}$	f_{DP}	10	19,2	Hz	
Dialling pulse period	$1/f_{DP}$	T_{DP}	100	52,2	ms	
Clock pulse frequency	$30 \times f_{DP}$	f_{CL}	300	575	Hz	
Break time (note 1)	$3/5 \times T_{DP}$	t_b	60	31,3	ms	M/S = H; n.c.
Make time (note 1)	$2/5 \times T_{DP}$	t_m	40	20,9	ms	M/S = H; n.c.
Break time (note 2)	$2/3 \times T_{DP}$	t_b	66,6	34,8	ms	M/S = L
Make time (note 2)	$1/3 \times T_{DP}$	t_m	33,3	17,4	ms	M/S = L
Inter-digit pause	$8 \times T_{DP}$	t_{id}	800	417	ms	
Reset delay time	$1,6 \times T_{DP}$	t_{rd}	160	83,5	ms	
Prepulse duration	$1/3 \times T_{DP}$	t_d	33,3	17,4	ms	
Debounce time						
min.	$5/30 \times T_{DP}$	$t_{e\ min}$	16,66	8,7	ms	
max.	$6/30 \times T_{DP}$	$t_{e\ max}$	20,0	10,44	ms	

parameter	symbol	min.	typ.	max.	unit	conditions
Frequency stability for f_{DP} = 10 Hz						see Fig. 12
V_{DD} = 2 to 6 V	Δf_{DP}	–	0,52	–	Hz	T_{amb} = 25 °C
V_{DD} = 3 V	Δf_{DP}	–	–0,144	–	Hz	T_{amb} = –40 to +85 °C

Notes

1. Mark-to-space ratio: 3:2.
2. Mark-to-space ratio: 2:1.
3. In the n.c. (not connected) condition, the input is drawn to the appropriate state by the internal pull-up/pull-down current.

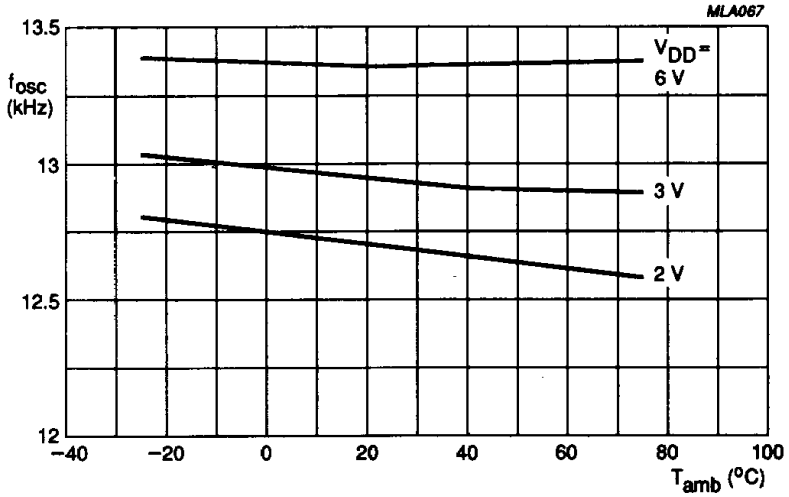


Fig. 12 RC oscillator frequency as a function of ambient temperature (T_{amb}) and supply voltage (V_{DD}).

Table 1 Dialling pulse frequency variation (T_{amb} = −40 to + 85 °C)

V_{DD} (V)	Δf_{DP} (Hz)
6,0	−0,007
3,0	−0,144
2,0	−0,217

Maximum frequency variation (Δf_{DP}):

$\Delta f_{DP} = f_{DP}$ (6 V, −40 °C) − f_{DP} (2 V, + 85 °C) = 0,637 Hz.