OM1400T-125

Preliminary Data Sheet

14-Bit Analog-to-Digital Converter Module with Turbolinear™ Technology

Description

The OM1400T-125 is a high-speed and high performance analog-to-digital converter module optimized to achieve an exceptionally high linearity when digitizing signals at very high IF. The module has a sampling rate of 125 MSPS and is primarily built around Optichron's Linearizer with Turbolinear™ technology in addition to the 14-bit ADS5500 analog-to-digital converter, and the AH22S buffer amplifier which provides a buffered, single-ended, 50-ohm input. The module output is a digitized signal with up to 25 dB improvement in SFDR when sub-sampling signals in the 2nd, 3rd, and 4th Nyquist zones.

The OM1400T-125 is targeted at a wide variety of applications requiring high linearity.

Features

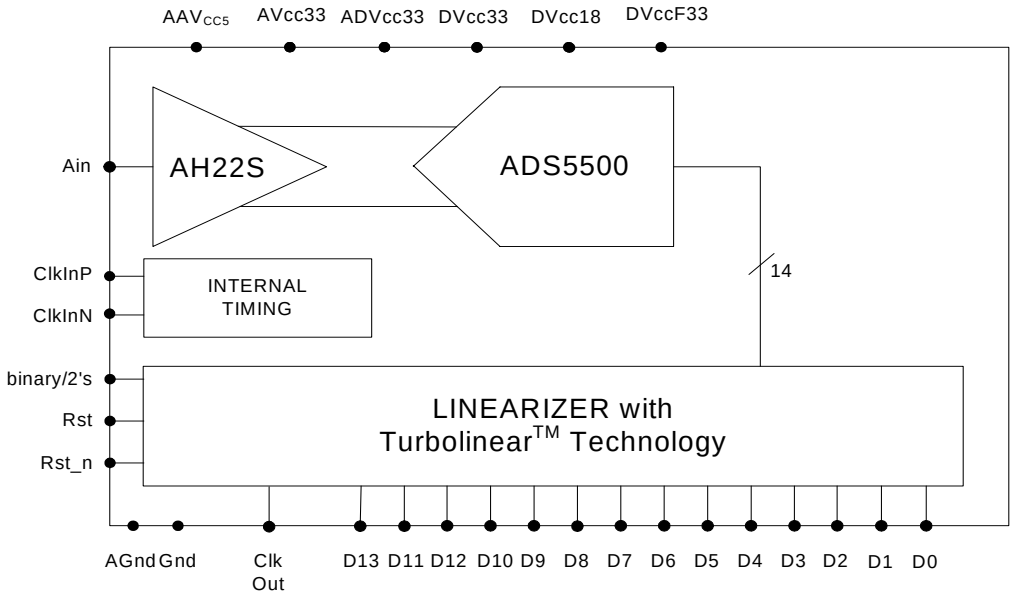
- 14-bit resolution, 125 MSPS sampling rate
- IF sampling to 244 MHz
- SFDR: 90 dBc typical for one-tone 130-180 MHz f_{IN} measured at –1 dBFS peak amplitude
- SNR: 71 dBFS typical for one-tone 130-180 MHz f_{IN} measured at –1 dBFS peak amplitude
- -2dBm full scale input power
- Single-ended, 50-Ohm analog input buffer
- Selectable 2s complement or binary outputs
- 3.3V CMOS compatible
- Output clock for data output latching
- Power dissipation: 3.2W

Applications

- Multi-channel, multi-mode receivers
- Base station infrastructure
- Communications instrumentation
- Test and measurement
- Radar, infrared imaging
- High-resolution medical imaging
- Power amplifier linearization

PRELIMINARY

Module Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings are over operating free-air temperature range unless otherwise noted.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Units
Electrical			
Analog Input Voltage		6	V
Digital Core Voltage		2	V
Digital I/O		3.6	V
Digital Output Current		30	mA
Analog Core Voltage		6	V
Environmental			
Junction Temperature		+125	°C
Operating Temperature Range	-40	+85	°C
Storage Temperature Range	-50	+150	°C

Caution: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only; functional operation of the device at these or other conditions beyond those in the operational section of this specification is not implied.

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degree of functionality.

DC Specifications

(Typical, min, max values at T = 25°C, AAV_{CC5} = 5V, AV_{CC33}= ADV_{CC33} = DV_{CC33} = DV_{CCF33} = 3.3V, DV_{CC18} = 1.8V; sampling rate = 125 MSPS with 50% clock duty cycle unless otherwise noted.)

Table 2: DC Specifications

Parameter	Notes	Min	Typical	Max	Units
Resolution			14		Bits
Accuracy					
No Missing Codes			Guaranteed		
Offset Error		TBD	TBD	TBD	mV
Offset Error Drift			TBD		ppm/°C
Gain Error		TBD	TBD	TBD	% FS
Gain Error Drift			TBD		ppm/°C
Power Supply Rejection Ratio			TBD		1 mv/V
Analog Input					
Input Voltage Range Fullscale			1.0		Vp-p
Input Return Loss			16		dB
Analog 5.0 V Supply Voltage	AAV_{CC5}	4.75	5.00	5.25	V
Analog Supply Current					
	AAV_{CC5} Supply		320	380	mA
Digital 3.3V Supply Voltage	DV_{CC33},DV_{CCF33}	3.00	3.3	3.60	V
Digital 3.3V Supply Current	Total		32	63	mA
Turbolinear I/O	DV_{CC33} Supply		32	45	mA
Flash Read	DV_{CCF33} Supply		14	18	mA
Flash Quiesent	DV_{CCF33} Supply		0.025	0.05	mA
ADC 3.3 V Supply Voltage	ADV_{CC33}	3.0	3.3	3.6	V
ADC I/O Digital 3.3 V Supply Current	ADV_{CC33}		61	75	mA
ADC Analog 3.3 V Supply Current	AV_{CC33}		175	190	mA
Digital 1.8V Supply Voltage	DV_{CC18}	1.72	1.80	1.88	V
Digital 1.8V Supply Current			390	TBD	mA
Module					
Power Dissipation			3.2		W
Digital Core Power				700	mW

Digital Specifications

(AAV_{CC5} = 5V, AV_{CC33}= ADV_{CC33} = DV_{CC33} = DV_{CCF33} = 3.3V, DV_{CC18} = 1.8V; TMIN and TMAX at rated speed grade unless otherwise noted.)

Table 3: Digital Specifications

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
Logic Inputs					
Logic 1 Voltage		2.2		3.6	V
Logic 0 Voltage		0.0		1.0	V
Logic Outputs					V
Logic Compatibility			CMOS		
Logic 1 Voltage (DV_{CC} = 3.3V)		2.7		3.6	V
Logic 0 Voltage (DV_{CC} = 3.3V)		0.0		0.5	V

Switching Specifications

(AAV_{CC5} = 5V, $DV_{CC}33$ = ADVcc33 = AVcc33 = DVccF33 = 3.3V, DV_{CC18} = 1.8V; CLOAD 10 pF)

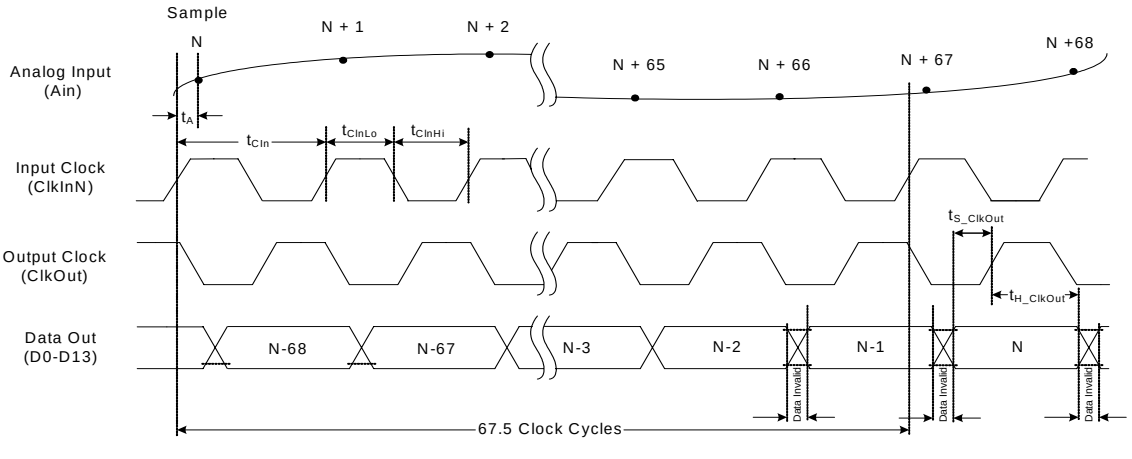
Table 4: Switching Specification

Parameter (Conditions)	Name	Minimum	Typical	Maximum	Units
Conversion Rate [a]					MSPS
OM1400T-1250NZx		120		125	
OM1400T-1200NZx		115		120	
OM1400T-1150NZx		110		115	
OM1400T-1100NZx		105		110	
ClkInP, ClkInN Inputs					
Differential Input Voltage		0.4			Vp-p
Differential Input Resistance			10		kΩ (kOhm)
Differential Input Capacitance			2.5		pF
ClkInP, ClkInN Input Parameters					
Clock Period	t_{CIN}		8.0		ns
Clock Pulsewidth High	t_{CINHI}		4.0		ns
Clock Pulsewidth Low	t_{CINLO}		4.0		ns
50% duty cycle for optimum performance					
ClkOut/DATA (D13:0)					
ClkOut Rising to DATA (Hold Time)	t_{H_CLKOUT}	2.0			ns
ClkOut Rising to DATA (Setup Time)	t_{S_CLKOUT}	2.0			ns
Latency			67.5		Clock cycles
Aperture Delay t_A			1.0		ns
Aperture Jitter			0.3		pS rms

a. The ‘x’ in NZx refers to the Nyquist zone versions 2, 3, or 4 of the product. Each part number is calibrated at the maximum listed specification where the best performance is obtained. It is highly recommended that the module is operated at that rate. For a complete part number listing, see Ordering Guide on page 21.

Timing Diagram

Figure 1. Timing Diagram



AC Specifications

Table 5: Nyquist Zone 2 (62.5-125 MHz, Temp = 25°C, fs = 125 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNRFS (one-tone input at -1 dBFS)					
f_{IN} = fmin + 5%fs			72		dB
f_{IN} = (fmax + fmin)/2			72		dB
f_{IN} = fmax – 5%fs			72		dB
SINAD (input at -1 dBFS)					
f_{IN} = fmin + 5%fs			TBD		dB
f_{IN} = (fmax + fmin)/2			TBD		dB
f_{IN} = fmax – 5%fs			TBD		dB
THD					
f_{IN} = fmin + 5%fs		TBD	TBD		dB
f_{IN} = (fmax + fmin)/2		TBD	TBD		dB
f_{IN} = fmax – 5%fs		TBD	TBD		dB
SFDR (one-tone input at -1 dBFS)					
f_{IN} = fmin + 5%fs		TBD	90		dBc
f_{IN} = (fmax + fmin)/2		TBD	90		dBc
f_{IN} = fmax – 5%fs		TBD	90		dBc
Two Tone IMD (F1, F2 at -7 dBFS)					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz		TBD	TBD		dBFS
Analog Input Bandwidth			450		MHz

Note: 'fs' is the sampling rate.
fmax=fs
fmin=fs/2

Table 6: Nyquist Zone 3 (125-187.5 MHz, Temp = 25°C, fs = 125 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNRFS (one-tone input at -1 dBFS)					
f_{IN} = fmin + 5%fs			71		dB
f_{IN} = (fmax + fmin)/2			71		dB
f_{IN} = fmax – 5%fs			71		dB
SINAD (input at -1 dBFS)					
f_{IN} = fmin + 5%fs			TBD		dB
f_{IN} = (fmax + fmin)/2			TBD		dB
f_{IN} = fmax – 5%fs			TBD		dB
THD					
f_{IN} = fmin + 5%fs		TBD	TBD		dB
f_{IN} = (fmax + fmin)/2		TBD	TBD		dB
f_{IN} = fmax – 5%fs		TBD	TBD		dB
SFDR (one-tone input at -1 dBFS)					
f_{IN} = fmin + 5%fs		TBD	90		dBc
f_{IN} = (fmax + fmin)/2		TBD	90		dBc
f_{IN} = fmax – 5%fs		TBD	90		dBc
Two Tone IMD (F1, F2 at -7 dBFS)					
f_{IN} = {(fmax + fmin)/2} – 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz		TBD	TBD		dBFS
Analog Input Bandwidth			450		MHz

Note: 'fs' is the sampling rate.
fmax=3fs/2
fmin=fs

Table 7: Nyquist Zone 4 (187.5-250 MHz, Temp = 25°C, fs = 125 MSPS)

Parameter (Conditions)	Notes	Minimum	Typical	Maximum	Units
SNRFS (one-tone input at −1 dBFS)					
f_{IN} = fmin + 5%fs			70		dB
f_{IN} = (fmax + fmin)/2			70		dB
f_{IN} = fmax – 5%fs			70		dB
SINAD (input at −1 dBFS)					
f_{IN} = fmin + 5%fs			TBD		dB
f_{IN} = (fmax + fmin)/2			TBD		dB
f_{IN} = fmax – 5%fs			TBD		dB
THD					
f_{IN} = fmin + 5%fs		TBD	TBD		dB
f_{IN} = (fmax + fmin)/2		TBD	TBD		dB
f_{IN} = fmax – 5%fs		TBD	TBD		dB
SFDR (one-tone input at −1 dBFS)					
f_{IN} = fmin + 5%fs		TBD	90		dBc
f_{IN} = (fmax + fmin)/2		TBD	90		dBc
f_{IN} = fmax – 5%fs		TBD	90		dBc
Two Tone IMD (F1, F2 at −7 dBFS)					
f_{IN} = {(fmax + fmin)/2} - 4.9 MHz {(fmax + fmin)/2} + 6.1 MHz		TBD	TBD		dBFS
Analog Input Bandwidth			450		MHz

Note: ‘fs’ is the sampling rate.
fmax=2fs
fmin=3fs/2

Typical Performance Characteristics (Nyquist Zone 3)

Figure 2. Single Tone (177.95 MHz) before Linearization SFDR 71.36dB (typical)

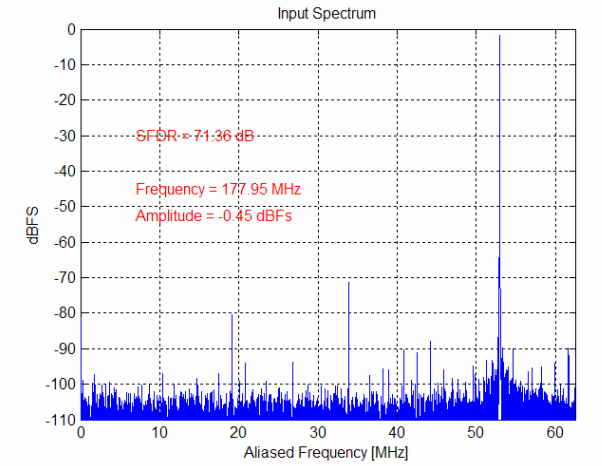


Figure 3. TwoTone (133.09, 151.50MHz) before Linearization SFDR 82.52dB (typical)

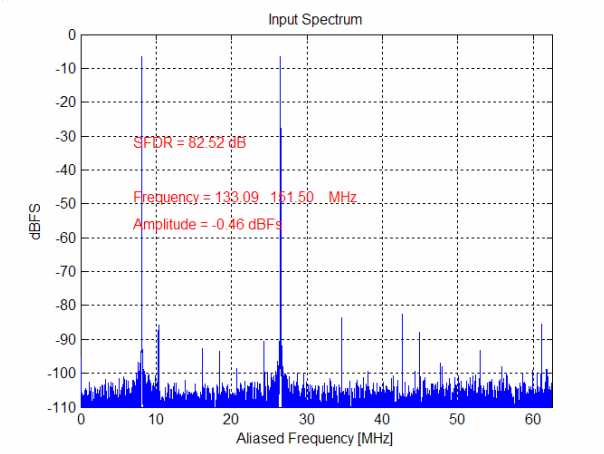


Figure 4. Three Tones (134.09, 147.77, 167.22MHz) before Linearization SFDR 89.60dB (typical)

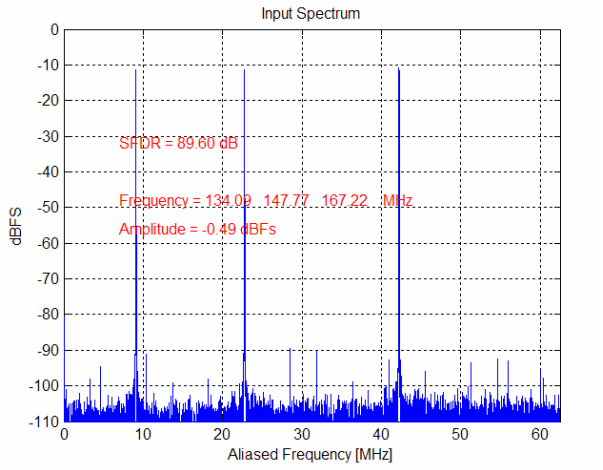


Figure 5. Single Tone (177.95MHz) after Linearization SFDR 90.00dB (typical)

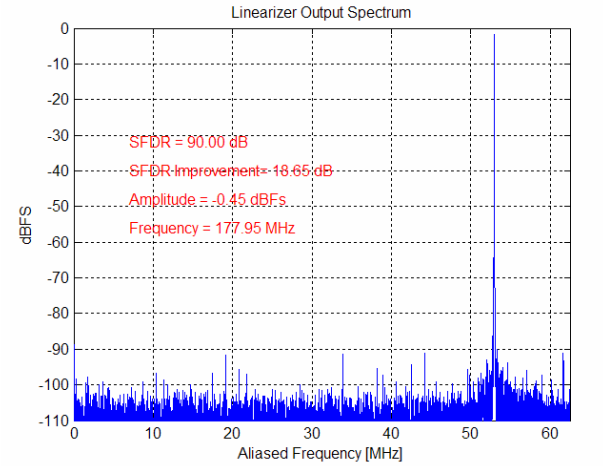


Figure 6. Two Tones (133.09, 151.50MHz) after Linearization SFDR 94.03dB (typical)

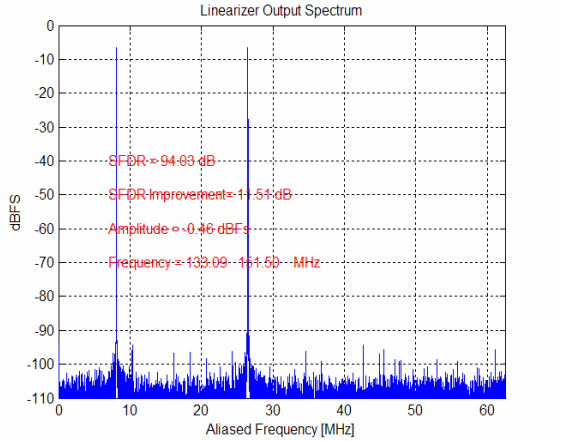
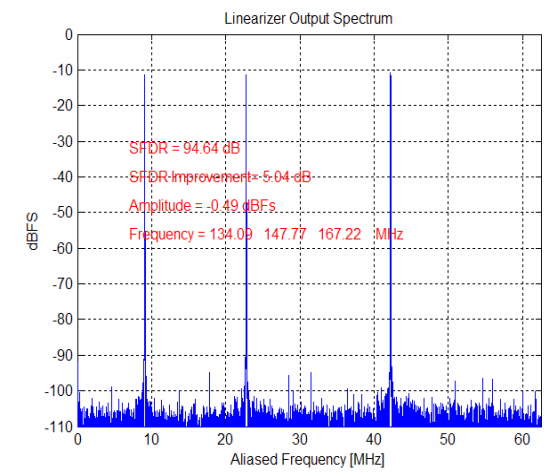


Figure 7. Three Tones (134.09, 147.77, 167.22MHz) after Linearization SFDR 94.64dB (typical)



Definition of Specifications

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay in time between the falling edge of the input sampling clock and the actual time at which sampling occurs.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Differential Input Voltage

The peak-to-peak differential voltage that must be applied to generate a full scale response. The peak differential voltage is calculated by measuring the voltage on one input pin and subtracting the voltage on the other input pin which is 180^{o} out of phase. The peak to peak value is then calculated by obtaining the voltages of the input pins with the phases reverses and calculating the difference between the peak measurements.

Differential Non-linearity (DNL)

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

An indication of the quality of an analog-to-digital converter. ENOB can be calculated with the following formula:

Equation 1. $$\text{ENOB} = \frac{\text{SINAD-1.76}}{6.02}$$

Gain error

The amount of deviation between the ideal transfer function and the measured transfer function (with the offset error removed) when a full scale analog input is applied, resulting in all 1s in the digital code. Gain error is measured in LSBs or as a percentage of the full scale range (%FSR).

Integral Non-linearity (INL)

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a linear least squares curves fit.

Maximum Conversion Rate

The clock rate at which parametric testing is performed.

Minimum Conversion Rate

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Nyquist Zone

The product performance is specified for input frequencies in three Nyquist zones. Typical performance is delivered over the middle 80% of each Nyquist zone.

Nyquist Zone 2: $f_{s/2}$ - f_s

Nyquist Zone 3: f_s - $3f_{s/2}$

Nyquist Zone 4: $3f_{s/2}$ - $2f_s$

Offset Error

Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Power Supply Rejection

The change in full scale from the value with the supply at the minimum limit to the value with the supply at the maximum limit measured at the mid-band frequency of the Nyquist zone under test.

Propagation Delay

The delay between the input clock rising edge and the time when all data bits are within valid logic levels.

Signal-to-Noise and Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (Without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic.

Total Harmonic Distortion (THD)

The ratio of the rms signal amplitude of the input to the rms value of distortion appearing at multiples (harmonics) of the input.

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third order inter modulation product; reported in dBc.

Temperature Drift

As measured for offset or gain error, it specifies the maximum change from the initial temperature value to the value at T_{Min} or T_{Max}.

Applications Information

Clock input

The clock input signal must be of high quality and therefore a low jitter, low phase noise source is required to ensure optimal performance. Additionally, in order to keep the accuracy of the 14-bit conversion, the clock inputs need to be driven differentially and the input signal needs to be AC coupled to the ClkInN and ClkInP clock inputs. For a single-ended sinusoidal reference signal, the conversion to differential signals can be done with a transformer like the ADT4-1WT.

Figure 8 shows a typical circuit where single-ended to differential transformation of the clock is done using an RF transformer. For best performance, the single-ended sinusoid should have a signal power of at least 13 dBm for best performance. Narrow band-pass filtering of this sinusoid will help reduce the jitter on this reference. The Schottky diodes across the secondary of the transformer limits the noise into the clock input pins and limits the voltage swing at the rails. It is important that the differential clock signal lines are placed close together and isolated from other analog inputs and digital outputs. Alternately, a low-jitter differential ECL/PECL clock signal may be AC coupled with series capacitors to the ClkInP and ClkInN inputs. This is the circuit used on the OM1400T-125 Evaluation Board.

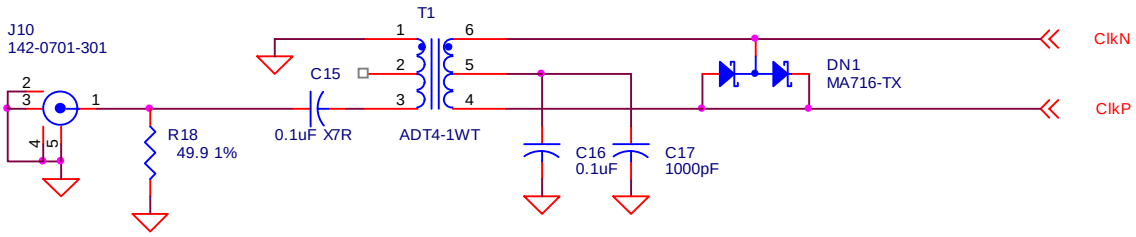
Analog Input

The module provides a 50-Ohm AC input impedance, therefore the user needs to provide a single-ended analog import source capable of driving 50 Ohms at -2dBm to achieve full-scale.

Supplies and Bypassing

Linear power supplies should be used for best performance. However, if switching power supplies are used they need to be appropriately shielded and filtered to avoid introducing spurious signals into the ADC. The ADVcc33 supply must be at least 0.4V by the time the AVcc33 supply reaches 3.0V. Should both power supplies not be turned on simultaneously, the ADC may stay in the power down mode. Decoupling capacitors need to be positioned as close to each power pin as possible to minimize high frequency supply noise by satisfying local current demands. 10%, 16V X7R 0603 0.1 uF and 20%,10V X7R 1206 10 uF capacitors are recommended for optimal results with the 0.1uF being the closest to the pin.

Figure 8. Single-Ended to Differential Clock Input



Grounding

To minimize the possibility of digital switching creating current coupling into analog ground, it is recommended a multi-layer board with a single ground plane be used. It is necessary to ensure that the digital and analog sections are kept physically separated. Digital traces should not be routed near or under unshielded analog lines. The pin-out of the module allows for easy implementation of the above recommendation. The ball rows 1-19 on the top side of the module are allocated to analog functions, power and ground while the ball rows from 20-39 on the bottom side are all allocated to digital functions, power and ground.

Input/Output

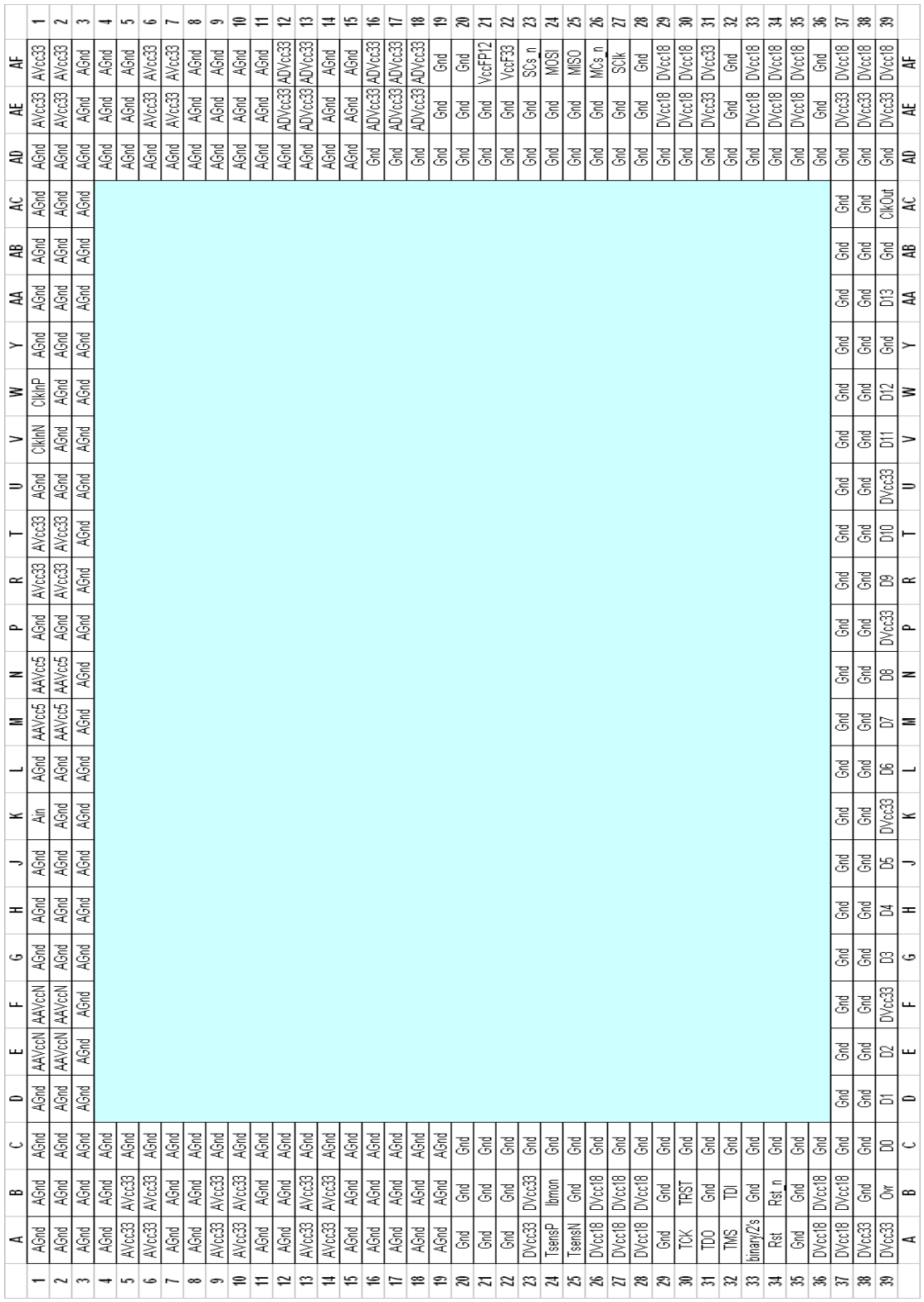
The module supports the industry standard SPI (Serial Peripheral Interface) for interfacing to external memory and/or logic. During the first 10 ms, after reset, the co-efficients are loaded and only after 10 ms does the module relinquish the bus master to external logic like an FPGA.

Support for JTAG is provided with the standard signals; TRST, TCK, TDO, TMS, TDI. While the JTAG coverage is only for the Linearizer, it does offer JTAG for the output data port, the binary/2s input and the ClkOut pins.

Digital Outputs

There are 13 data output pins that provide the digital output from the Linearizer. The format of that output (binary or 2s complement) is selected via the Binary/2s input. The port is a standard 8mA, 3.3V CMOS output. Therefore, the digital outputs should be routed to minimize capacitive loading and fanout (use only one gate on each output line). For instance, to maintain a 2ns edge, the total capacitance on a given output line should not exceed 5 pF. Digital output timing is maintained for loads up to 10 pF provided the capacitive loading on data and clock lines are well matched. External series resistors on the output lines are included inside the module and are not required on the board on which the module attaches.

Pin Configuration Top View



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	AGnd	AGnd	AGnd	AGnd	AAVccN	AAVccN	AGnd	AGnd	AGnd	Ain	AGnd	AAVcc5	AAVcc5	AGnd	AVcc33	AVcc33	AGnd	ClkInN	ClkInP	AGnd	AGnd	AGnd	AGnd	AGnd	AVcc33	AVcc33	1
2	AGnd	AGnd	AGnd	AGnd	AAVccN	AAVccN	AGnd	AGnd	AGnd	AGnd	AGnd	AAVcc5	AAVcc5	AGnd	AVcc33	AVcc33	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AVcc33	AVcc33	2
3	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	AGnd	3
4	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	4
5	AVcc33	AVcc33	AGnd																					AGnd	AGnd	AGnd	5
6	AVcc33	AVcc33	AGnd																					AGnd	AVcc33	AVcc33	6
7	AGnd	AGnd	AGnd																					AGnd	AVcc33	AVcc33	7
8	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	8
9	AVcc33	AVcc33	AGnd																					AGnd	AGnd	AGnd	9
10	AVcc33	AVcc33	AGnd																					AGnd	AGnd	AGnd	10
11	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	11
12	AGnd	AGnd	AGnd																					ADVcc33	ADVcc33	ADVcc33	12
13	AVcc33	AVcc33	AGnd																					ADVcc33	ADVcc33	ADVcc33	13
14	AVcc33	AVcc33	AGnd																					AGnd	AGnd	AGnd	14
15	AGnd	AGnd	AGnd																					AGnd	AGnd	AGnd	15
16	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	16
17	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	17
18	AGnd	AGnd	AGnd																					Gnd	ADVcc33	ADVcc33	18
19	AGnd	AGnd	AGnd																					Gnd	Gnd	Gnd	19
20	Gnd	Gnd	Gnd																					Gnd	Gnd	Gnd	20
21	Gnd	Gnd	Gnd																					Gnd	Gnd	VccFP12	21
22	Gnd	Gnd	Gnd																					Gnd	Gnd	VccF33	22
23	DVcc33	DVcc33	Gnd																					Gnd	Gnd	SCs_n	23
24	TsensP	Ibmon	Gnd																					Gnd	Gnd	MOSI	24
25	TsensN	Gnd	Gnd																					Gnd	Gnd	MISO	25
26	DVcc18	DVcc18	Gnd																					Gnd	Gnd	MCs_n	26
27	DVcc18	DVcc18	Gnd																					Gnd	Gnd	SClk	27
28	DVcc18	DVcc18	Gnd																					Gnd	Gnd	Gnd	28
29	Gnd	Gnd	Gnd																					Gnd	DVcc18	DVcc18	29
30	TCK	TRST	Gnd																					Gnd	DVcc18	DVcc18	30
31	TDO	Gnd	Gnd																					Gnd	DVcc33	DVcc33	31
32	TMS	TDI	Gnd																					Gnd	Gnd	Gnd	32
33	binaryI2s	Gnd	Gnd																					Gnd	DVcc18	DVcc18	33
34	Rst	Rst_n	Gnd																					Gnd	DVcc18	DVcc18	34
35	Gnd	Gnd	Gnd																					Gnd	DVcc18	DVcc18	35
36	DVcc18	DVcc18	Gnd																					Gnd	Gnd	Gnd	36
37	DVcc18	DVcc18	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	DVcc33	DVcc18	37
38	DVcc33	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	DVcc33	DVcc18	38
39	DVcc33	Dvr	D0	D1	D2	DVcc33	D3	D4	D5	DVcc33	D6	D7	D8	DVcc33	D9	D10	DVcc33	D11	D12	Gnd	D13	Gnd	ClkOut	Gnd	DVcc33	DVcc18	39
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	

PRELIMINARY

Pin Assignments

Table 8: Pin Assignments by function

Function	Ball Number	Signal Name
Active High Reset	B34	RST
Active Low Reset	A34	RST_N
Amplifier Positive Supply Voltage	M1, M2, N1, N2	AAV_{CC5}
Amplifier Negative Supply Voltage (Linearized ADC Module standard family pinout; not required for the OM1400T-125)	E1, E2, F1, F2,	AAV_{CCN}
Analog Ground	A1-4, A7-8, A11-12, A15-19, B1-4, B7-8, B11-12, B15-19, C1-19, D1-3, E3, F3, G1-3, H1-3, J1-3, K2-3, L1-3, M3, N3, P1-3, R3, T3, U1-3, V2-3, W2-3, Y1-3, AA1-3, AB1-3, AC1-3, AD1-15, AE3-6, AE8-11, AE14-15, AF3-6, AF8-11, AF14-15	AGND
Analog Input Signal	K1	AIN
Clock Input Negative. Complement of ClkInP, Differential Input.	W1	CLKINN
Clock Input Positive. Conversion on rising edge.	V1	CLKINP
Clock Output of Linearizer	AC39	CLKOUT
Core Analog Supply for ADC	A5-6, A9-10, A13-14, B5-6, B9-10, B13-14, R1-2, T1-2, AE1-2, AE6-7, AF1-2, AF6-7	AV_{CC33}
Core Supply for Linearizer	A26-28, A36-37, B26-28, B36-37, AE29-30, AE33-35, AF29-30, AF33-35, AF37-39	DV_{CC18}
Data Output of Linearizer in 2s Complement if binary/2s is set.	C39, D39, E39, G39, H39, J39, L39, M39, N39, R39, T39, V39, W39, AA39	D(0-13)
Digital Ground	A20-22, A29, A35, B20-22, B29, B35, B38, C20-38, D37-38, E37-38, F37-38, G37-38, H37-38, J37-38, K37-38, L37-38, M37-38, N37-38, P37-38, R37-38, T37-38, U37-38, V37-38, W37-38, Y37-39, AA37-38, AB37-39, AC37-38, AD16-39, AF19-28, AF32, AF36	GND
Digital I/O Supply for ADC	AE12-13, AE16-18, AF12-13, AF16-18	ADV_{CC33}
Flash Memory Supply Voltage	AF22	V_{CCF33}
I/O Supply for Linearizer	A23, A38-39, B23, F39, K39, P39, U39, AE31, AE37-39, AF31	DV_{CC33}
JTAG	B30	TRST
JTAG	A30	TCK
JTAG	A31	TDO
JTAG	A32	TMS
JTAG	B32	TDI
No Connect	A24, A25, B24, E5, E35, AB5, AB35, AF21, AF23-27	NC
Set 2s Complement Output. Reset Binary Output.	A33	Binary/2s
Serial Peripheral Interface	AF23	SCS_N

Table 8: Pin Assignments by function (Continued)

Function	Ball Number	Signal Name
Serial Peripheral Interface	AF24	MOSI
Serial Peripheral Interface	AF25	MISO
Serial Peripheral Interface	AF26	MCS_N
Serial Peripheral Interface	AF27	SCLK

Table 9: Pin Assignments by Pin Number

Pin Number	Signal
A1	AGND
A2	AGND
A3	AGND
A4	AGND
A5	AVCC33
A6	AVcc33
A7	AGND
A8	AGND
A9	AVcc33
A10	AVcc33
A11	AGND
A12	AGND
A13	AVcc33
A14	AVcc33
A15	AGND
A16	AGND
A17	AGND
A18	AGND
A19	AGND
A20	GND
A21	GND
A22	GND
A23	DVCC33
A24	NC
A25	NC
A26	DVCC18
A27	DVCC18
A28	DVCC18

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
A29	GND
A30	TCK
A31	TDO
A32	TMS
A33	BINARY 2S
A34	RST
A35	GND
A36	DVCC18
A37	DVCC18
A38	DVCC33
A39	DVCC33
B1	AGND
B2	AGND
B3	AGND
B4	AGND
B5	AVcc33
B6	AVcc33
B7	AGND
B8	AGND
B9	AVcc33
B10	AVcc33
B11	AGND
B12	AGND
B13	AVcc33
B14	AVcc33
B15	AGND
B16	AGND
B17	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
B18	AGND
B19	AGND
B20	GND
B21	GND
B22	GND
B23	DVCC33
B24	NC
B25	GND
B26	DVCC18
B27	DVCC18
B281	DVCC18
B29	GND
B30	TRST
B31	GND
B32	TDI
B33	GND
B34	RST_N
B35	GND
B36	DVCC18
B37	DVCC18
B38	GND
B39	NC
C1	AGND
C2	AGND
C3	AGND
C4	AGND
C5	AGND
C6	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
C7	AGND
C8	AGND
C9	AGND
C10	AGND
C11	AGND
C12	AGND
C13	AGND
C14	AGND
C15	AGND
C16	AGND
C17	AGND
C18	AGND
C19	AGND
C20	GND
C21	GND
C22	GND
C23	GND
C24	GND
C25	GND
C26	GND
C27	GND
C28	GND
C29	GND
C30	GND
C31	GND
C32	GND
C33	GND
C34	GND
C35	GND
C36	GND
C37	GND
C38	GND
C39	D0
D1	AGND
D2	AGND
D3	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
D37	GND
D38	GND
D39	D1
E1	AAVCCN
E2	AAVCCN
E3	AGND
E37	GND
E38	GND
E39	D2
F1	AAVCCN
F2	AAVCCN
F3	AGND
F37	GND
F38	GND
F39	DVCC33
G1	AGND
G2	AGND
G3	AGND
G37	GND
G38	GND
G39	D3
H1	AGND
H2	AGND
H3	AGND
H37	GND
H38	GND
H39	D4
J1	AGND
J2	AGND
J3	AGND
J37	GND
J38	GND
J39	D5
K1	AIN
K2	AGND
K3	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
K37	GND
K38	GND
K39	DVCC33
L1	AGND
L2	AGND
L3	AGND
L37	GND
L38	GND
L39	D6
M1	AAVCC5
M2	AAVCC5
M3	AGND
M37	GND
M38	GND
M39	D7
N1	AAVCC5
N2	AAVCC5
N3	AGND
N37	GND
N38	GND
N39	D8
P1	AGND
P2	AGND
P3	AGND
P37	GND
P38	GND
P39	DVCC33
R1	AVcc33
R2	AVcc33
R3	AGND
R37	GND
R38	GND
R39	D9
T1	AVcc33
T2	AVcc33
T3	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
T37	GND
T38	GND
T39	D10
U1	AGND
U2	AGND
U3	AGND
U37	GND
U38	GND
U39	DVCC33
V1	CLKINN
V2	AVcc33
V3	AGND
V37	GND
V38	GND
V39	D11
W1	CLKINN
W2	AVcc33
W3	AGND
W37	GND
W38	GND
W39	D12
Y1	AGND
Y2	AGND
Y3	AGND
Y37	GND
Y38	GND
Y39	GND
AA1	AGND
AA2	AGND
AA3	AGND
AA37	GND
AA38	GND
AA39	D13
AB1	AGND
AB2	AGND
AB3	AGND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AB37	GND
AB38	GND
AB39	GND
AC1	AGND
AC2	AGND
AC3	AGND
AC37	GND
AC38	GND
AC39	CLKOUT
AD1	AGND
AD2	AGND
AD3	AGND
AD4	AGND
AD5	AGND
AD6	AGND
AD7	AGND
AD8	AGND
AD9	AGND
AD10	AGND
AD11	AGND
AD12	AGND
AD13	AGND
AD14	AGND
AD15	AGND
AD16	GND
AD17	GND
AD18	GND
AD19	GND
AD20	GND
AD21	GND
AD22	GND
AD23	GND
AD24	GND
AD25	GND
AD26	GND
AD27	GND

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AD28	GND
AD29	GND
AD30	GND
AD31	GND
AD32	GND
AD33	GND
AD34	GND
AD35	GND
AD36	GND
AD37	GND
AD38	GND
AD39	GND
AE1	AVcc33
AE2	AVcc33
AE3	AGND
AE4	AGND
AE5	AGND
AE6	AVcc33
AE7	AVcc33
AE8	AGND
AE9	AGND
AE10	AGND
AE11	AGND
AE12	ADVCC33
AE13	ADVCC33
AE14	AGND
AE15	AGND
AE16	ADVCC33
AE17	ADVCC33
AE18	ADVCC33
AE19	GND
AE20	GND
AE21	GND
AE22	GND
AE23	GND
AE24	GND

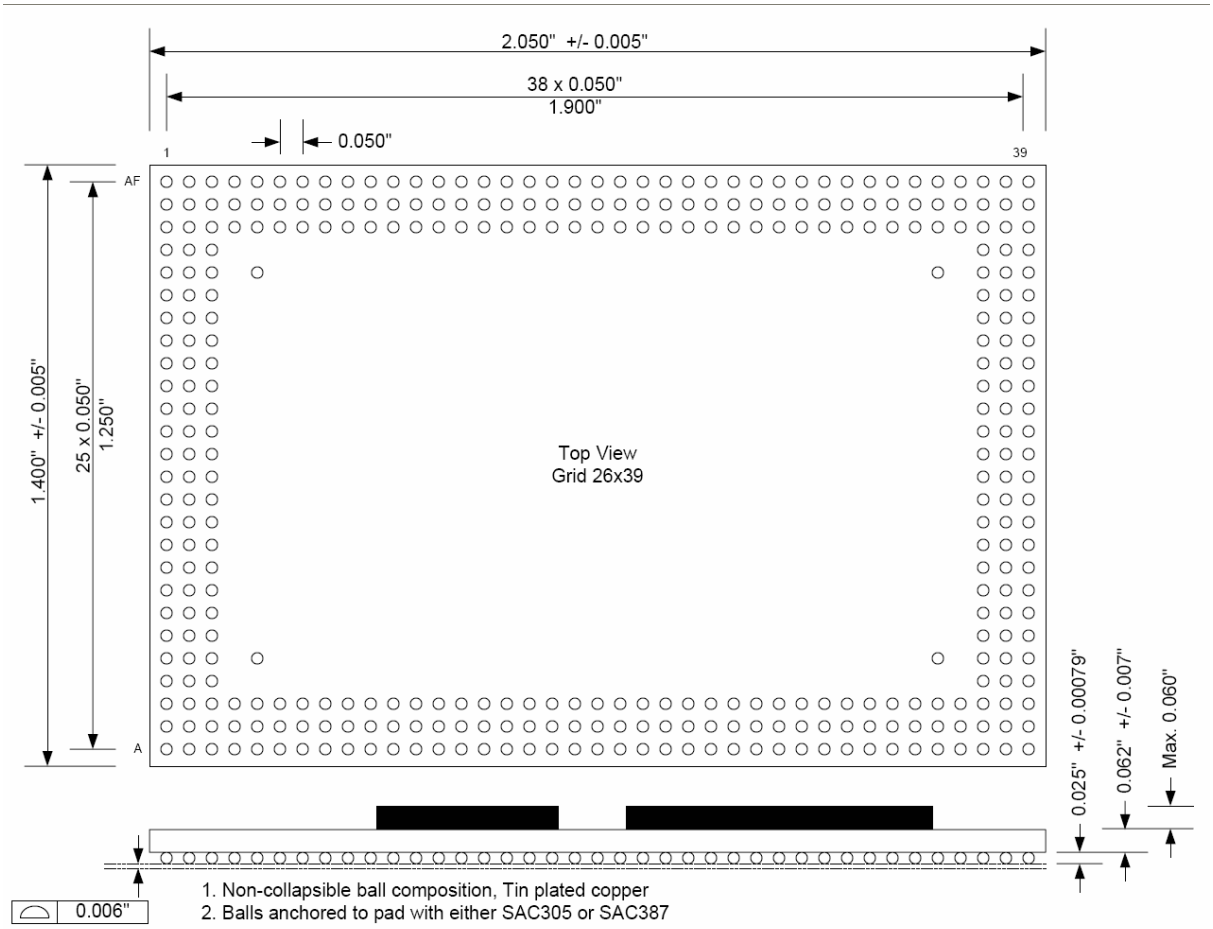
Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AE25	GND
AE26	GND
AE27	GND
AE28	GND
AE29	DVCC18
AE30	DVCC18
AE31	DVCC33
AE32	GND
AE33	DVCC18
AE34	DVCC18
AE5	DVCC18
AE36	GND
AE37	DVCC33
AE38	DVCC33
AE39	DVCC33
AF1	AVcc33
AF2	AVcc33
AF3	AGND
AF4	AGND
AF5	AGND
AF6	AVcc33
AF7	AVcc33
AF8	AGND
A9	AGND
AF10	AGND
AF11	AGND
AF12	ADVCC33
AF13	ADVCC33
AF14	AGND
AF15	AGND
AF16	ADVCC33
AF17	ADVCC33
AF18	ADVCC33
A19	GND
AF20	GND
AF21	NC

Table 9: Pin Assignments by Pin Number (Continued)

Pin Number	Signal
AF22	VCCF33
AF23	SCS_N
AF24	MOSI
AF25	MISO
AF26	MCS_N
AF27	SCLK
AF28	GND
AF29	DVCC18
AF30	DVCC18
AF31	DVCC33
AF32	GND
AF33	DVCC18
AF34	DVCC18
AF35	DVCC18
AF36	GND
AF37	DVCC18
AF38	DVCC18
AF39	DVCC18

Mechanical Dimensions



Ordering Guide

Table 10: Ordering Guide

Product	Ordering Number	Sampling rate (MSPS)	Nyquist Zone
Linearized ADC Module			
OM1400T-125	OM1400T-1250NZ2	125.0	2
OM1400T-125	OM1400T-1250NZ3	125.0	3
OM1400T-125	OM1400T-1250NZ4	125.0	4
OM1400T-125	OM1400T-1200NZ2	120.0	2
OM1400T-125	OM1400T-1200NZ3	120.0	3
OM1400T-125	OM1400T-1200NZ4	120.0	4
OM1400T-125	OM1400T-1150NZ2	115.0	2
OM1400T-125	OM1400T-1150NZ3	115.0	3
OM1400T-125	OM1400T-1150NZ4	115.0	4
OM1400T-125	OM1400T-1100NZ2	110.0	2
OM1400T-125	OM1400T-1100NZ3	110.0	3
OM1400T-125	OM1400T-1100NZ4	110.0	4
Evaluation Board			
	OM1400T-1250NZ2EVAL	125.0	2
	OM1400T-1250NZ3EVAL	125.0	3
	OM1400T-1250NZ4EVAL	125.0	4
	OM1400T-1200NZ2EVAL	120.0	2
	OM1400T-1200NZ3EVAL	120.0	3
	OM1400T-1200NZ4EVAL	120.0	4
	OM1400T-1150NZ2EVAL	115.0	2
	OM1400T-1150NZ3EVAL	115.0	3
	OM1400T-1150NZ4EVAL	115.0	4
	OM1400T-1100NZ2EVAL	110.0	2
	OM1400T-1100NZ3EVAL	110.0	3
	OM1400T-1100NZ4EVAL	110.0	4

Parts with other sample rates are available on request.

Please contact Optichron Sales at (510) 249-5230.

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Revision History

Revision	Change	Page Number	Date
OM1400T-125 rev0.1	Initial Publication	22	7/18/05

