OM1895

Simmerstat control IC

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1 FEATURES

- rfi elimination triac drive circuit
- Low external component count
- Low supply current required
- Variable ON and OFF cycle times
- External ON/OFF triac control available
- No DC component in the AC mains supply
- The ON period always has an odd number of half cycles, and the OFF period an even number
- Gate pulse width may be externally set
- Negative triac gate drive (avoids insensitive quadrant operation)
- Versions available with slower cycle times to meet EMC flicker regulations

2 GENERAL DESCRIPTION

The OM1895 is a precision low power simmerstat control IC for triggering a triac in applications where variable ON and OFF cycle time is required. It is suitable for a broad range of applications, extending from the zero-crossing control of a heating element, a fan motor and other complex loads.

Because the operation of the OM1895 uses characteristics of triacs which are common to typical triacs, but may show some variation in triacs designed to emphasise specific uncommon features, it is preferable to use triacs which have been characterized and specified as suitable for use in this application.

The triac firing circuit uses a unique circuit arrangement by which load current zero crossing is detected, and a widened gate pulse applied during the critical current zero crossing period. Triac conduction is therefore maintained throughout the zero crossing time, ensuring that rfi transients are not generated during this time. With inductive loads only the final half cycle that ends an ON period (made up of an odd number of mains half cycles), will finish with a voltage transient. This may still need a snubber network to limit dv/dt, although it will not be required for the consecutive conducting half cycles during the ON time.

The OM1895 provides a triac controller which offers circuits using a minimum number of components, yet giving great flexibility and accuracy in triac controlled applications.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM1895P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
OM1895T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
OM1895 A		ZAP1 & ZAP2 open circuit	cycling time 0.64s
OM1895 B		ZAP1 open circuit & ZAP2 connected to V_{EE}	cycling time 5.12s
OM1895 C		ZAP1 connected to V_{EE} & ZAP2 open circuit	cycling time 40.96s
OM1895 D		ZAP1 & ZAP2 connected to V_{EE}	cycling time 327.6s

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4 PINNING INFORMATION

4.1 Pin description

SYMBOL	PIN	DESCRIPTION
PWR	1	AC line sense and power input
POT	2	Control input, triac ON/OFF
MODE	3	Triac ON/OFF & function
V_{EE}	4	Negative supply
PX	5	Gate pulse extender
TRG	6	Triac gate drive
V_{CC}	7	Positive Common
RESET	8	Reset input/output

4.2 Pinning layout

Fig.1 Pin configuration
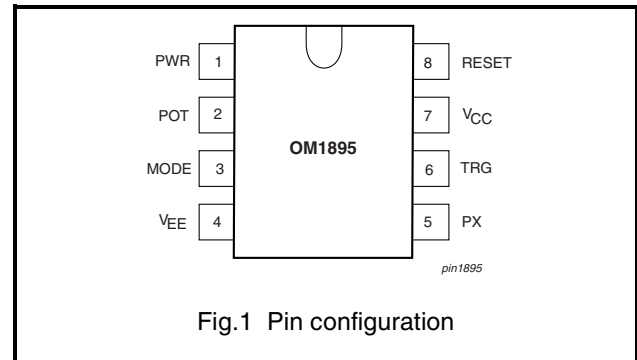
5 BLOCK DIAGRAM

Fig.2 Block diagram
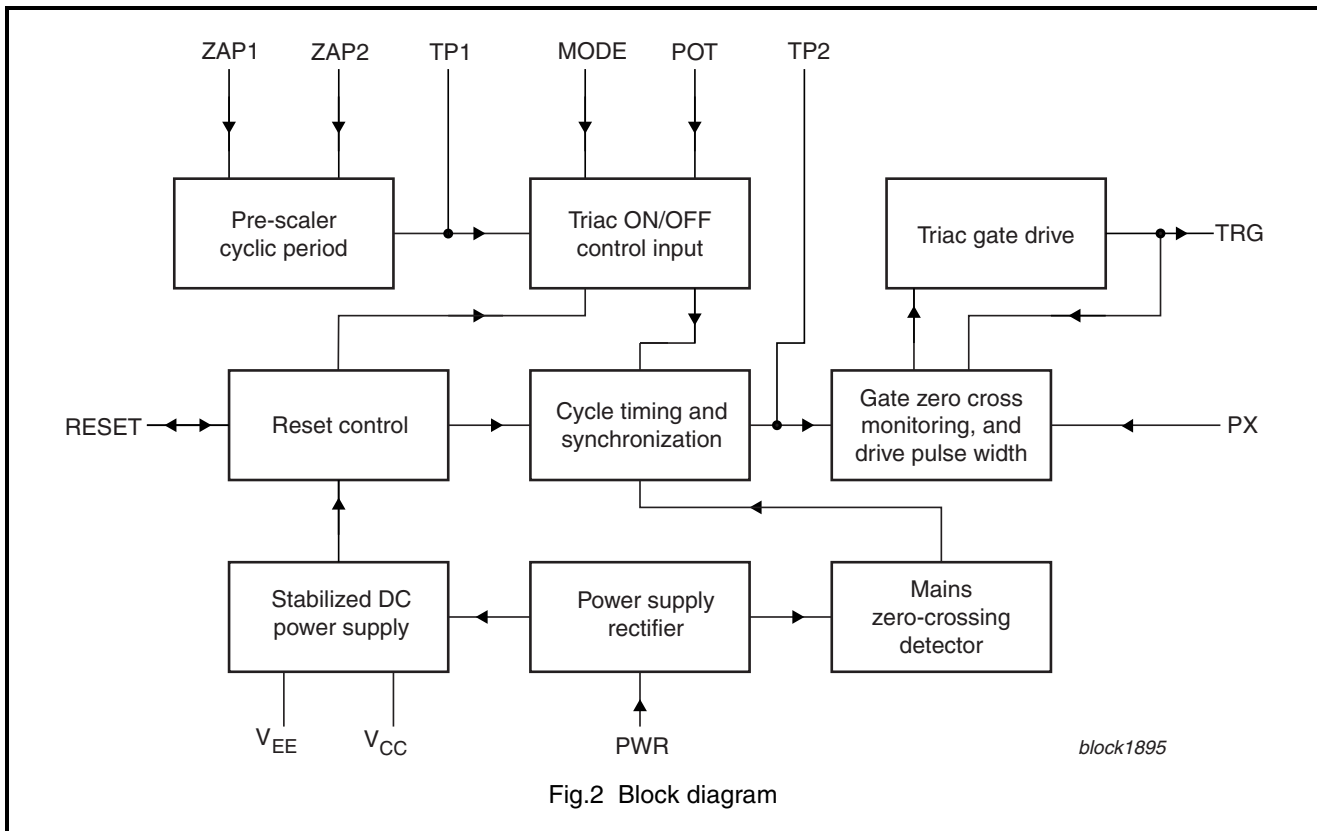
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6 FUNCTIONAL DESCRIPTION

6.1 V_{CC} – Common, positive DC supply

The positive DC supply rail for the control IC type OM1895 is used as the common reference. This is always connected to the T1 terminal of the triac, and being the positive supply rail allows negative gate drive to the triac in both positive and negative supply half cycles on T2. By driving the triac in this way the insensitive quadrant (negative T2 voltage, and positive gate triggering signal) of triacs is avoided.

6.2 V_{EE} – Negative DC supply, substrate

This pin connects to the substrate and the internally generated and regulated negative DC supply, and should be bypassed to V_{CC} (common) by a capacitor of typically 100 μF. The capacitor needs to be sufficiently large to maintain the operating voltage during the half cycle when it is not being charged, as well as to provide the energy to drive the triac gate during the gate pulse.

Internal supply sensing prevents the commencement of an ON cycle while the voltage is too low for reliable circuit operation. If during an ON cycle the supply voltage falls below this level the ON cycle will terminate at the first opportunity consistent with the logic cycle algorithm.

6.3 PWR – Power supply and synchronisation from the mains supply line

The PWR input provides both a synchronisation signal for the logic functions of the OM1895, as well as the DC current used to provide the power supply from which the OM1895 is powered. Signals are derived which indicate the phase and magnitude of the signal on the AC supply. Three states, positive, zero and negative, of this signal is recognised for synchronisation of the triggering times to the mains.

See Figure 3, OM1895 Power Supply Circuit.

The PWR pin is driven by a current limiting resistor from the mains supply. During the positive half cycle current flows through the upper diode D1 to the positive common rail, while

on a negative half cycle the current flows through the lower diode D2, and charges the V_{EE} power supply capacitor.

The zero crossing is signalled by the two comparators, the output signals of which indicate whether the mains voltage is above the common rail voltage, or below the negative V_{EE}. There may be additional resistors in a simple network from the AC supply and V_{EE} to adjust these zero-crossing signals to provide a symmetrical response in the positive as well as the negative going direction.

As the AC signal passes through zero, comparators provide control signals Tp (when $V_{PWR} > V_{CC}$) and Tn (when $V_{PWR} < V_{EE}$) indicating whether the voltage on PWR pin is greater or less than V_{CC} or V_{EE} respectively. A resistor network ensures that these switching points correspond to equal positive or negative thresholds about the AC zero thus giving symmetrical zero-crossing information to the synchronisation and logic circuit.

Synchronisation is obtained from the threshold comparators at the levels of V_{CC} and V_{EE} on the chip.
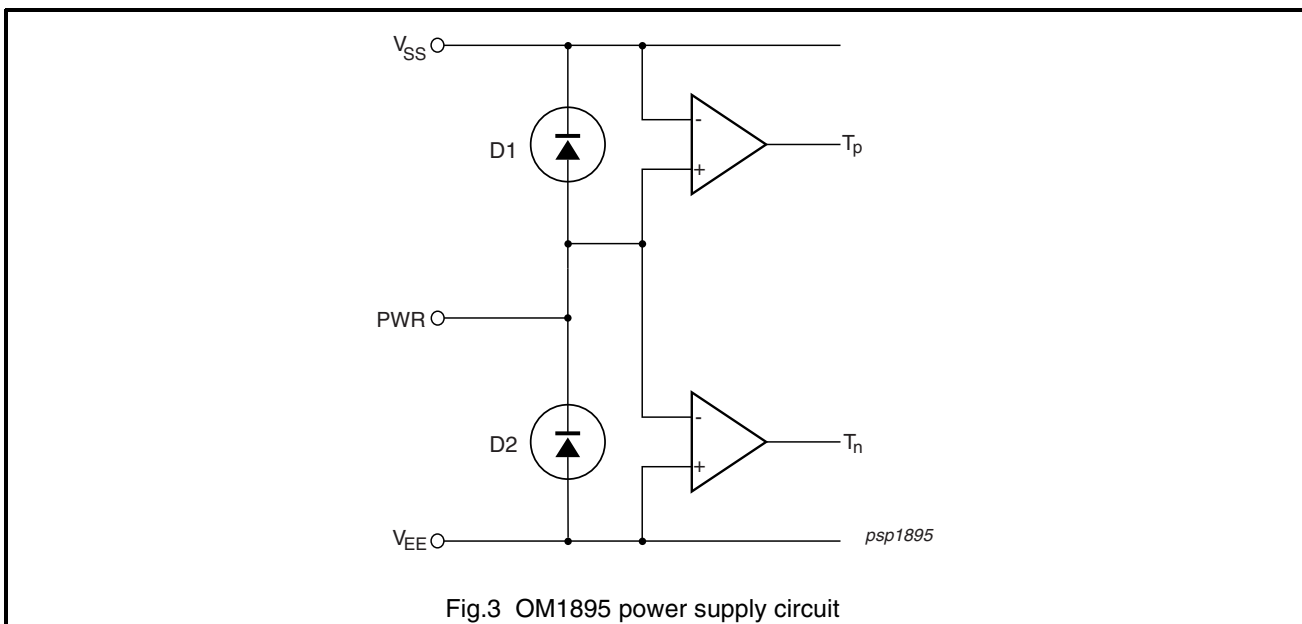

Fig.3 OM1895 power supply circuit

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Adjustment of the initial switching point, and hence the time of initiation of the first firing pulse, and its symmetry about the zero crossing point, is possible by varying the values of the resistors connected between PWR and the active supply, a resistor to V_{EE}, and a resistor to V_{CC}.

When the triac has switched on, the zero-crossing synchronisation information is derived from the voltage on the triac gate while it is conducting, although the polarity information provided by the PWR input signal continues to provide phase information to enable the ON and OFF transitions at the start and finish of an ON burst of conducting half cycles, to be synchronised to prevent repeated firing in the same polarity half cycle, and a resultant net DC load current.

6.4   RESET /Ext_Reset status and control

As the power supply rises towards its operating voltage, a reset signal is generated which holds the logic in an initial state until the voltage has risen to a sufficient value to sustain full operation.

The reset signal is active high to preserve a predictable voltage relationship with the Common supply rail (V_{CC}) rather than V_{EE}. The RESET pin is pulled high by 50µA when the internal reset signal is active. When the power supply voltage reaches its normal regulated level, the RESET pin is pulled low (6µA), and the controller then begins normal operation.

This reset signal can be used to reset counters and other electronic logic circuits which need to begin operation in a known state.

Furthermore, when OM1895s are used in parallel, or with other control circuits, an external reset signal can be applied which will override these internally generated signals.

6.5   MODE – external triac ON/OFF, or function

The mode pin is an external triac ON/OFF control input, and has three active states.

When MODE pin is connected to either V_{CC} (held high) or V_{EE} (held low), then the triac is turned ON and OFF respectively. Irrespective of the control input on POT pin. Figure 5 shows the MODE functions against voltage graphically.

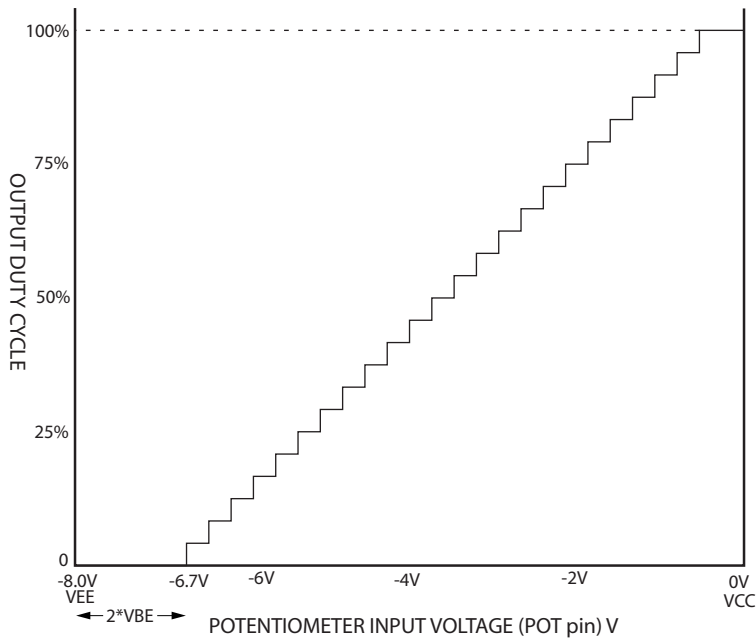When MODE pin is not connected, the OM1895 uses the control input (POT) to turn the triac ON/OFF.

Fig.4 OM1895 POT pin input voltage versus duty cycle characteristic

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6.6 POT – Triac drive control input

When POT pin is connected to V_{CC}, then the triac is turned ON 100%. When POT pin is left unconnected or is connected to 1.2V with respect to V_{EE}, then the triac is fully OFF. Figure 4 shows the characteristic of duty cycle against POT voltage.

The OM1895 generates an internal reference voltage signal which consists of 32 voltage levels, ranging from typically 7.79V down to 1.3V (2Vbe) with respect to V_{EE}. The OM1895 compares the generated reference voltage signal with the voltage signal set on the POT pin, which turns the triac ON when the voltage set on POT pin is greater than the reference voltage, and OFF when the voltage set on POT pin is less than or is equal to the reference voltage.

Additional cycling period can be achieved to extend the triac ON/OFF period by grounding the appropriate ZAP1 and ZAP2 internal pins to V_{EE}. ZAP1 and ZAP2 internal pins are permanently wired during pretest. When ZAP1, ZAP2 pins are not connected, cycling time is 0.64 seconds. If ZAP1 pin not connected and ZAP2 pin is connected to V_{EE}, cycling time is 5.12 seconds. While if ZAP1 pin is connected to V_{EE} and ZAP2 pin not connected, cycling time is 40.96 seconds. Finally, if ZAP1 and ZAP2 pins are both connected to V_{EE}, cycling time is 327.68 seconds or 5.46 minutes.

The voltage signals on POT and MODE pins will switch the triac ON or OFF in a manner which is synchronised to the mains zero crossings. These signals may change at any time, but the triac will only be switched ON or permitted to turn OFF, at a time that is consistent with controlling it at the first available opportunity consistent with the cycling algorithm which triggers the triac for

an odd number cycles in each ON period, and lets it remain OFF for and even number of half cycles. In this way there is no DC current present in the mains supply when it is averaged over a large number of ON cycles and at the same time for inductive loads, a new ON period begins on a half wave of the opposite polarity to the start and finish half wave of the previous run cycle.

6.7 TRG – Triac gate drive

The triac gate output drives the gate through an external current setting resistor. It has in-built protection to withstand transient voltage signals which may be induced on the gate of the triac by mains transients during firing. The gate drive current should be set to a value suited to the gate sensitivity of the triac used. The firing pulse width will need to be of such a width that the specified latching current of the triac when used with the design load has been reached before the gate pulse ends.

In the OM1895 the gate drive is first applied at the start of an ON period at the zero crossing of the mains supply. The leading edge of this obtained from the signal derived from the PWR resistor network before the falling mains voltage reaches zero.

On this first half cycle current is flowing in the triac, and subsequent zero crossings of the triac can be determined in another way. While a resistive load may have the zero crossing determined from the mains supply, this is not possible when the load is inductive (for example, when it is a motor). The current is no longer in phase with the supply voltage, and can reach zero at a time significantly lagging the supply voltage phase.

In the OM1895, the voltage of the triac gate has been found to provide an indicator of imminent zero crossing, and with an appropriate threshold circuit, the gate drive can be

re-applied before the triac turns fully off. Again the gate pulse is determined by the length of the internal delay circuit, plus any additional delay from the application of external resistor and capacitors applied in parallel from the pin PX to V_{EE}

6.8 PX – triac gate pulse width external setting

The gate pulse must be wide enough to be applied from the time the triac is about to turn off until the increasing current in the triac in the opposite direction has reached the latching current of the triac being used.

While there is a time delay circuit within the OM1895 to provide a minimum gate pulse width of typically 100μs, for lower powered loads, where it takes longer for the load current to reach the triac latching current, then it may be necessary to extend the gate pulse.

A parallel resistor and capacitor are connected from pin PX (pulse extender) to V_{EE} giving a pulse extension time of:

$$t_{pw} \approx 1.4 \cdot R \cdot C \qquad (s)$$

The gate pulse is applied for a time determined by either the internal delay time of typically 100μs or the extended time, set by the RC network on the PX pin, whichever is greater.

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7   IMPORTANT: ELECTRICAL SAFETY WARNING

OM1895 circuit is connected to the mains electrical supply and operates at voltages which need to be protected by proper enclosure and protective covering. Application circuits for OM1895 should be designed to conform to relevant standards (such as IEC 65, or Australian Standards AS3100, AS3250 and AS3300), it should only be used in a manner that ensures the appliance in which they are used complies with all relevant national safety and other Standards.

It is recommended that a printed circuit board using this integrated circuit be mounted with non-conductive clips, and positioned such that the minimum creepage distances from the assembly to accessible metal parts, and between high voltage points cannot be transgressed.

It should be noted that as there are Mains Voltages on the circuit board adequate labelling should be attached to warn service personnel, and others, that this danger exists.

A control board assembly should be mounted, preferably vertically, with sufficient free air flow across its surface to prevent the heat dissipated in various components from causing an unacceptable rise in the ambient temperature. The triac also needs to have an adequate heatsink, as exceeding its rated maximum junction temperature can result in loss of control, unpredictable behaviour, and possible dangerous conditions.

The board should be mounted in a place that is clean and dry at all times, not subject to condensation or the accumulation of dust and other contaminants.

8   LIMITING VALUES
In accordance with the Absolute Maximum Rating System (IEC 134).
All voltage measured with respect to V_{CC}, Common.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I	DC current (any pin except 4 & 6)		–	20	mA
I	DC current (pins 4 & 6)		–	70	mA
V_{TRG}	Voltage range TRG, pin6, transient	V_{6-7}	V_4-30	+50	V
V_{PWR}	Voltage range PWR	V_{1-7}	$V_4-0.8$	+0.8	V
$V_{MODE}, V_{PX}, V_{RESET}$	Voltage range MODE, PX, RESET	$V_{3-7}, V_{5-7}, V_{8-7}$	$V_4-0.8$	+0.8	V
P_{tot}	total power dissipation		–	300	mW
T_{stg}	storage temperature		–40	+150	°C
T_{amb}	operating ambient temperature		0	+85	°C

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9   CHARACTERISTICS

At T_{amb} = 25°C; Voltages are specified with respect to V_{CC}.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power supply						
$-V_{EE}$	supply voltage (operating)	I_{CC} = 1 mA	7.4	8.0	8.6	V
$-I_{EE}$	quiescent current	TRG pin open circuit	–	300	350	µA
Power and sensing input, pin PWR						
V_{ut}	upper threshold		–	0	–	V
V_{lt}	lower threshold		–	V_{EE}	–	V
Reset output/input, pin RESET						
V_{reset}	internally generated reset signal	active until power up	–	0	–	V
I_{high}	reset active pull-up current	V_{reset} = –0.5 V	–	50	–	µA
I_{low}	reset off pull-down current	V_{reset} = V_{EE}	–	6	–	µA
V_{reset}	external reset threshold		–	–2	–	V
Gate drive, pin TRG						
I_G	gate current (triac T1 to V_{CC})	set by R_G connected from TRG to gate	–	–	50	mA
V_Gth– V_Gth+	gate sensing thresholds (triac G to V_{CC}, positive and negative)	gate voltage sensing of current zero crossing	–120 +120	–150 +150	–180 +180	mV mV
Pulse stretching, pin PX						
t_{pulse}	gate pulse width	390KΩ from PX to V_{EE}	–	100	–	µs
t_{pulse}	stretched gate pulse width	390KΩ & 220pF in parallel from PX to V_{EE}	–	120	–	µs
Triac drive mode, pin MODE						
V_{ut}	upper mode threshold	hold ON threshold	–	–1.2	–	V
V_{lt}	lower mode threshold	hold OFF threshold	–	V_{EE}+1.2	–	V
I_{in}	mode control input current	V_{mode} = V_{CC} or V_{EE}	–	–	10	µA
Triac drive mode, pin POT						
V_{ut}	upper pot threshold	Output ON 100%	–	0	–	V
V_{lt}	lower pot threshold	Output OFF	–	V_{EE}+1.2	–	V
	POT pin open circuit	Output OFF	–	–	–	–
I_{in}	pot control input current	V_{pot} = V_{CC} or V_{EE}	–	–	1	µA
Cycle timing						
$t_{P(A)}$	Cycle period (mains divided)	OM1895A - 50Hz supply OM1895A - 60Hz supply	– –	0.64 0.53	–	s s
$t_{P(B)}$	Cycle period (mains divided)	OM1895B - 50Hz supply OM1895B - 60Hz supply	– –	5.1 4.3	–	s s
$t_{P(C)}$	Cycle period (mains divided)	OM1895C - 50Hz supply OM1895C - 60Hz supply	– –	41.0 34.1	–	s s
$t_{P(D)}$	Cycle period (mains divided)	OM1895D - 50Hz supply OM1895D - 60Hz supply	– –	328 273		s s

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10 APPLICATION INFORMATION

10.1 Design considerations

Resistors connected directly to the AC supply rail should be specified to withstand the voltage. It is recommended that (Philips BC Components) VR37 (or VR25) high-ohmic / high-voltage resistors be used. These resistors meet the safety requirements of a number of international standards on high voltage applications.

10.2 MODE function

Figure 5 shows graphically the functions obtained by applying a voltage to the mode pin. Open circuit the MODE pin floats in the Cycling part of its characteristic, but a current of less than 10μA flows into or out of MODE when it is held HIGH or LOW to override the cycling function.

The thresholds are set to be 2 x VBE away form the VCC and VEE supply rails, and therefore these are temperature sensitive (−4 mV/deg C). Therefore to guarantee functionality over the temperature range an indeterminate region is shown where the actual observed function will be temperature dependent.
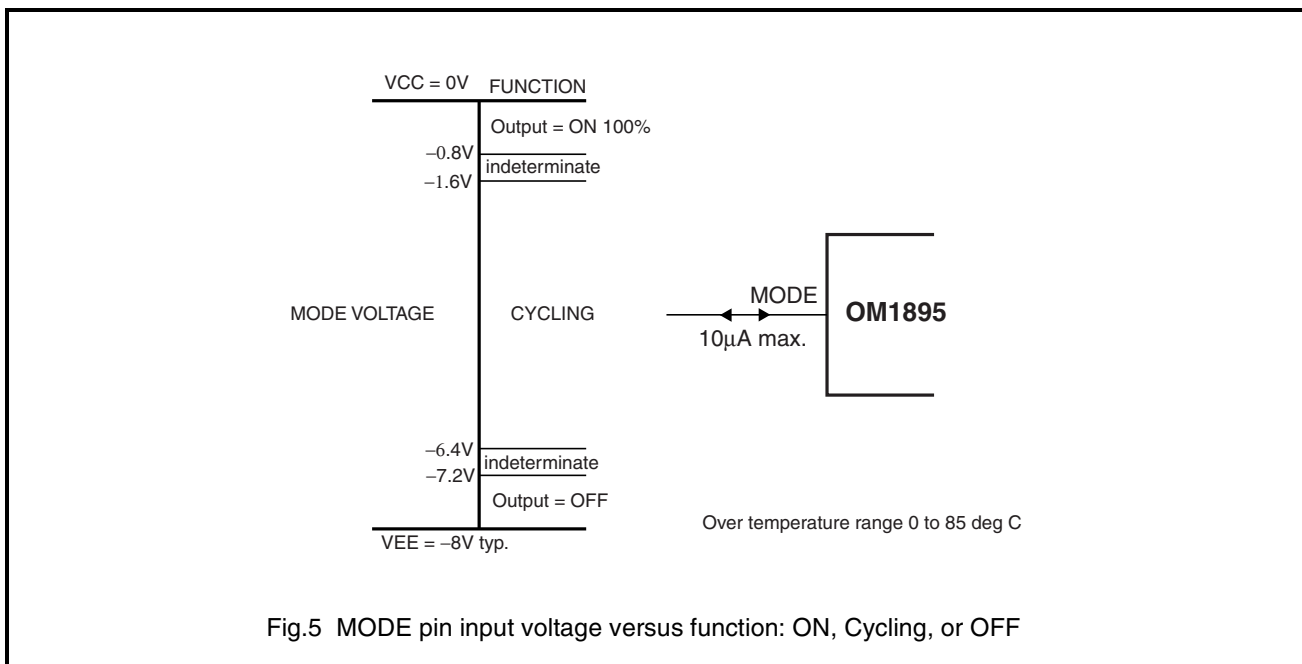

Fig.5 MODE pin input voltage versus function: ON, Cycling, or OFF

10.3 Potentiometer circuits for limiting the power range

In figure 6 a circuit is shown in which resistors can be added to the simple voltage divider between VCC and VEE to limit the range of the input voltage to the POT pin), and in this way limit the control range covered by the potentiometer to a range that does not cover the full zero to 100% range capability of the OM1895.

If there is no significant impedance, or current input loading on the wiper tap on the potentiometer, then by using the potentiometer as a voltage divider between VCC and VEE the resistance tolerance of the potentiometer does not influence the divided voltage. For the OM1895 the POT pin presents very little loading to the potentiometer divider. But even if they did present a load impedance at the IC input pin, it would not effect the duty cycle at each end of the potentiometer travel. Such a load impedance would result in curvature of the potentiometer control characteristic, and any spread from the tolerance of the potentiometer resistance would apply only to the curvature the IC loading presented.

Adding the extra resistors R1, R2 and/or R3 adapts the range covered by the voltage applied to POT to a range that corresponds to the required reduced duty cycle span.

From the graph in figure 7 the required upper and lower (minimum and maximum) duty cycle readings can be read off the horizontal scale in terms of voltage. The input resistor network can then be analysed to find resistor values which provide these voltages when the potentiometer is at the extremes of its range.

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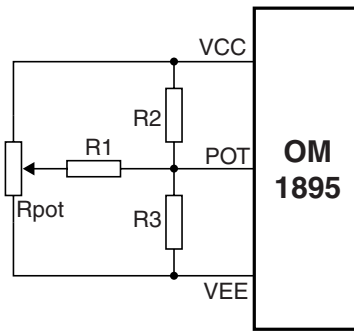

Fig.6 Potentiometer circuit to set a control range of less than 0 to 100%

The choice of potentiometer resistance is limited by the loading which can be applied to the -VEE power supply. Choice of 470k will load the 8 V power supply with a current of 17 μA. The current in the resistor network loads the wiper tap on the potentiometer, the current flowing in R1 needing to be small compared to the current in the potentiometer.

As an example, a circuits is shown in figure 12 using a 470k potentiometer, and values of resistors R1, R2 and R3 chosen to give control over the range of 40% to 80%.

This has been calculated on a spreadsheet, which also calculates the error in the linearity caused by the resistor loading on the potentiometer. (Note that the maximum error may be near the mid point on the

potentiometer if only R2 or R3 are used alone, while if both R2 and R3 are used the error curve is S shaped with an accurate point around the mid-range of the pot. The equivalent circuit load of the potentiometer at its mid point is one quarter of the total resistance Rpot, or 117.5 kΩ. At each end of its travel the potentiometer impedance is zero ohms.
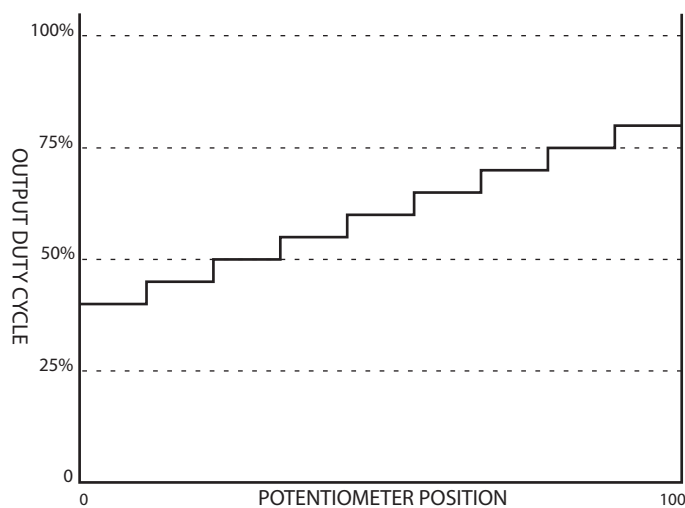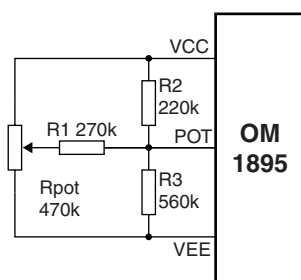

Fig.7 Potentiometer characteristic and circuit to set a control range of 40 to 80%

Because the accuracy of the voltage on Vpot depends on the divided voltage on the potentiometer wiper, and accurate resistors chosen to set the required range, then potentiometer and resistor tolerances and spreads will have negligible effect on the actual duty cycles achieved.

The Excel spreadsheet potcalc.xls automatically calculates the control range for different resistor values in the input network. It shows graphically the duty cycle stepped characteristic that will be provided by the OM1895 controller.

In addition another graph in the spreadsheet shows the ideal characteristic (by ignoring the resistance of the potentiometer and giving a straight line) and the real curve which deviates from the straight line depending on the loading offered by the resistor network R1 to R3. This error may be curved above or below the ideal line or S shaped, depending on whether the R2 or R3 resistors are used, or both.

The final spreadsheet graph shows the error as a deviation from the ideal curve in percentage terms, ignoring the stepped characteristic of the input circuit of the OM1895. It needs to be recognised that one step is about 4%, and that an error of less than 4% can be ignored, especially considering that it is accurate anyway when the pot is fully clockwise or anti-clockwise. As can be shown in the calculated spreadsheet values, changing the pot resistance only changes the error, the end points are not dependent on pot tolerance.

10.4 Gate drive

The 300Ω gate resistor shown in the application circuits gives a little over 10 mA gate drive. Thus for the circuit shown a triac would need to be specified that is suitable for 10 mA triggering with negative triggering signal for both positive and negative

voltage on T2. From the threshold levels determined from the resistive network on PWR, and the AC supply, the timing of the first gate pulse in a conduction cycle can be calculated (assuming a sine wave supply). The specification of the triac will indicate the latching current for switch-on, and knowing the minimum load with which the circuit is to operate, then proper design will ensure that the gate pulse will be long enough, and will not be removed before the triac current reaches this figure.

In addition to the triac gate current, the circuit also uses about 3mA to operate the output gate drive circuit when a triac gate pulse is required.

10.5 Pulse width extension

When the gate pulse is extended by adding a parallel resistor and capacitor from the pulse width extension pin PX to V_{EE}, the power supply current used in driving the gate is a major portion of the available DC power supply needed in the circuit. This has therefore to be included in the calculation of the total power supply requirements.

In particular allowance must be made for the changes in triac characteristics below normal room temperature.

10.6 Power supply requirements

The DC power supply current available for the operation of the circuit is derived from the resistor connected to the PWR pin. On the negative half cycle of the AC signal applied to this resistor, the current into the OM1895 charges the power supply capacitor (typically 100 μF) connected between V_{CC} and V_{EE}.

Apart from the current required by the chip, the triac gate drive presents the major DC current requirement of the circuit. As the gate pulse must be wide enough for the load current to reach the triac's specified holding

current, this may be a significant load on the DC supply (especially with small resistive & inductive triac loads)

10.7 Startup reset

While the reset pin provides an output of the reset condition within the OM1895, and provides a suitable reset signal to reset timers, and external logic circuits which might be used it can also be driven from an external reset source, or connected to another OM1895 reset pin.

It is active HIGH with 50 μA pull up current, and once the power supply reaches its regulated voltage level, falls to a 6 μA pull down condition.

An externally applied reset signal will override these currents, and reset the internal circuitry of the OM1895 in accordance with the state of the externally applied signal.

When two or more OM1895 have reset interconnected, the reset will only be freed when the first of the OM1895 device reaches the shunt operating level. This hysteresis feature on reset pin is to ensure that full operating voltage is reached before reset to internal logic is release during start up.

10.8 Zero-crossing detection

The two thresholds at which the zero-crossing of the input voltage on PWR is sensed are the two supply rails, V_{CC} and V_{EE}. This is set by the resistor from the mains active to PWR and an equal resistor connected between PWR and V_{EE}. The positive threshold will therefore be an equal voltage above V_{CC} due to the divider action of the resistors, while the negative threshold is still equal to V_{EE}, at which point no current is flowing in the second resistor. If a third resistor with suitable values is added from PWR to V_{CC}, then the positive and negative threshold can

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be made larger than the DC supply voltage of $V_{CC} - V_{EE}$.

The symmetry about the zero crossing set by the external resistor network described above only applies to the initial switching point of the first firing pulse. Once the triac has switched on, zero-crossing is derived from the voltage on the triac gate while it is conducting. It is thought that no great benefit is gained from the information provided by the external resistor network. Therefore the resistors connected from PWR to V_{EE} and from PWR to V_{CC} are not included in the application circuit.

10.9 Inductive loads

Because of the triac control method used in the OM1895, both resistive and inductive loads can be controlled without changing the controller circuit.

In the application circuits shown in this data sheet, snubber networks are not shown connected across the triac, nor is an rfi filtering capacitor shown between active and neutral.

The OM1895 provides zero crossing firing of both inductive and resistive loads, and rfi suppression may only be needed to filter residual transient behaviour of the triac which would be present even if the gate was DC fired. For example with high current resistive loads.

However with inductive loads, while the OM1895 provides zero crossing firing during the run cycle at every current zero crossing through this period, when the last half cycle finishes at zero current (not in phase with the mains voltage supply) a single voltage transient will occur which may exceed the dv/dt rating of the triac, and need a snubbing circuit to bring it within the triac ratings. Also that last transient may generate rfi which exceeds the limits published in the standards. However it will no longer be at 100Hz and higher harmonics, as is the case with interference generated in phase with the supply frequency; it will only be a single transient coming at the end of the ON cycle, and therefore occurring a lot less frequently, and falling under other clauses of the standard.

11 APPLICATION CIRCUITS

Two application circuits are included in this data sheet. The first shown in Figure 8 is the basic simmerstat circuit, with potentiometer control of the duty cycle from OFF (zero duty cycle) to fully ON (a duty cycle of 100% ON).

The second circuit in Figure 9 uses the MODE input to give over-riding control of the operation to a thermistor divider, so that if the thermistor detects over-temperature the OM1895 is switched OFF.

To assist in carrying out circuit designs using the OM1895 design spread sheets are available. For figure 8 the file "OM1895 fig 8 app cct.xls" is provided, and for figure 9 the file name is "OM1895 fig 9app cct.xls". These can greatly assist in selecting appropriate values for the external components around the OM1895.

The design process involved in applications using the spreadsheet is as follows:

Enter the nominal, maximum and minimum mains supply voltages and the frequency. (The numbers in BLUE are for the designer to enter). The design needs to ensure that sufficient power supply current is available to maintain operation at the minimum voltage, and yet not dissipate excessive power in the power supply resistor (R2) when the supply voltage is at its maximum.

Next provide the intended load figures (in Watts). Usually the load is fixed (for the example in Figure 9, 1000W), but a circuit may be intended to cover a range of possible loads. The gate pulse needs to be sufficiently wide to cover the zero crossing behaviour of the triac used on minimum load, and at the same time have a sufficient current rating to carry the load current.

Choose a suitable triac. Current rating, gate sensitivity, latching and holding current figures need to be inserted into the table.

It is then necessary to enter the various component values into the spreadsheet, and to check that the results of the calculations give figures that indicate proper operation of the circuit.

The following are the important points, with key results from the calculations shown on the spreadsheet in RED alongside the component values being used:

The heat dissipation in R2, the power supply resistor is important. The resistor must be chosen such that it can handle the mains voltage applied across it (including good transient handling capability), as well as being able to dissipate the power.

R4 sets the gate current. The gate current sensitivity in the data sheet is given for a triac at 25 deg. A margin is desirable for initial operation below 25 deg, and the temperature sensitivity figures are found in the data sheet.

The next important figure is the required gate pulse width. That is the minimum pulse width to be applied to the gate so that the gate drive begins as the triac load current falls below

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the triac holding current (and the triac turns OFF, and continues until the increasing load current in the other polarity has reached the holding current.

The resistor R1 and capacitor C1 are then chosen to give a gate pulse that is at least a wide as the calculated required pulse width (allowing a margin for component tolerances). If the required pulse width is less than 100µs, then the minimum pulse width of 100µs is used and only the resistor is needed from pin PX to VEE (This is the case in the circuit of figure 9 where the higher power load does not need wide gate pulse).

Finally it is necessary to ensure that there is sufficient power supply

available. All of the loads presented to the VEE-VCC DC supply are added up to give a figure indicating the total power supply needed, and this figure is compared to the calculated DC current available through the power supply resistor R2. The available current should exceed that needed by a margin to allow for tolerances, and errors.

The power supply load if first of all the current needed by the OM1895, followed by the average gate current consumed while the gate is driving the triac. Finally any other circuit connected between VEE and VCC requires an estimate of its current load to be included in the spreadsheet.

In these example spread sheets it should be evident how in Figure 9 the extra load presented by the NTC divider has been covered by an addition line in the spreadsheet (cells B83 & B84).

These spread sheets are presented as an aid to support the circuit design, and as other circuit ideas are suggested they are intended to be freely modified by the designer to cover a customer's specific application. Some of the mathematical concepts used are discussed in Application Notes AN001, and AN002. Although these Application Notes were written for other control ICs the discussion of the mathematical concepts used apply equally well to the OM1895.
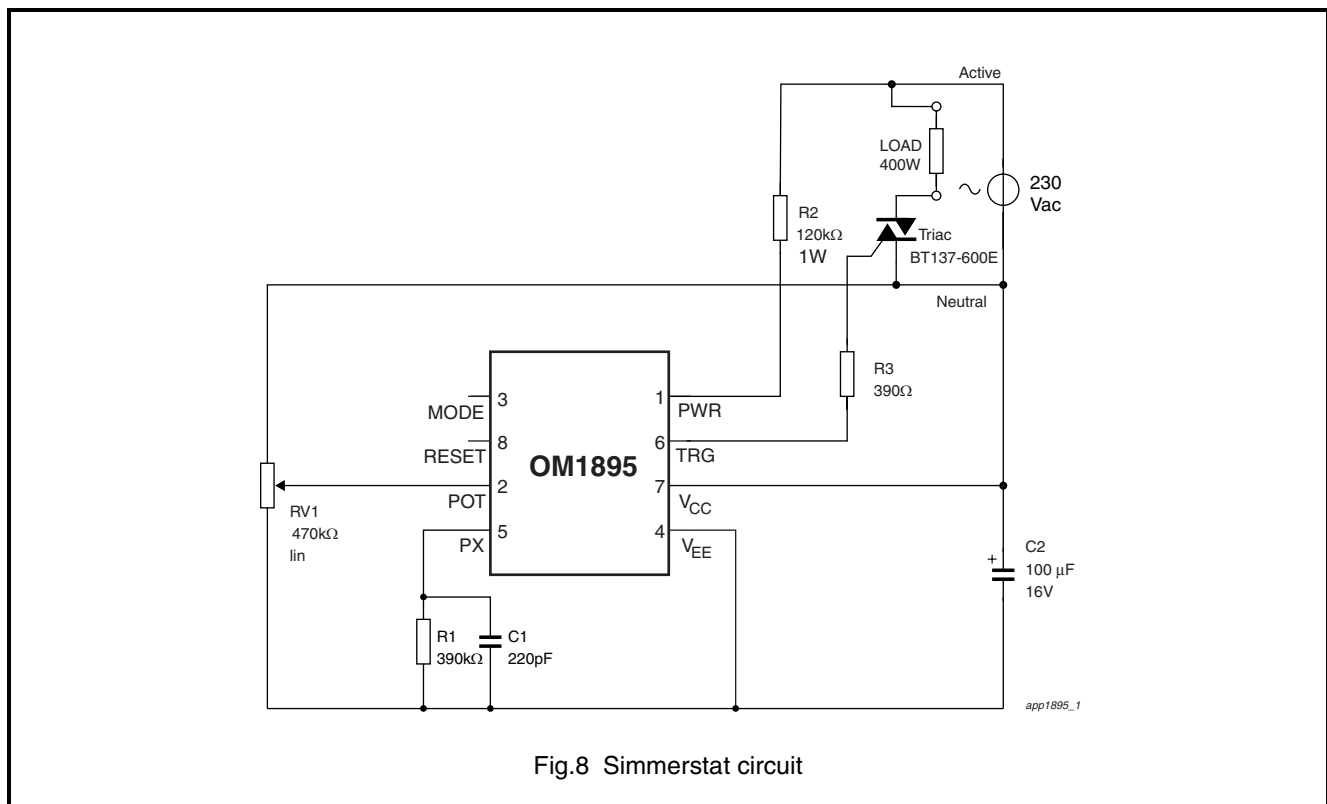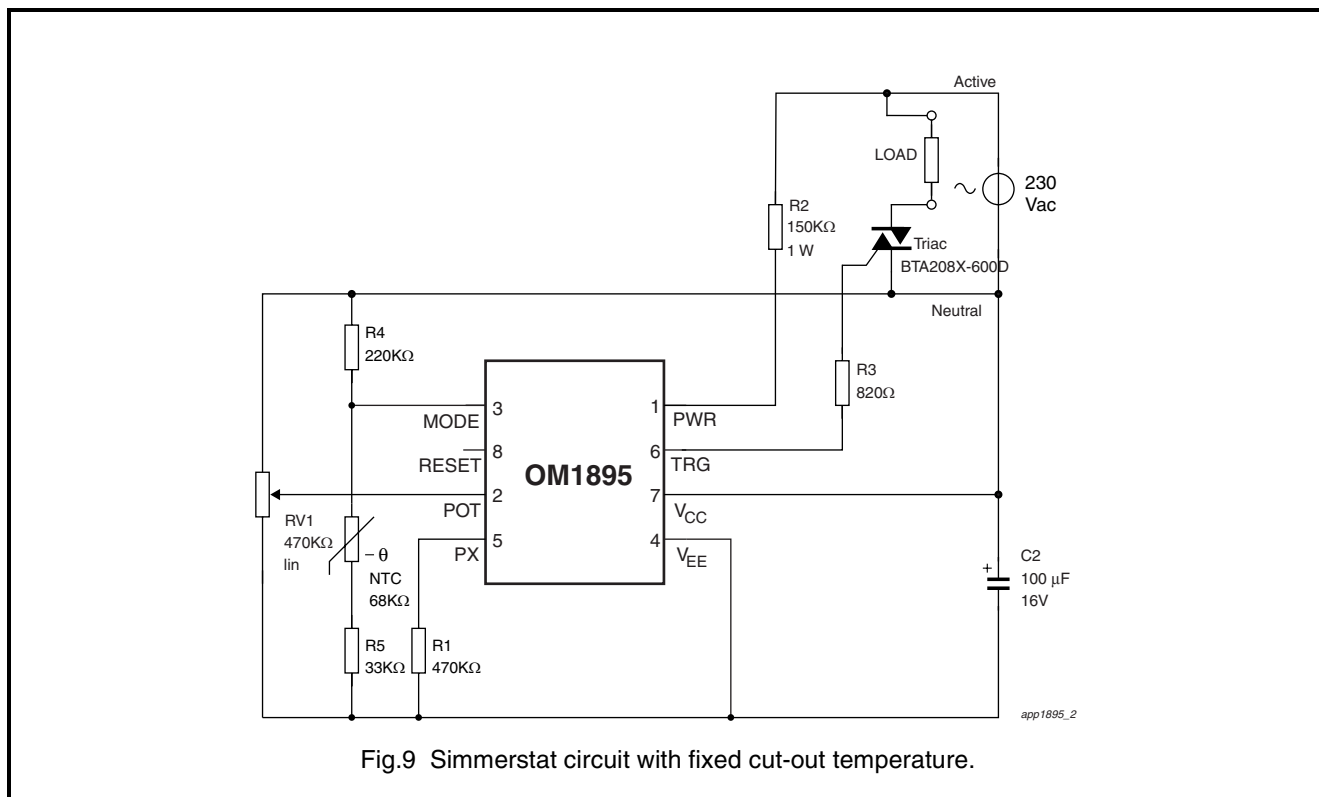

Fig.8 Simmerstat circuit

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Fig.9 Simmerstat circuit with fixed cut-out temperature.

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12 PACKAGE OUTLINES

SO8: plastic small outline package; 8 leads; body width 3.9 mm   **SOT96-1**
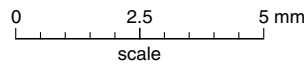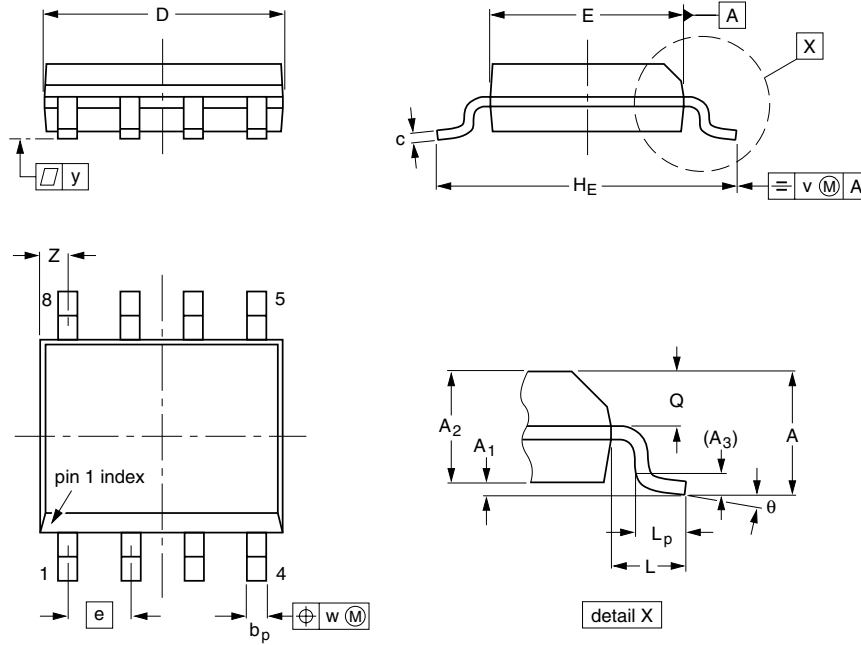
DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

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DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**


```
0        5        10 mm
scale
```

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	b₂	c	D (1)	E (1)	e	e₁	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			95-02-04 99-12-27

13 SOLDERING

13.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Data book" (order code 9398 652 90011).

13.2 DIP

13.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

13.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

13.3 SO

13.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

13.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

13.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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14 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility.Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

15 IES INFORMATION

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