DATA SHEET

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STB5660 (Set-Top Box) STB concept

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STB5660 (Set-Top Box) STB concept OM5721

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1 FEATURES

1.1 SAA7214 features

1.1.1 General SAA7214 features

- Internal PR3001 32-bit RISC processor running at 40.5 MHz
- Comprehensive driver software and development tool support
- A JTAG interface for board test support
- 1-kbyte data and 4-kbyte instruction caches (write-through style).

1.1.2 MPEG2 systems features

- Parsing of Transport Stream (TS), Philips Semiconductors hardware and proprietary software data streams. Maximum input rate is 108 Mbits/s.
- A Digital Video Broadcasting (DVB) compliant descrambler core, incorporating storage for up to 6 control word pairs
- Hardware section filtering based on 32 different Packet Identifiers (PIDs) with a flexible number of filter conditions (8 or 4-byte condition plus 8 or 4-byte mask) per PID and a total filter capacity of 40 (8-byte condition checks) or up to 80 (4-byte condition checks) filter conditions
- 4 Transport Stream/Packetized Elementary Stream (PES) filters for retrieval of data at TS or PES level for applications such as subtitling, TXT or retrieval of private data
- Flexible Direct Memory Access (DMA) based storage of the 32 section substreams and 4 TS/PES data substreams in the external memory
- System time base management with a double counter mechanism for clock control and discontinuity handling
- 2 Presentation Time Stamp (PTS)/Decoding Time Stamp (DTS) timers
- A General Purpose/High Speed (GP/HS) filter which can serve as alternative input from e.g. IEEE 1394 devices. It can also output either scrambled or descrambled TS to IEEE 1394 devices.

1.1.3 External interface features

- A 16-bit microcontroller extension bus supporting DRAM, Flash, (E)PROM and external memory mapped I/O devices. It also supports a synchronous interface to communicate with the integrated MPEG Audio Video Graphics (AVG) decoder SAA7215 at 40.5 Mbytes/s.
- An IEEE 1284 interface supporting master and slave modes. Usable as a general purpose port.
- 3 UART (RS232) data ports with DMA capabilities (187.5 kbits/s) including hardware flow control signals RXD, TXD, RTS, CTS for modem support
- Two dedicated smart-card reader interfaces (ISO 7816 compatible) with DMA capabilities
- Two I^2C-bus master/slave transceivers supporting the standard (100 kbits/s) and fast (400 kbits/s) I^2C-bus modes
- 32 general purpose, bidirectional I/O interface pins, which may also be used as interrupt inputs.
- 2 Pulse Width Modulated (PWM) outputs with 8-bit resolution.

1.2 SAA7215 features

1.2.1 General SAA7215 features

- Single or double external synchronous DRAM organized as $1M \times 16$ or $2 \times 1M \times 16$ interfacing at 81 MHz. Due to efficient memory use in MPEG decoding, more than 1 Mbit is available for graphics in the single SDRAM configuration whereas 17 Mbits are available in the double SDRAM configuration targeted to BSkyB 3.00 and Canal+ 4.0 specifications.
- Dedicated input for compressed audio and video in PES or Elementary Stream (ES) in byte wide or bit serial format. Accompanying strobe signals distinguish between audio and video data.
- Optimum compatibility with the SAA7214 Transport Mega Instructions Per Second (TMIPS) controller
- Flexible memory allocation under control of the external Central Processing Unit (CPU) enables optimized partitioning of memory for different tasks.
- Boundary scan testing implemented.

1.2.2 CPU related features

- External SDRAM self test
- Asynchronous interface possible with external microcontroller

- Support of fast DMA transfer
- High speed/low latency interface with second graphics SDRAM
- Byte access to the full SDRAM in the upper 16-Mbit address range
- Fast 16-bit data plus 22-bit address synchronous interface with external controller at up to 40.5 MHz
- Support of Motorola ColdFire and 68xxx interfaces as well as LSI L64108 interface.

1.2.3 MPEG2 SYSTEM FEATURES

- Support for seamless time base change (edition)
- Processing of errors flagged by channel decoding section.

1.2.4 MPEG2 VIDEO FEATURES

- Decoding of MPEG2 video up to main level, main profile
- Output picture format: CCIR-601 4 : 2 : 2 interlaced pictures. Picture format 720 to 576 at 50 Hz or 720 to 480 at 60 Hz.
- Support of constant and variable bit rates up to 15 Mbits/s for the elementary stream
- Digital video input/output interface on 8-bit, 27 MHz (CbYCrY multiplexed bus), at a CCIR-656 format
- Analog video output interface on both the RGB and Y/C/CVBS formats (internal digital encoder)
- Horizontal and vertical pan and scan allows the extraction of a window from the coded picture
- Flexible horizontal scaling from 0.5 up to 4 allows easy aspect ratio conversion including support for 2.21 : 1 aspect ratio movies. In case of shrinking an anti-aliasing pre-filter is applied.
- Vertical scaling with fixed factors 0.5, 0.75 factor 0.75 is used for letter-box presentation, 1 or 2. Factor 0.5 realizes picture shrink
- Factor 2 can be used for up-conversion of pictures with 288 (240) lines or less
- Horizontal and vertical scaling can be combined to scale pictures to $\frac{1}{4}$ their original size, thus freeing up screen space for graphic applications like Electronic Program Guides (EPGs)
- Non full screen MPEG pictures can be displayed in a box of which position and background colour are adjustable by the external microcontroller. Structured background is available as part of the graphic features.
- Nominal video input buffer size for MP at ML 27-Mbit
- Decoding and presentation can be independently handled under CPU control.
- Various trick modes under control of external microcontroller
- Freeze field/frame on I- or P-frames; restart on I-picture
- Freeze field on B-frames; restart at any moment
- Scanning and decoding of I- or I- and P-frames in a IBP sequence
- Single step mode
- Repeat/Skip field for time base correction
- Repeat/Skip frame for display parity integrity.

1.2.5 MPEG2 AUDIO FEATURES

- Decoding of 2 channel, layer I and II MPEG audio. Support for mono, stereo, intensity stereo and dual channel mode.
- Constant and variable bit rates up to 448 kbits/s
- Supported audio sampling frequencies: 48, 44.1, 32, 24, 22.05 and 16 kHz
- Selectable output channel in dual channel mode
- Dynamic range control at output.
- Independent channel volume control and programmable inter-channel crosstalk through a baseband audio processing unit.
- Muting possibility via (external) controller. Automatic muting in case of errors.
- Generation of ‘beeps’ with programmable tone height, duration and amplitude
- Support for up to 8 channels linear Pulse Code Modulation (PCM) elementary audio streams with 8, 16, 20 and 24 bits/sample and bit rates up to 6.144 Mbits/s
- 96 kHz Linear Pulse Code Modulated (LPCM) samples will be mapped to a 48 kHz multi-channel format
- Volume control for linear PCM samples in three steps: −6 dB, −12 dB and −18 dB
- Burst-formatting of AC-3 elementary streams and MPEG-2 multi-channel streams in ES or PES format for interconnection with an external multi-channel decoder via the digital audio output or the IEC 958 output

- Serial multi-channel digital audio output with 16, 18, 20 or 24 bits/sample, compatible either to I^2S or Japanese formats. Output can be set to high-impedance mode via the external controller.
- Serial Sony/Philips Digital Interface (SPDIF) (IEC 958) audio output. Output can be set to high-impedance mode.

1.2.6 GRAPHICS FEATURES

- Graphics is presented in boxes independent of video format
- Boxes can be up to full screen allowing double buffer display mechanism
- Two independent graphics planes are available for background and/or graphics overlay
- Two independent data paths with RGB 4 : 4 : 4 and YCbCr 4 : 2 : 2 formats available with independent mixing
- RGB path transparent to YCbCr format
- Screen arrangement of boxes is determined by display list mechanism which allows for multiple boxes, background loading, fast switching, scrolling, overlapping and fading of regions
- Real-time anti-flickering performed in hardware. Programmable hardware available for off-line anti-flickering.
- Hard-edged or soft-edged wiping of regions available
- Support of 2, 4, 8, 16 bits/pixel in fixed bit maps format or coded in accordance to the DVB variable/run length standard for region based graphics
- Chrominance down-sampling filter switched per region
- Display colours are obtained via Colour Look-Up Tables (CLUT) or directly from bitmap. CLUT output can be YCbCrT at 8-bit for each signal component thus enabling 16 M different colours and 6-bit for T which gives 64 mixing levels with video. CLUT output can also be RGBT with same resolutions. Non-linear processing available by means of LUTs.
- Conversion matrices available to allow any format on any different data path (RGB or YCbCr)
- Graphics boxes may overlap vertically even inside one graphics layer due to the use of flexible chained descriptors
- Internal support for fast 3-D block moves in external SDRAM through Data Manipulation Unit (DMU)
- DMU allows format conversion and bit manipulation from a chained list of instructions
- Graphics mechanism can be used for signal generation in the vertical blanking interval. Useful for teletext, wide screen signalling, closed caption, etc.
- Support for a single down loadable cursor of 1K pixel with programmable shape
- Supported shapes are 8×128 pixels, 16×64 pixels, 32×32 pixels, 64×16 pixels and 128×8 pixels
- Cursor colours obtained via two 16 entry CLUTs with YCbCrT at 6, 4, 4 respectively
- 2 bits and RGBT at 4, 4, 4 respectively 4 bits (or 4, 5, 3, respectively 4 bits). Mixing of cursor with video and graphics in 4 levels.
- Cursor can be moved freely across the screen without overlapping restrictions.

2 GENERAL DESCRIPTION

2.1 Introduction

Philips Semiconductors Set-Top Box (STB) concept is a Digital Media Broadcast (DMB) platform designed to help developers bring the right product to market at the right time, with a minimum of risk. A complete hardware and software solution for fully-featured digital cable, satellite and terrestrial system, it is based around a powerful, programmable embedded microprocessor core, allowing manufacturers to develop and rapidly evaluate system designs and test application software.

This programmability is the key to maintaining flexibility and reducing risk. Application software can be easily modified to meet changing requirements, so highly featured and differentiated STB designs can be brought quickly to market. It also allows flexible handling of graphics, so manufacturers can implement menus, electronic program guides and the sophisticated graphics-based features expected by today's users.

Sophisticated hardware is supported by a full suite of software, developed in partnership with customers to meet real-world needs and provide the reliability required for consumer electronics products.

2.2 Reference design goal

The Philips STB concept STB5660 is a reference design of a complete hardware and software solution intended for the digital satellite receiver Set-Top Box market. This reference design addresses the potential customer base who is targeting the new world of digital media broadcasting. The reference platform for a Set-Top Box combines the key ICs, the SAA7214 transport MPEG source decoder and the SAA7215 AVG decoder/video encoder, and the software to run a Set-Top Box.

As in many cases a platform is a stepping stone from which evolution and specification enhancements can be launched. The first reference design of the platform contains the necessary functions which demonstrate the performance and capabilities of the system.
Enhancements in the ICs as well as for SW modules will be released during the lifetime of the platform.
The convention which has been used is that backwards compatibility is guaranteed within the platform (STB5000 range).

The main objectives are:

- Firstly providing this complete system, greatly reduces the required investments needed in scarce design resources, and helps customers focus on building a position and responding quickly to the market demand
- Secondly, an advantage of the reference design approach is that the system consisting of complex functions realized in silicon and software can be validated in tangible results
- Thirdly, to create a stable platform from which customized solutions can be derived faster.

It is expected that in the coming years the market will grow in all segments, satellite, cable and terrestrial; and that the captive broadcasters gradually open up their system, focusing more on the services rather then the contents of the box. Their service role at the beginning is to create the market by having box content, then it will change towards the real core service activities bringing content and new services to the home.

This changing behaviour of the service providers calls for the semiconductor providers to offer competitive solutions, enabling the future dreams of the service providers. This implies that in order to plan the evolution of the Set-Top Box functionality, one must be positioned and in control of the whole system.

2.3 Benefits

2.3.1 KEY SYSTEM BENEFITS

- STB5660 offers a good compromise between flexibility, performance and integration of functions which leads to a very attractive price/performance offer
- The SAA7214 performs the descrambling, demultiplexing and control of the STB while the SAA7215 performs the media processing functions such as MPEG2 audio video and graphics processing.
  The communication between the two ICs as well as the memory partitioning and management have been designed so that a true unified memory concept can be implemented with no performance degradation.
- Within the STB family of products, HW and SW footprints will be maintained to ensure the maximum possible reuse of resources
- Philips offering the most comprehensive portfolio of ICs combined with our well known technological capabilities brings the best on a complete system level. This in combination with our local technical support centres gives the customer a fast and secure inroad to the new field of emerging technology.

2.3.2 KEY IC BENEFITS

- SAA7214 incorporates a low cost high performance 32 bits MIPS processor with 4 kbytes instruction cache and 1-kbyte data cache. In addition a 4-kbyte second-level cache, designed for SW optimization but can also be used for ‘last minute’ CPU intensive software patches is offered to software developers, boosting application performance.
- A flexible hardware/software partitioning and optimization for DVB TS demultiplexing has been designed targeted to Canal+ specification. This partitioning makes parsing of incoming stream in hardware, in order to off-load the processor and makes most of the processing from system memory by the MIPS processor, which leaves to software developers the freedom to allocate the right priority at the application level for MPEG system data handling.
- All required DVB/MPEG2 system services are covered by SAA7214, such as full DVB descrambling, section filtering with 32 PIDs handled in hardware and more if required in software, TS/PES filter for maximum flexibility in the service handling and edition (time base discontinuity)

- In terms of interfaces, the SAA7214 interfaces with basic STB peripherals such as UART, smart card interface, IEEE 1284, but also with the next generation high speed interfaces such as IEEE 1394
- SAA7214 is able to control with a high speed clock (40.5 MHz) DRAMs, Flash, EEPROM and is able to control the SAA7215 as a memory mapped device with a maximum sustained rate of 40.5 Mbytes/s, which enables fast graphic update in the second SDRAM
- SAA7215 has a scalable memory architecture: 16 Mbits for low-end and 32 Mbits for mid/high-end applications. Furthermore, there is a full decoupling of MPEG processing and graphics/CPU control buses and control, which offers a high bandwidth and low latency for CPU when accessing the graphics memory.
- SAA7215 features 5 independent graphics planes that can address all the known digital TV video and graphics requirements:
  - Background: where still pictures can be displayed in the background
  - Foreground: where broadcast graphics and the user interface can be displayed
  - Video: where still or moving video is displayed
  - Cursor: implemented in hardware to offer fast responses times.
- Graphics are processed internally in high resolution RGB 4 : 4 : 4 format which provides the best quality in graphics rendering as well as for mixing with video in 4 : 2 : 2 format
- A dedicated Data Manipulation Unit (bit block transfer type) offers very fast block move and data manipulation during the transfers. This can be used to perform scaling of graphics, transfers from 4 : 2 : 0 to CLUT or RGB formats, or fast block move in MPEG or graphics SDRAMs.
- SAA7215 offers flexible scaling features, including letter box conversion that is now becoming a needed features for broadcasters
- Two independent mixed video/graphics and video-only signal paths are implemented and allow software disabling of the user interface for recording on VCR
- Integrated digital video encoder with Y/C, CVBS and RGB outputs reduce the Bill of Materials (BOM) and also the board space, while still offering the possibility to have access to the YUV digital bus through CCIR-656 interface.
- SAA7215 is ready for future audio features such as AC-3 or high fidelity LPCM audio, such as requested by the world-wide DVD standard, but also for high-end STB in the USA. SAA7215 processes LPCM audio data and can interface gluelessly with an external multi-channel audio decoder such as the SAA2505, through IEC 958 interface.

3 BLOCK DIAGRAM

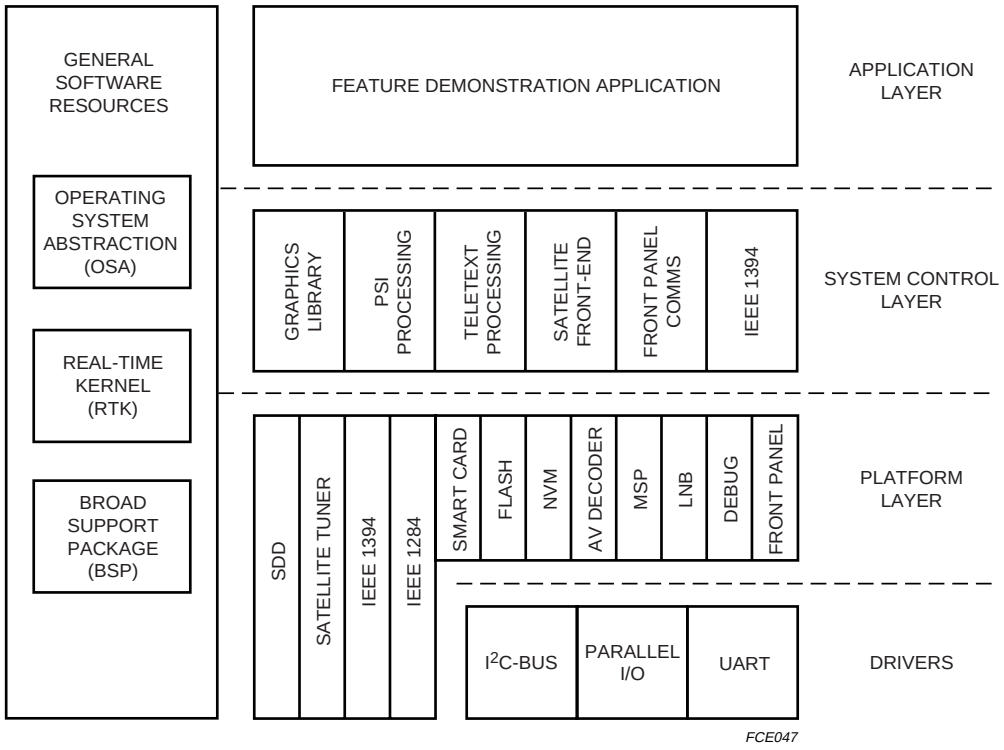

Fig.1 Software block diagram.

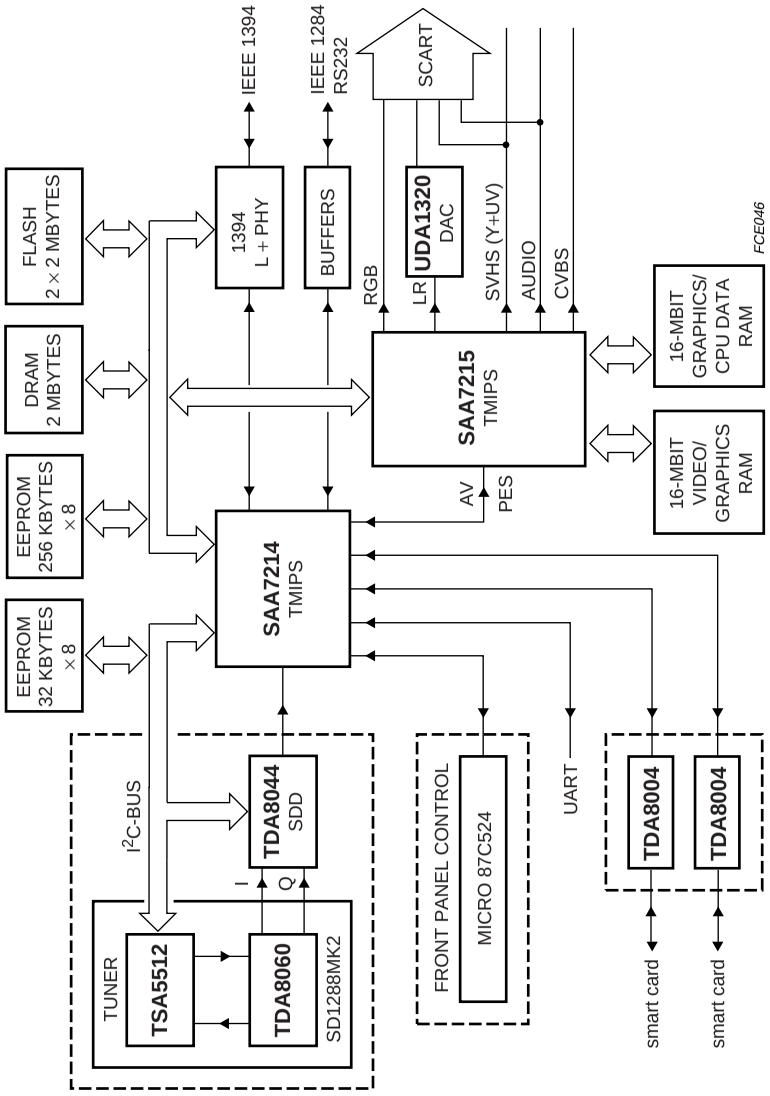

Fig.2 Hardware block diagram.

4 HARDWARE

4.1 IC list

Table 1 Description of system ICs

HARDWARE	DESCRIPTION
Channel module	
SD1288MK2	Tuner
TDA8044	Satellite demodulator and decoder
Front panel board	
87C524	Microcontroller
Main board	
SAA7214	Descrambler, demultiplexer and MIPS core
SAA7215	Audio, video, graphics and digital encoder
PDI1394L11	Link and physical layer of 1394
PDI1394P11	Link and physical layer of 1394
UDA1320	Audio DAC
TDA8004	Smart Card Interface

4.2 Main board

4.2.1 SAA7214

The SAA7214 (TMIPS) is a transport MPEG2 source system decoder it includes a MIPS R3000 microcontroller core and several peripheral interfaces such as UARTs, I^2C-bus units, an IEEE 1394, and an IEEE 1284 (Centronics) interface.

SAA7214 receives transport streams through a versatile stream input interface capable of handling both byte-parallel and bit-serial streams, in various formats, supporting data streams up to and including 13.5 Mbytes/s (108 Mbits/s). The stream data is first applied to an on-chip descrambler incorporating DVB descrambling algorithms, on the basis of 6 control word pairs stored in on-chip RAM.

Demultiplexing is subsequently applied to the stream, to separate up to 40 individual data streams.
The demultiplexer section includes clock recovery and timebase management.

Program Specific Information (PSI), Service Information (SI), Conditional Access (CA) messages and private data is selected and stored in external memory, for subsequent off-line processing by the internal R3000 microcontroller core.

4.2.2 SAA7215

The SAA7215 is a MPEG2 source decoder which combines audio decoding and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics, background display and/or on-screen display as well as encoding of output video. Due to an optimized architecture for audio and video decoding, maximum capacity in external memory and processing power from the external CPU is available for graphic support.

4.3 Front-end

The front-end allows reception of channels transmitted by satellite received via a satellite dish in combination with a Low Noise Blockdown (LNB). The Outdoor unit can be controlled with:

- 0FF/14 V/18 V pouring for polarisation steering
- 22 kHz tone switching control for band switching
- Digital Satellite Equipment Control (DiSEqC) V1.0.

4.4 Front panel

4.4.1 LNB INTERFACE

Master transmitter DiSEqC is provided and 14/18 V switching this is routed through the digital board to the front-end utility connector. The possibility to disable the DiSEqC on the front panel, allows for the next generation Quatro Phase Shift Key (QPSK) front-end which will have DiSEqC.

4.4.2 IR

The on-board microcontroller decodes the IR commands in RC5/6 format and relays via the serial link to the SAA7214.

4.4.3 KEYS

STANDBY, UP, DOWN, LEFT, RIGHT, OK, MENU

4.4.4 SCART CONTROL

Pin 8 control as per the SCART specification for 16×9 and 4×3.

Pin 16 control as per SCART specification for RGB fast blanking (in this case used to switch between RGB and composite).

4.5 Memory

4.5.1 NON-VOLATILE MEMORY (NVM)

A 32-kbyte NVM is implemented with an EEPROM connected to the I^2C-bus to allow for channel data storage, etc.

4.5.2 DRAM

2 Mbytes (1M × 16); 60 ns fast or hyper-page mode.

4.5.3 BOOT ROM

256 kbytes (256 kbytes × 8) to allow for ROM boot up and also to provide ROM emulation.

4.5.4 FLASH

2 Mbytes [2 × (512K × 16)]; this can be up-graded to 4 Mbytes [2 × (1M × 16)].

Two flash banks are needed to allow code to be run from one bank while writing to the other.

4.5.5 VIDEO AND GRAPHICS RAM

4 Mbytes SDRAM [2 × (1M × 16)] at 81 MHz.

4.5.6 MEMORY OPTIONS

Surface mount links can select memory configuration.

Remark: The boot chip select is selectable between Boot ROM and Flash.

4.6 Connectors

Table 2 The main board connectors

CONNECTOR	DESCRIPTION
Optical SPDIF	A SPDIF signal from the SAA7215 is brought out via an optical output connector.
SPDIF	To allow connection of the Philips SAA2505 AC3/MPEG7.1 surround sound.
SCART	1 standard SCART, audio/video output signals only.
3 Phonos (RCAs)	CVBS, right audio and left audio.
SVHS	The Y/C output from the SAA7215 is brought out to a standard SVHS connector.
CCIR 656 connector	A connector to the CCIR 656 YUV output from the SAA7215.
JTAG	A standard JTAG connector for Boundary Scan testing.
DEBUG socket	A surface mount DEBUG socket allowing connection to a Philips REDDX connector via a conversion board to allow connection to a REDDNET or REDDROM board.
RS232	An additional RS232-C (±12 V) interface to provide a board connector for debug use. One half of a suitable RS232 driver chip will be used for signal level conversion.
IEEE 1394	The Philips PDI1394L11 and PDI1394P11 is implemented to provide half-duplex 1394 access from the SAA7214. Under isolation mode the power for the physical IC will be taken from the bus via the switching regulator. The option between isolated and non-isolated is selectable via option links. Two 1394 connectors are available on the back panel.
IEEE 1294	Subject to Electro-Static Discharge (ESD), standard logic are implemented as buffers to provide 1284 to a 25-way D-type female connector on the back panel.

5 SOFTWARE DESCRIPTION

5.1 Software overview

5.1.1 General Software Resources

- Real-time kernel
- Board support package
- Operating system abstraction package.

5.1.2 Application layer

- Feature demonstration application.

5.1.3 System Control layer

- Graphics library
- PSI processing
- Front panel communications
- 1394
- Satellite front-end component
- Teletext processing component.

5.1.4 Platform layer

- MPEG System Processor (MSP)
- Audio/Video/Graphics device driver
- Front Panel device driver
- Flash Memory device driver
- Non-Volatile Memory device driver
- Debug UART device driver
- IEEE 1394 device driver
- Smart Card device driver
- IEEE 1284 device driver
- LNB device driver
- Satellite Tuner device driver
- TDA8044 device driver.

5.1.5 I/O device drivers

- Parallel I/O device driver
- I^2C-bus device driver
- UART device driver.

5.2 General software resources

This layer is used by all the layers. Typical parts are Real-time operating system functionality, C-library and debug components.

5.3 System Control layer

Part of the System Control layer provides functionalities which are a compound of device driver functionality.

Examples of the system control layer components are teletext, which uses the TS/PES package a part of MSP device driver and the AVG device driver. Also the front-end satellite component is a functional layer component, it uses the LNB device driver, the Satellite Tuner device driver and the TDA8044 device driver.

5.4 Platform layer

The platform layers consists of set of platform drivers each controlling a Set-Top Box functionality that is implemented in hardware. Examples of a Set-Top Box functionality are video decoding, audio decoding and section filtering. It is possible that more than one platform driver can control a physical hardware component (IC) if this component provides a set of Set-Top Box functions.

The interface of a platform driver consists of generic set of functions. It is the intention not to directly specify hardware interface functions but MPEG/DVB related functions. In this way future generations of controlled hardware use the same sub-set of interface functions. Some platform drivers do not directly interface with the hardware but use an I/O platform driver. Platform drivers are not allowed to communicate with each other. If communicating is required between platform drivers it is under control of a component located in the functional layer.

The I/O platform drivers provide the functions when a device driver does not directly have access to the hardware. Examples of I/O device drivers are an I^2C-bus device driver and an UART device driver.

5.5 Application layer

This layer has been limited only to demonstrate the possibilities that can be implemented at the application layer.

5.5.1 TOP LEVEL MENU

Main menu options:

- Installation menu
- Tuning menu
- Feature demonstration menu.

5.5.2 INSTALLATION MENU

The installation menu is used to select the board configuration options. The selected options are stored to NVM.

Table 3 Board configuration options

ITEM	CONFIGURATION OPTION
LNB setup	On/off DiSEqC LNB and Single or Dual band; note 1.
Video standard	PAL or NTSC; default PAL.
SCART	Pin 16 control (RGB or composite video signalled).
Display	Allows selection of 16 : 9 or 4 : 3 TV screen.

Note

1. With non-DiSEqC LNBs the control is simply by 14/18 V switching for polarity and in the case of a Dual band the use of 22 kHz signal (no modulation) selecting the High Band. With DiSEqC LNBs the control is by sending DiSEqC commands via modulation in the 22 kHz signal. (This means DiSEqC level 1).

5.5.3 TUNING MENU

5.5.3.1 Transponder setup

The transponder can be setup automatically or manually.

Selecting the automatic option gives the user the possibility to sweep the band over a particular frequency range at all symbol rates. All transponders found will be logged and stored to NVM. The sweep can be started by pressing the start button via the user controls.

Selecting the automatic network option will give the user the possibility to sweep the band over a particular frequency range at a user defined symbol rate.
The Network Information Table (NIT) from the first transponder found will be read and the services known in this NIT will be logged and stored to NVM.

Table 4 Program setup

ITEM	OPERATION
Source	The source of the transport stream can be selected between tuner and stream server. In Tuner mode the ability to change the selected transponder is available.
Listing	Shows the current transport stream and the possible audio PIDS for the selected service. The service can be selected and the audio PID chosen.

Selecting the manual option provides the user with the ability to enter additional transponder data, or to adjust transponders found with an auto setup. To add a transponder the correct frequency, symbol rate, polarisation and Forward Error Correction (FEC) rate are required.

5.5.4 FEATURE DEMONSTRATION MENU

Table 5 Screens highlighting the main features of the Philips SAA7214/SAA7215 chip-set.

SCREEN	FEATURE
Audio	
Audio routing and Dual channel	Audio routing options; mono, stereo, LL, RR. Dual channel options; Channel 1, Channel 2, both (1-L, 2-R).
Mute	Sound muted
Balance	Control via a text box for left/right balance
Beep	Control of the volume, frequency and duration; the beep can then be heard.
LPCM demonstration	Show the possibility of decoding Linear Pulse Code Modulated (LPCM) audio samples. This besides the decoding of normal MPEG audio although both cannot be not done at the same time. This feature is for example used to play uploaded audio samples. A command is given when the audio and video decoding is running. This command will start the demonstration. The function itself will play about 1 second of LPCM audio and will continue with normal MPEG audio and video decoding afterwards.
IEEE 1394	
IEEE 1394 disable	I/O of IEEE 1394 traffic can be disabled. IEEE 1394 will carry on relaying any IEEE 1394 between the two IEEE 1394 ports. Also choose between input/output of data into systems.
Smart card	
Smart card	A service scrambled using the default keyword will be descrambled upon insertion of a Smart card which contains authorization to use the default keyword.
PC download	
PC download	When selected, the MPEG board will wait for the download of a bit map picture, via the IEEE 1284 port. Upon completion of the download the picture will be displayed, the progress of the download is also displayed.
MIPS performance	
MIPS Performance	This will show the MIPS performance in drystones under the current setup.
Block copy	To show a fast block copy, a bit map picture is copied across the screen. This function is also supported in hardware but handling this in software makes the function more flexible. The actual copying is executed in the SAA7215 hardware by the DMU. Software however has to upload the picture, initialize and start the DMU with correct parameters. The cost however compared to the hardware tiling is processor and memory use.
Graphics	
Text and Drawings	A combination of different fonts and line drawings to demonstrate colour depth and resolution capabilities.
Fast transfer	Fast transfer feature; via IEEE 1284.
Planes demo	Demonstration of the different graphics layers, by displaying quarter screen video over a MPEG I frame background with superimposed text and cursor.
Fade	Combination of video and graphic layers showing fading in and out of the graphics layer.
Tiling	One smaller picture is displayed multiple times in a user selectable rectangle.
Hard-edge wiping	Two pictures in one plane, overlapping each other where the user can move and select the pictures
Soft-edge wiping	Two user selectable and movable pictures in two planes, with transparency in the pictures.

SCREEN	FEATURE
Anti-flickering	The anti-flickering demonstration highlights the functions available in the SAA7215 to reduce the line flickering in graphics regions. During this demonstration, 2 graphics regions are displayed. One with anti-flickering and one without. The contents of the bit map in the regions is one that shows flickering without anti-flicker measures active. Video and audio decoding are still active and visible during the demonstration.
Grab frame store to OSD and scale ¼ continuously location	A picture of the running video is grabbed and displayed ¼ of its original size as a 16-bit, bit map on a graphics plane. The picture data of an I or P picture is copied from a frame store to SDRAM2 memory. During the copy the format of the data is converted from 4 : 2 : 0 format to 4 : 2 : 2 and converted into the graphics memory bit map format. Then the picture is displayed on the screen. The demonstration runs continuously. It displays the running video while a graphics region ¼ of the screen size is in the top left corner. This graphics region is showing the I- and P-pictures of the running video.
Scale ⅑ of 16 bit per pixel graphics location	This demonstration shows a 16 bit /pixel bit map in an OSD region on the screen. This picture will be scaled to a factor ¼ and ⅑ of the original size and displayed on the screen, after the original is removed. The scaling is done by using a software routine that executes a DMU program. During the demonstration, audio and video is playing.
Menu	During all the demonstrations, graphics regions with menu bars and buttons are visible for control of the demonstration.
Scaling	
Cut-out	Display of 16 : 9 video on a 4 : 3 display by cutting out 4 : 3 centres and panning/scanning. This demonstration shows the pan/scan control via the left/right cursor keys. This function would usually be under control from data in the transport stream.
Letter-box	Display of 16 : 9 video on a 4 : 3 display using letter-boxing.
Continuous horizontal, vertical steps	Allows a window to be selected using the cursor; the video will then be resized to fit the selected window.
Video control	
Video control	Scan, freeze, play, stop
Teletext	
Teletext	Switch on and off of the VBI insertion by using a graphics region in VBI lines.
Debug	
Event logging	User enabled event logging provided via the RS232 debug socket.

6 DEVELOPMENT ENVIRONMENT

This chapter describes how you can develop your own STB5660 application, what environment you need. What hardware and software interface the system provides. It answers the question what you need to start developing your application. In addition it will tell you what you will receive with the system that gets you on your way and shorten development time and reduce the costs involved.

6.1 Summary of the STB5660 kit

When you receive the STB5660 development system it will offer you a complete Set-Top Box system with all needed documentation for development. This will give you a 'plug and play' solution to test and develop a system based on this platform.

6.1.1 THE HARDWARE

This consists off a satellite front-end board, a front panel with the display and IR-receiver, a main board, smart card unit, the remote control and all cables needed to make the necessary connections. On the main board you will find a programmed EPROM and Flash memory.

6.1.2 THE SOFTWARE

You will receive not only the binary executable, but also all source codes in C, header files and documentation files. The software will include the complete Application Programmers Interface (API) for all components on the board, except for IEEE 1394, which will be a subset of the standard. This API will offer a developers logical services like audio, video, graphics, descrambling, etc. Together with this you will get the Feature Demonstration Application (FDS). This is an application that will show you the key features of the system.

6.1.3 DOCUMENTATION

Here you will find the user manual and programmers reference for all major parts of the system like the SAA7215 (AVGD chip), the SAA7214 (MPEG2 descrambler demultiplexer chip), and the satellite front-end module (OM5718).

6.1.4 TEST REPORTS

These are included to prove the system maturity. You will see the reports of the API tests and the reports concerning the extensive In-System-Test. The latter is done to prove the chip-set in a complete system environment, a customer like set-up, customer use based on our experience with previous end-customers.

6.2 How to get started

The first day you receive the system you can hook up a satellite dish or transport stream (DiSEqC or not), a TV, connect power to the system and it will start with the FDS program. This demo gives you a menu driven interface to the system. You can test and experiment with all main features of the system. See how fast the On-Screen Display functions, try out the IEEE 1394 interface to a similar board, look at window tests, try out teletext, etc. This will give you an understanding of the system and its possibilities.

6.3 Hardware interface with the STB5660

Besides the dish and the TV (SCART, SVHS, CCIR 656 YUV) there is an interface to IEEE 1394, SPDIF (multi-channel audio decoder, to a PC via RS232 and IEEE 1284 (Centronics), a debug socket (ROM emulator, I/O), JTAG connector (boundary scan testing), smart-card unit and a remote control.

To use a ROM emulator there is an I/O connector on the main PCB where an extension board fits on the debug connector. This extension gives you access to two footprints for 1-Mbyte ROMs.

6.4 Software interface with the STB5660

In the following way you can interface to the system to develop and debug your own application. Connect a PC (or other development system) with a ROM emulator to extension board on the debug connector, compile the supplied source code and load the executable in the ROM emulator. Connect the RS232 debug port to the PC and run a terminal program, this will give you a debug screen.

If you don't have a ROM emulator you can use the parallel port (IEEE 1284) of the Set-Top Box. There is a loader program embedded in the EPROM of the system which allows development without ROM emulator.

The maximum possible memory configuration consists of a boot ROM (256 kbytes) with the loader program, 2 Mbytes fast DRAM as scratch memory, 32 kbytes NVM for channel data storage, 4 Mbytes Flash memory to store the program and 4 Mbytes SDRAM video memory. The boot Chip Select can be switched between boot ROM and Flash memory. Of course a smaller configuration is possible, just leave the memory footprints open.

6.5 Running ‘Hello world’

We have supplied a small program which is called ‘Hello world’ to help you start developing you own software. How can we get the supplied ‘Hello world’ application running if we work with the a PC and a ROM emulator?

Connect the emulator to the STB5660 board via the extension board. Then connect the PC RS232 port to the STB5660 RS232 port. The program is running pSOS as the read-time software. You need the pSOS libraries to build the software. Compile the platform layer (drivers), the Board Support Package and the ‘Hello world’ program. Load the executable in the ROM emulator and start the program. You will see the ‘Hello world’ text on the debug window. You are now ready to start writing your own application, with help from the programmers reference documentation and user guide.

7 CONTENTS LIST FOR STB5660

Table 6 Delivery list for the STB5660 system

ITEM	DESCRIPTION
1. Hardware	Front panel
	OM5718
	STB5660 main board
	STB5660 main board
2. Software	Front panel driver
	Satellite Software driver
	SAA7214 driver
	SAA7215 driver
	TXT driver
	Feature demonstration application
3. Documentation	Objective system specification long
	SAA7214 IC specification
	SAA7214 Driver Software Programmer’s Reference
	SAA7214 User manual
	SAA7215 IC specification without registers medium
	SAA7215 Driver Software Programmer’s Reference
	SAA7215 User manual
	TDA8044 specification
	87C524 specification
	PDI1394L11 specification
	PDI1394P11 specification
	UDA1320 specification
	TDA8004 specification
	TDA8060 specification
	TSA5512 specification
	Hardware Definition Document of main board
	STB5660 System Validation Report
	User Guide of Feature demonstration application
	Schematics OM5721, Front panel
	Gerber files
	Check list
4. Cables	RS232 cable, 1394 cable
	SCART, power cable

8 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

9 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

10 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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