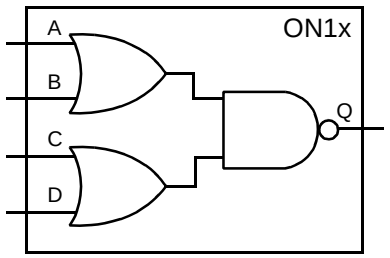
### Description

ON1x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 2-input NAND gate.

**Logic Symbol**




**Truth Table**

| A | B | C | D | Q |
|---|---|---|---|---|
| L | L | X | X | H |
| X | X | L | L | H |
| All other combinations | | | | L |



### HDL Syntax

Verilog ..... ON1x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON1x port map (Q, A, B, C, D);

### Pin Loading

| Pin Name | Equivalent Loads | | | |
|---|---|---|---|---|
| | ON11 | ON12 | ON14 | ON16 |
| A | 1.0 | 1.0 | 1.0 | 2.1 |
| B | 1.0 | 1.0 | 1.0 | 2.1 |
| C | 1.0 | 1.0 | 1.0 | 2.1 |
| D | 1.0 | 1.0 | 1.0 | 2.1 |

### Size And Power Characteristics

| Cell | Equivalent Gates | Power Characteristics[a] | |
|---|---|---|---|
| | | Static $I_{DD}$ ($T_J$ = 85°C) (nA) | $EQL_{pd}$ (Eq-load) |
| ON11 | 2.0 | TBD | 2.3 |
| ON12 | 4.0 | TBD | 6.6 |
| ON14 | 4.0 | TBD | 7.6 |
| ON16 | 8.0 | TBD | 15.7 |

a. See page 2-15 for power equation.

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## AMI5HG 0.5 micron CMOS Gate Array

### Propagation Delays (ns)

Conditions: $T_J$ = 25°C, $V_{DD}$ = 5.0V, Typical Process

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **ON11** | **Number of Equivalent Loads** | | **1** | **2** | **5** | **8** | **10 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.16<br>0.21 | 0.22<br>0.26 | 0.39<br>0.41 | 0.54<br>0.54 | 0.64<br>0.63 |
| **ON12** | **Number of Equivalent Loads** | | **1** | **4** | **8** | **13** | **17 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.37<br>0.38 | 0.47<br>0.50 | 0.59<br>0.64 | 0.73<br>0.79 | 0.84<br>0.91 |
| **ON14** | **Number of Equivalent Loads** | | **1** | **8** | **15** | **22** | **30 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.39<br>0.42 | 0.50<br>0.59 | 0.59<br>0.71 | 0.69<br>0.82 | 0.81<br>0.93 |
| **ON16** | **Number of Equivalent Loads** | | **1** | **14** | **28** | **42** | **56 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.37<br>0.42 | 0.46<br>0.57 | 0.54<br>0.70 | 0.63<br>0.81 | 0.73<br>0.91 |

Delay will vary with input conditions. See page 2-17 for interconnect estimates.