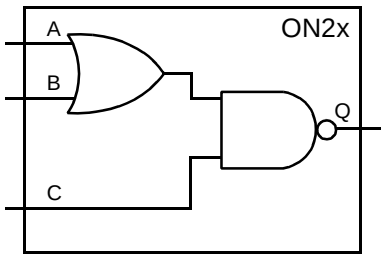
Description

ON2x is a familyof OR-NAND circuits consisting of one 2-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	Q
L	L	X	H
X	X	L	H
All other combinations			L

HDL Syntax

Verilog ..... ON2x *inst_name* (Q, A, B, C);

VHDL..... *inst_name*: ON2x port map (Q, A, B, C);

Pin Loading

Pin Name	Equivalent Loads			
	ON21	ON22	ON24	ON26
A	1.0	1.0	1.0	2.1
B	1.1	1.0	1.0	2.1
C	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON21	2.0	TBD	2.0
ON22	3.0	TBD	6.4
ON24	4.0	TBD	7.3
ON26	7.0	TBD	15.2

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON21	**Number of Equivalent Loads**		**1**	**2**	**5**	**8**	**10 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.12 0.20	0.19 0.25	0.38 0.39	0.55 0.51	0.65 0.60
ON22	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.37 0.39	0.45 0.51	0.57 0.65	0.72 0.81	0.84 0.94
ON24	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.40 0.43	0.50 0.60	0.60 0.72	0.70 0.83	0.82 0.94
ON26	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.38 0.43	0.47 0.58	0.59 0.70	0.71 0.80	0.80 0.90

Delay will vary with input conditions. See page 2-17 for interconnect estimates.