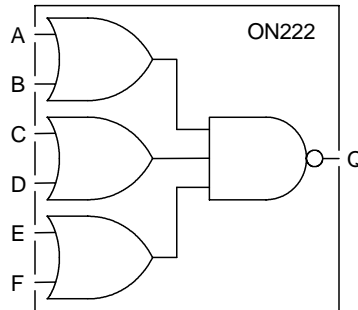


ON222 is an OR/NAND circuit providing the logical function $Q = \text{NOT} [(A+B).(C+D).(E+F)]$.

Truth Table

A	B	C	D	E	F	Q
L	L	X	X	X	X	H
X	X	L	L	X	X	H
X	X	X	X	L	L	H
X	H	X	H	X	H	L
X	H	X	H	H	X	L
X	H	H	X	X	H	L
X	H	H	X	H	X	L
H	X	X	H	X	H	L
H	X	X	H	H	X	L
H	X	H	X	X	H	L
H	X	H	X	H	X	L



Capacitance

	Ci (pF)
A	0.053
B	0.060
C	0.054
D	0.061
E	0.061
F	0.066

Area

0.95 mils²

Power

3.06 μW/MHz

Delay [ns] = tpd.. = f(SL, L)

with SL = Input Slope [ns] ; L = Output Load [pF]

Output Slope [ns] = op_sl.. = f(L)

with L = Output Load [pF]

AC Characteristics : Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Delay A to Q	tpdar	0.72	2.08	2.67	0.87	2.12	2.79
	tpdaf	0.46	1.39	1.77	0.47	1.32	1.76
Delay B to Q	tpdbr	0.69	1.99	2.69	0.95	2.18	2.81
	tpdbf	0.42	1.35	1.73	0.42	1.26	1.69
Delay C to Q	tpdcr	0.60	1.97	2.55	0.77	1.99	2.65
	tpdcf	0.44	1.34	1.74	0.52	1.36	1.79
Delay D to Q	tpddr	0.58	1.86	2.61	0.85	2.04	2.67
	tpddf	0.40	1.31	1.71	0.48	1.33	1.76
Delay E to Q	tpder	0.50	1.84	2.44	0.65	1.89	2.53
	tpdef	0.39	1.28	1.68	0.56	1.39	1.81
Delay F to Q	tpdfr	0.44	1.75	2.48	0.74	1.92	2.57
	tpdff	0.36	1.27	1.64	0.50	1.33	1.76

Characteristics	Symbol	SL = 0.1			SL = 2.0		
		L = 0.1	L = 0.7	L = 1.0	L = 0.1	L = 0.7	L = 1.0
Output Slope A to Q	op_slar	1.83	5.73	7.83	1.95	5.81	7.83
	op_slaf	1.01	3.65	4.90	1.17	3.62	4.93
Output Slope B to Q	op_slbr	1.87	5.81	7.73	2.17	5.88	7.78
	op_slbf	0.95	3.57	4.93	1.11	3.55	4.86
Output Slope C to Q	op_slcr	1.67	5.55	7.62	1.83	5.58	7.62
	op_slcf	1.02	3.67	4.90	1.25	3.67	4.97
Output Slope D to Q	op_sl dr	1.68	5.57	7.61	1.90	5.57	7.61
	op_sl df	0.93	3.58	4.81	1.18	3.58	4.87
Output Slope E to Q	op_sl er	1.53	5.73	7.76	1.63	5.76	7.68
	op_sl ef	1.02	3.67	4.88	1.35	3.73	5.00
Output Slope F to Q	op_sl fr	1.48	5.63	7.66	1.75	5.52	7.65
	op_sl ff	0.95	3.56	4.92	1.27	3.65	4.88