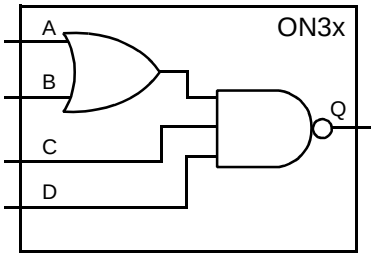
Description

ON3x is a family of OR-NAND circuits consisting of a 2-input OR gate and two direct inputs into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	X	X	H
X	X	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON3x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON3x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON31	ON32	ON34	ON36
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.1	1.0	1.0	2.1
D	1.0	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON31	2.0	TBD	2.6
ON32	4.0	TBD	9.0
ON34	4.0	TBD	6.3
ON36	8.0	TBD	15.8

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON31	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.17 0.23	0.23 0.29	0.32 0.41	0.42 0.53	0.51 0.65
ON32	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.49	0.49 0.63	0.61 0.78	0.75 0.94	0.86 1.06
ON34	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.43	0.50 0.59	0.60 0.71	0.69 0.81	0.80 0.92
ON36	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.36 0.43	0.47 0.59	0.57 0.70	0.66 0.80	0.75 0.89

Delay will vary with input conditions. See page 2-17 for interconnect estimates.