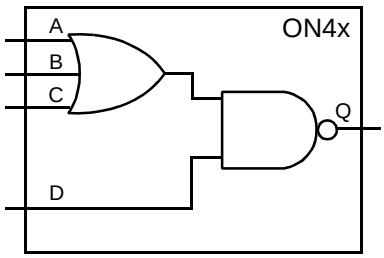
Description

ON4x is a family of OR-NAND circuits consisting of one 3-input OR gate into a 2-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	X	H
X	X	X	L	H
All other combinations				L

HDL Syntax

Verilog ..... ON4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: ON4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	ON41	ON42	ON44	ON46
A	1.0	1.0	1.0	2.1
B	1.0	1.0	1.0	2.1
C	1.0	1.0	1.0	2.1
D	1.0	1.0	1.0	1.0

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ON41	2.0	TBD	2.5
ON42	4.0	TBD	7.6
ON44	4.0	TBD	8.2
ON46	8.0	TBD	13.4

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ON41	**Number of Equivalent Loads**		**1**	**2**	**4**	**6**	**8 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.17 0.20	0.26 0.26	0.42 0.35	0.58 0.44	0.72 0.54
ON42	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.50 0.43	0.59 0.55	0.71 0.69	0.86 0.84	0.97 0.96
ON44	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.48 0.46	0.59 0.62	0.69 0.75	0.79 0.85	0.89 0.96
ON46	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.46 0.42	0.56 0.59	0.67 0.72	0.77 0.82	0.86 0.91

Delay will vary with input conditions. See page 2-17 for interconnect estimates.