

AMI5HG 0.5 micron CMOS Gate Array

Description

ON8x is a family of OR-NAND circuits consisting of two 2-input OR gates into a 3-input NAND gate.

Logic Symbol	Truth Table																														
	<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>E</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>X</td> <td>X</td> <td>X</td> <td>H</td> </tr> <tr> <td>X</td> <td>X</td> <td>L</td> <td>L</td> <td>X</td> <td>H</td> </tr> <tr> <td>X</td> <td>X</td> <td>X</td> <td>X</td> <td>L</td> <td>H</td> </tr> <tr> <td colspan="5">All other combinations</td> <td>L</td> </tr> </tbody> </table>	A	B	C	D	E	Q	L	L	X	X	X	H	X	X	L	L	X	H	X	X	X	X	L	H	All other combinations					L
A	B	C	D	E	Q																										
L	L	X	X	X	H																										
X	X	L	L	X	H																										
X	X	X	X	L	H																										
All other combinations					L																										

Core Logic

HDL Syntax

Verilog ON8x *inst_name* (Q, A, B, C, D, E);

VHDL *inst_name*: ON8x port map (Q, A, B, C, D, E);

Pin Loading

Pin Name	Equivalent Loads		
	ON82	ON84	ON86
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics ^a	
		Static I _{DD} (T _J = 85°C) (nA)	EQL _{pd} (Eq-load)
ON82	5.0	TBD	9.9
ON84	5.0	TBD	10.3
ON86	12.0	TBD	22.0

a. See page 2-15 for power equation.

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Propagation Delays (ns)

Conditions: $T_J = 25^\circ\text{C}$, $V_{DD} = 5.0\text{V}$, Typical Process

ON82	Number of Equivalent Loads		1	4	8	13	17 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.50	0.50 0.64	0.62 0.80	0.77 0.98	0.88 1.11
ON84	Number of Equivalent Loads		1	8	15	22	30 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.41 0.55	0.50 0.74	0.60 0.88	0.71 1.01	0.83 1.14
ON86	Number of Equivalent Loads		1	14	28	42	56 (max)
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.39 0.51	0.48 0.68	0.60 0.81	0.70 0.92	0.78 1.03

Delay will vary with input conditions. See page 2-17 for interconnect estimates.