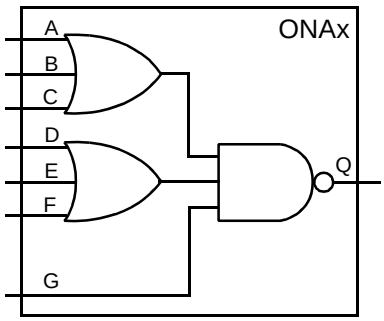
Description

ONAx is a family of OR-NAND circuits consisting of two 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	Q
L	L	L	X	X	X	X	H
X	X	X	L	L	L	X	H
X	X	X	X	X	X	L	H
All other combinations							L

HDL Syntax

Verilog ..... ONAx *inst_name* (Q, A, B, C, D, E, F, G);

VHDL..... *inst_name*: ONAx port map (Q, A, B, C, D, E, F, G;)

Pin Loading

Pin Name	Equivalent Loads		
	ONA2	ONA4	ONA6
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1
G	1.0	1.0	2.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONA2	6.0	TBD	11.7
ONA4	8.0	TBD	12.3
ONA6	12.0	TBD	22.7

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONA2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.53 0.53	0.62 0.67	0.72 0.82	0.86 0.98	0.97 1.11
ONA4	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.45 0.53	0.58 0.71	0.68 0.85	0.78 0.96	0.89 1.07
ONA6	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.48 0.52	0.59 0.72	0.67 0.85	0.76 0.97	0.86 1.09

Delay will vary with input conditions. See page 2-17 for interconnect estimates.