AMERICAN MICROSYSTEMS, INC.

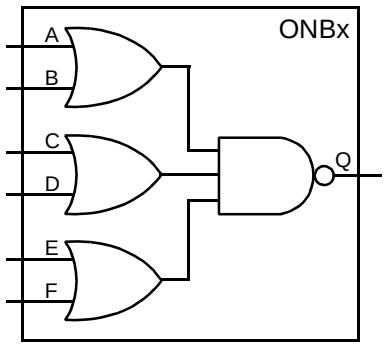
## AMI5HG 0.5 micron CMOS Gate Array



### Description

ONBx is a family of OR-NAND circuits consisting of three 2-input OR gates into a 3-input NAND gate.

**Logic Symbol**




**Truth Table**

| A | B | C | D | E | F | Q |
|---|---|---|---|---|---|---|
| L | L | X | X | X | X | H |
| X | X | L | L | X | X | H |
| X | X | X | X | L | L | H |
| All other combinations | | | | | | L |

### HDL Syntax

Verilog ..... ONBx *inst_name* (Q, A, B, C, D, E, F);

VHDL..... *inst_name*: ONBx port map (Q, A, B, C, D, E, F)

### Pin Loading

| Pin Name | Equivalent Loads | | |
|---|---|---|---|
| | ONB2 | ONB4 | ONB6 |
| A | 1.0 | 1.0 | 2.1 |
| B | 1.0 | 1.0 | 2.1 |
| C | 1.0 | 1.0 | 2.1 |
| D | 1.0 | 1.0 | 2.1 |
| E | 1.0 | 1.0 | 2.1 |
| F | 1.0 | 1.0 | 2.1 |

### Size And Power Characteristics

| Cell | Equivalent Gates | Power Characteristics[a] | |
|---|---|---|---|
| | | Static $I_{DD}$ ($T_J$ = 85°C) (nA) | $EQL_{pd}$ (Eq-load) |
| ONB2 | 5.0 | TBD | 10.5 |
| ONB4 | 6.0 | TBD | 11.1 |
| ONB6 | 12.0 | TBD | 18.8 |

a. See page 2-15 for power equation.

### Propagation Delays (ns)

Conditions: $T_J$ = 25°C, $V_{DD}$ = 5.0V, Typical Process

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **ONB2** | **Number of Equivalent Loads** | | **1** | **4** | **8** | **13** | **17 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.41<br>0.50 | 0.49<br>0.65 | 0.60<br>0.80 | 0.74<br>0.97 | 0.86<br>1.10 |
| **ONB4** | **Number of Equivalent Loads** | | **1** | **8** | **15** | **22** | **30 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.42<br>0.56 | 0.54<br>0.75 | 0.64<br>0.89 | 0.74<br>1.01 | 0.84<br>1.13 |
| **ONB6** | **Number of Equivalent Loads** | | **1** | **14** | **28** | **42** | **56 (max)** |
| | From: Any Input<br>To: Q | $t_{PLH}$<br>$t_{PHL}$ | 0.37<br>0.46 | 0.48<br>0.63 | 0.58<br>0.80 | 0.68<br>0.92 | 0.78<br>1.02 |

Delay will vary with input conditions. See page 2-17 for interconnect estimates.