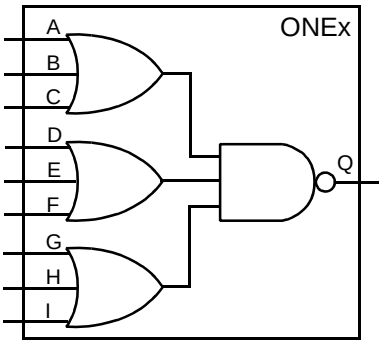
Description

ONEx is a family of OR-NAND circuits consisting of three 3-input OR gates into a 3-input NAND gate.

Logic Symbol



Truth Table

A	B	C	D	E	F	G	H	I	Q
L	L	L	X	X	X	X	X	X	H
X	X	X	L	L	L	X	X	X	H
X	X	X	X	X	X	L	L	L	H
All other combinations									L

HDL Syntax

Verilog ..... ONEx *inst_name* (Q, A, B, C, D, E, F, G, H, I);

VHDL..... *inst_name*: ONEx port map (Q, A, B, C, D, E, F, G, H, I);

Pin Loading

Pin Name	Equivalent Loads		
	ONE2	ONE4	ONE6
A	1.0	1.0	2.1
B	1.0	1.0	2.1
C	1.0	1.0	2.1
D	1.0	1.0	2.1
E	1.0	1.0	2.1
F	1.0	1.0	2.1
G	1.0	1.0	2.1
H	1.0	1.0	2.1
I	1.0	1.0	2.1

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
ONE2	7.0	TBD	13.3
ONE4	8.0	TBD	14.4
ONE6	14.0	TBD	22.4

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

ONE2	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.51 0.52	0.60 0.67	0.72 0.82	0.86 0.99	0.97 1.12
ONE4	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.52 0.57	0.63 0.76	0.73 0.89	0.83 1.01	0.94 1.12
ONE6	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.50 0.53	0.60 0.72	0.69 0.85	0.77 0.98	0.85 1.09

Delay will vary with input conditions. See page 2-17 for interconnect estimates.