

FEATURES

- *Guaranteed max. 0.5 μ V/ $^{\circ}$ C Drift*
- *Guaranteed max. 0.6 μ V pk-pk Noise*
- *Guaranteed max. 2nA Bias Current*
- *Guaranteed minimum 114dB CMRR*

APPLICATIONS

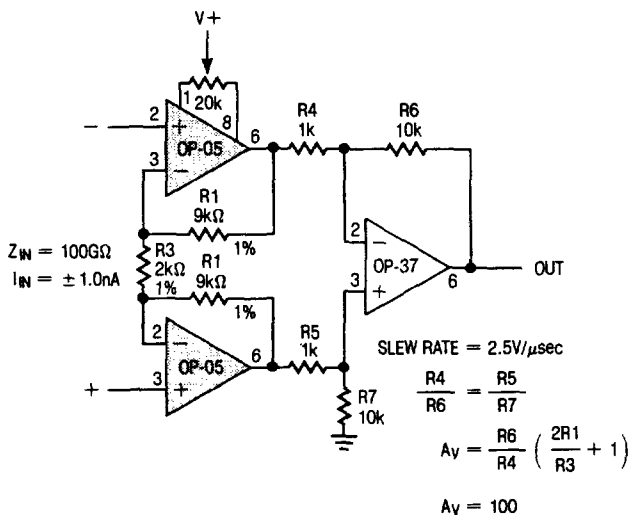
- Strain Gauges
- Thermocouple Amplifiers
- Instrumentation Amplifiers
- Medical Instruments

DESCRIPTION

The OP-05 is an internally compensated op-amp which provides excellent input offset voltage, low bias current, very high common mode rejection, and low offset voltage drift with temperature when the input offset voltage is externally trimmed to zero. Direct replacement of similar devices in existing systems can result in significant system performance improvement without redesign. The OP-05 is particularly well suited for instrumentation and low signal level applications where precision and stability over time and temperature are important. Internal frequency compensation enhances the OP-05's versatility for a wide variety of precision op-amp uses. Linear's advanced design, process and test techniques ensure device performance as well as reliability. An instrumentation amplifier application is shown below. For higher performance requirements see the LT1001 single precision op amp and the LT1002 dual matched precision op amp series.

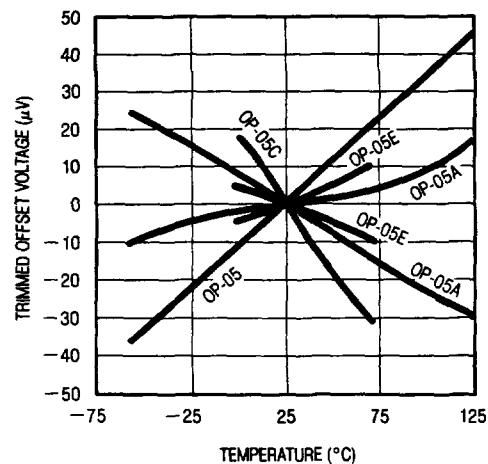
2

Instrumentation Amplifier



Trimmed Offset Voltage with Temperature of Six Representative Units

(Offset Trimmed to Zero at 25 $^{\circ}$ C with 20k Ω Pot)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 22V
Differential Input Voltage	± 30V
Input Voltage Equal to Supply Voltage	
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
OP-05/OP-05A	-55°C to 125°C
OP-05E/OP-05C	0°C to 70°C
Storage Temperature Range	
All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW OFFSET ADJUST	ORDER PART NO.	OFFSET VOLTAGE MAX
<p>METAL CAN H PACKAGE</p>	OP-05AH OP-05H OP-05EH OP-05CH	0.15mV 0.5mV 0.5mV 1.3mV
<p>HERMETIC J8 PACKAGE PLASTIC DIP N8 PACKAGE</p>	OP-05AJ8 OP-05J8 OP-05EJ8 OP-05CJ8 OP-05EN8 OP-05CN8	0.15mV 0.5mV 0.5mV 1.3mV 0.5mV 1.3mV

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			0.07	0.15		0.2	0.5	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.2	1.0		0.2	1.0	$\mu V/$ Month
I_{OS}	Input Offset Current			0.7	2.0		1.0	2.8	nA
I_B	Input Bias Current			± 0.7	± 2.0		± 1.0	± 3.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.35	0.6	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3 10.0 9.6	18.0 13.0 11.0		10.3 10.0 9.6	18.0 13.0 11.0	nV/\sqrt{Hz}
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		14	30	pA_{p-p}
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32 0.14 0.12	0.80 0.23 0.17		0.32 0.14 0.12	0.80 0.23 0.17	pA/\sqrt{Hz}
R_{in}	Input Resistance Differential Mode	(Note 3)	30	80		20	60		M Ω
	Input Resistance Common Mode			200			200		G Ω
	Input Voltage Range		± 13.5	± 14.0		± 13.5	± 14.0		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$	114	126		114	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	100	108		100	108		dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$ $R_L \geq 500\Omega, V_o = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)	300 150	500 500		200 150	500 500		V/mV
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		± 12.5 ± 12.0 ± 10.5	± 13.0 ± 12.8 ± 12.0		V
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)	0.1	0.3		0.1	0.3		V/ μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)	0.4	0.6		0.4	0.6		MHz
Z_o	Open Loop Output Impedance	$V_o = 0, I_o = 0, f = 10Hz$		60			60		Ω
P_d	Power Dissipation	No load $V_S = \pm 3V$, No load		90 4	120 6		90 4	120 6	mW
	Offset Adjustment Range	Null Pot = 20k Ω		± 4			± 4		mV

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05A			OP-05			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	0.10	0.24		0.3	0.7	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2)	●	0.3	0.9	●	0.7	2.0	$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	1.0	4.0		1.8	5.6	nA
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	5	25		8	50	pA/°C
I_B	Input Bias Current		●	± 1.0	± 4.0		± 2.0	± 6.0	nA
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	8	25		13	50	pA/°C
	Input Voltage Range		●	± 13.0	± 13.5		± 13.0	± 13.5	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	123		110	123	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	94	106		94	106	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$	●	200	400		150	400	V/mV
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6		± 12.0	± 12.6	V

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, T_A = 25^\circ C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage			0.2	0.5		0.3	1.3	mV
$\frac{\Delta V_{OS}}{\Delta Time}$	Long Term Input Offset Voltage Stability	(Notes 1 and 2)		0.3	1.5		0.4	2.0	$\mu V/$ Month
I_{OS}	Input Offset Current			1.2	3.8		1.8	6.0	nA
I_B	Input Bias Current			± 1.2	± 4.0		± 1.8	± 7.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.35	0.6		0.38	0.65	μV_{p-p}
	Input Noise Voltage Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		10.3	18.0		10.5	20.0	nV/ \sqrt{Hz}
				10.0	13.0		10.2	13.5	
				9.6	11.0		9.8	11.5	
i_n	Input Noise Current	0.1Hz to 10Hz (Note 2)		14	30		15	35	pA $_{p-p}$
	Input Noise Current Density	$f_o = 10Hz$ $f_o = 100Hz$ (Note 2) $f_o = 1000Hz$		0.32	0.80		0.35	0.90	pA/ \sqrt{Hz}
				0.14	0.23		0.15	0.27	
				0.12	0.17		0.13	0.18	
R_{in}	Input Resistance Differential Mode	(Note 3)		15	50		8	33	M Ω
	Input Resistance Common Mode				160			120	G Ω
	Input Voltage Range			± 13.5	± 14.0		± 13.5	± 14.0	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13.5V$		110	123		100	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$		94	106		90	104	dB
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$ $R_L \geq 500\Omega, V_O = \pm 0.5V$ $V_S = \pm 3V$ (Note 3)		200	500		120	400	V/mV
				150	500		100	400	
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$		± 12.5	± 13.0		± 12.0	± 13.0	V
				± 12.0	± 12.8		± 11.5	± 12.8	
				± 10.5	± 12.0		± 12.0		
SR	Slew Rate	$R_L \geq 2k\Omega$ (Note 2)		0.1	0.3		0.1	0.3	V/ μS
GBW	Closed Loop Bandwidth	$A_{VCL} = +1$ (Note 2)		0.4	0.6		0.4	0.6	MHz
Z_o	Open Loop Output Impedance	$V_O = 0, I_O = 0, f = 10Hz$			60			60	Ω
P_d	Power Dissipation	No load $V_S = \pm 3V$, No load		90	120		95	150	mW
				4	6		4	8	
	Offset Adjustment Range	Null Pot = 20k Ω		± 4			± 4		mW

See Notes on page 2-324

ELECTRICAL CHARACTERISTICS $V_s = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C.$

SYMBOL	PARAMETER	CONDITIONS	OP-05E			OP-05C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	0.25	0.6	0.35	1.6	mV	
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Input Offset Voltage Drift Without External Trim With External Trim	Null Pot = 20k Ω (Note 2)	●	0.7	2.0	1.3	4.5	$\mu V/^\circ C$	
			●	0.2	0.6	0.4	1.5		
I_{OS}	Input Offset Current		●	1.4	5.3	2.0	8.0	nA	
$\frac{\Delta I_{OS}}{\Delta Temp}$	Average Input Offset Current Drift	(Note 2)	●	8	35	12	50	$\mu A/^\circ C$	
I_B	Input Bias Current		●	± 1.5	± 5.5	± 2.2	± 9.0	nA	
$\frac{\Delta I_B}{\Delta Temp}$	Average Input Bias Current Drift	(Note 2)	●	13	35	18	50	$\mu A/^\circ C$	
	Input Voltage Range		●	± 13.0	± 13.5	± 13.0	± 13.5	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	107	123	97	120	dB	
PSRR	Power Supply Rejection Ratio	$V_s = \pm 3V$ to $\pm 18V$	●	90	103	86	100	dB	
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_o = \pm 10V$	●	180	450	100	400	V/mV	
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.0	± 12.6	± 11.0	± 12.6	V	

The ● denotes the specifications which apply over the full operating temperature range.

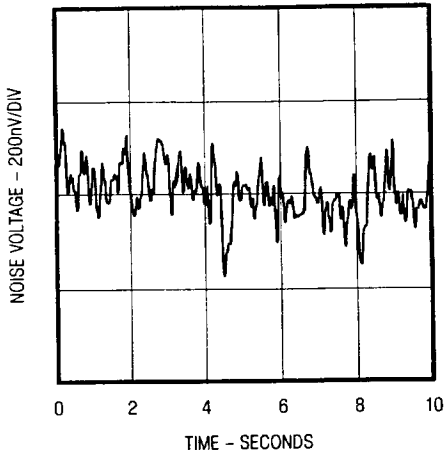
Note 1: Long term offset voltage stability is the average value of offset voltage vs. time plotted over extended periods following 30 days of operation. Values for time under 30 days of operation are typically $2.5\mu V$ following the first hour of operation.

Note 2: This parameter is sample tested.

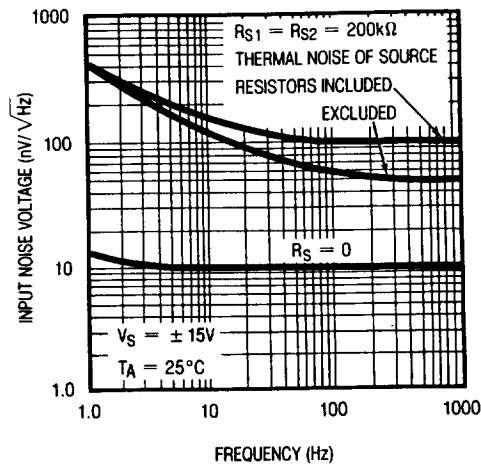
Note 3: This parameter is guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

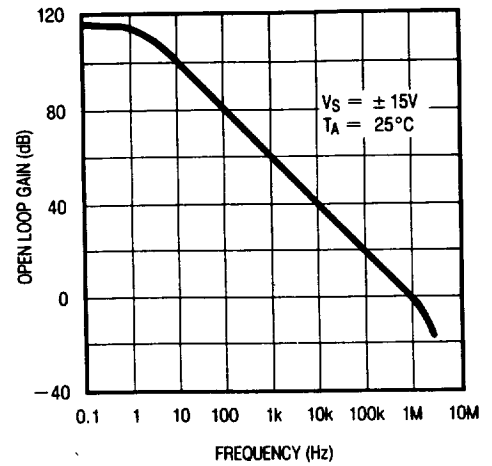
Low Frequency Noise
(Closed Loop Gain = 25,000)



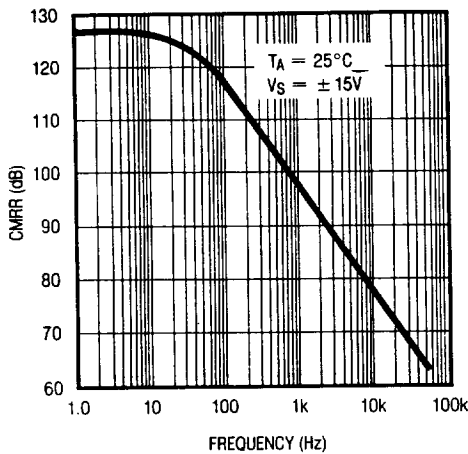
Total Input Noise Voltage vs Frequency



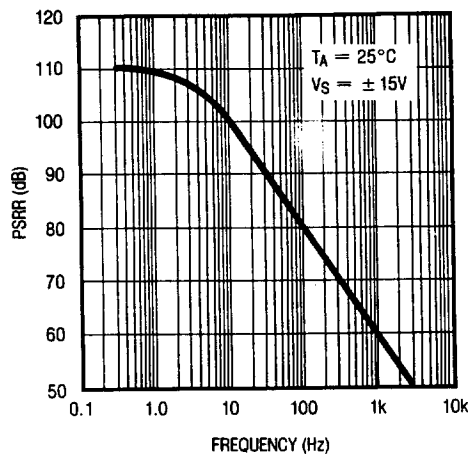
Open-Loop Frequency Response



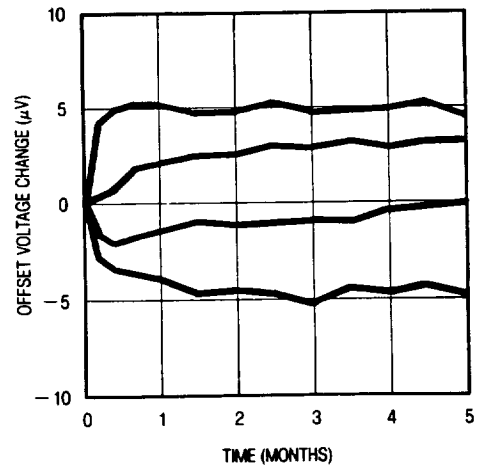
Common Mode Rejection Ratio vs Frequency



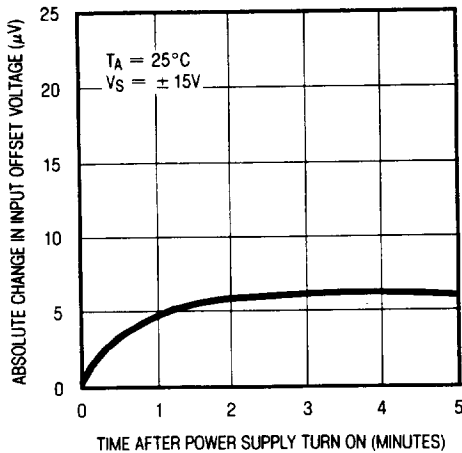
Power Supply Rejection Ratio vs Frequency



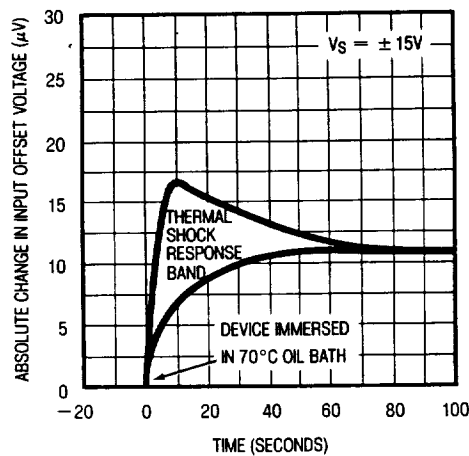
Long Term Stability of Four Representative Units



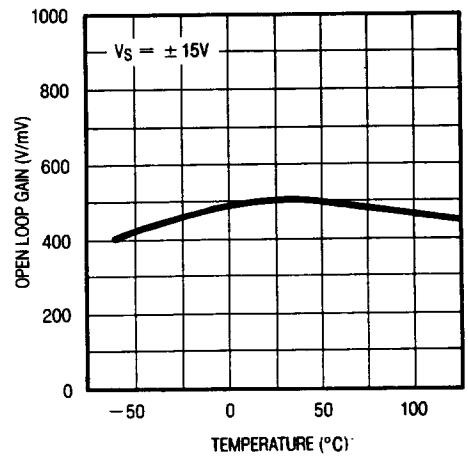
Warm-Up Drift



Offset Voltage Change Due to Thermal Shock

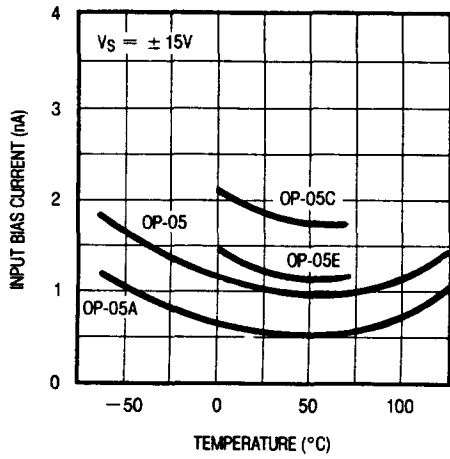


Open-Loop Gain vs Temperature

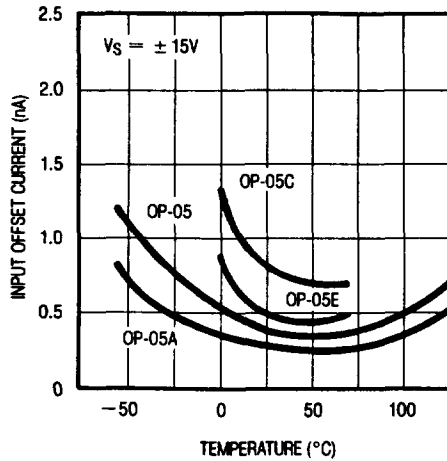


TYPICAL PERFORMANCE CHARACTERISTICS

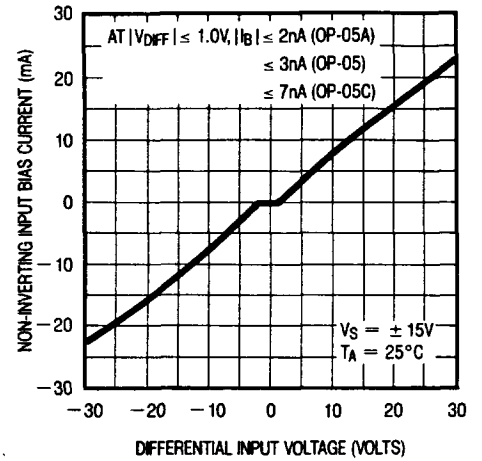
Input Bias Current vs Temperature



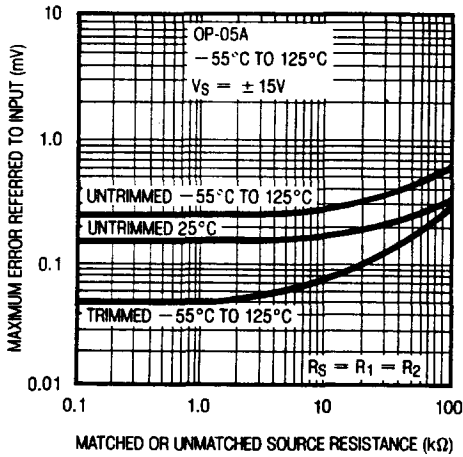
Input Offset Current vs Temperature



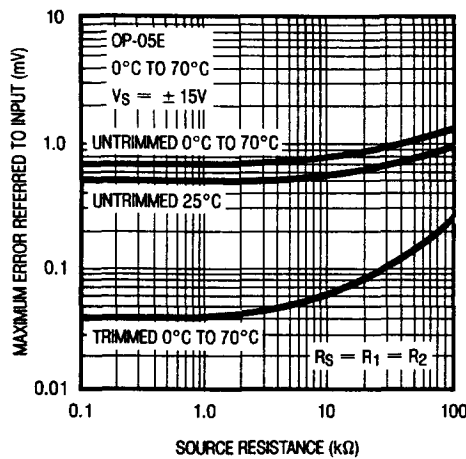
Input Bias Current vs Differential Input Voltage



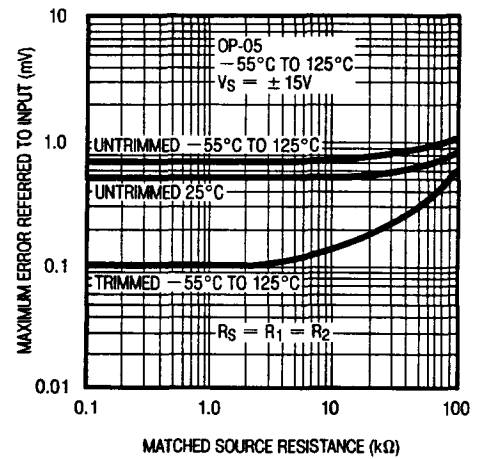
Maximum Error vs Source Resistance



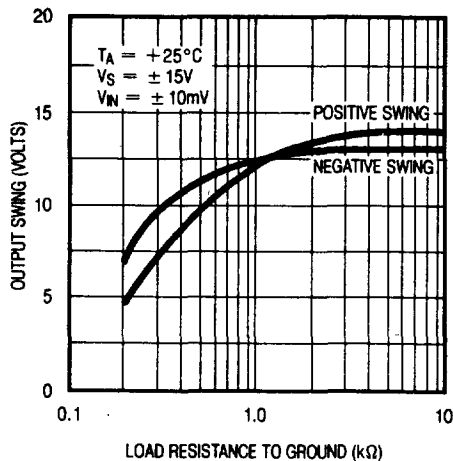
Maximum Error vs Source Resistance



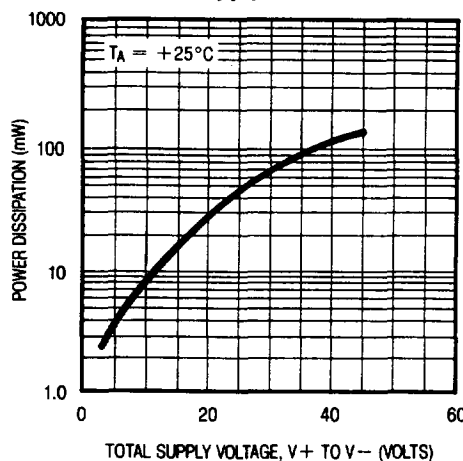
Maximum Error vs Source Resistance



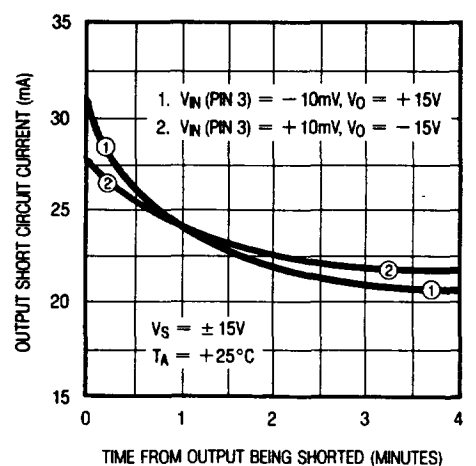
Output Voltage vs Load Resistance



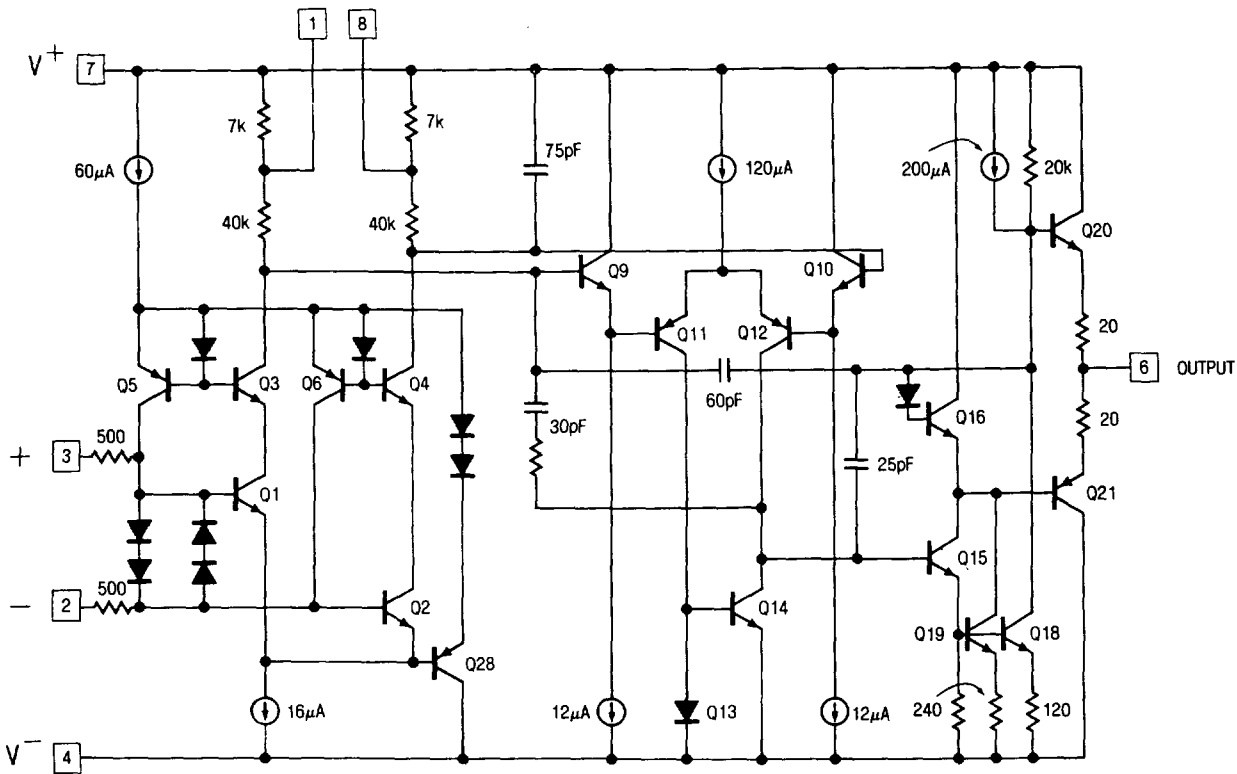
Power Consumption vs Power Supply



Output Short-Circuit Current vs Time



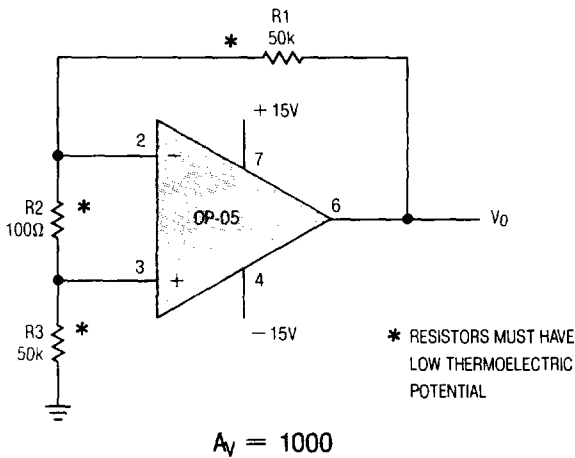
SCHEMATIC DIAGRAM



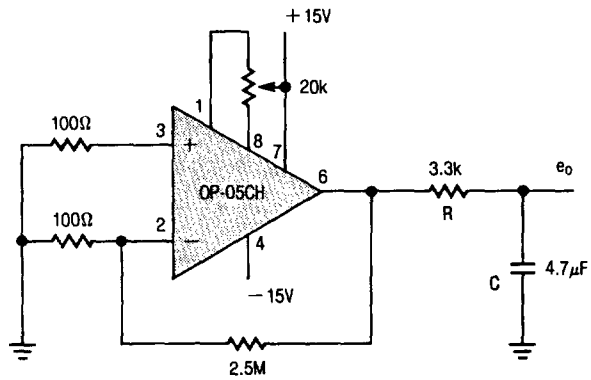
2

TEST CIRCUIT DIAGRAMS

Offset Voltage Test Circuit †



Offset Nulling and Low Frequency Noise Test Circuit



NOTES:

- 1) RC APPROXIMATELY 10Hz FILTER
- 2) OBSERVE OUTPUT FOR 10 SECONDS
AV = 25000

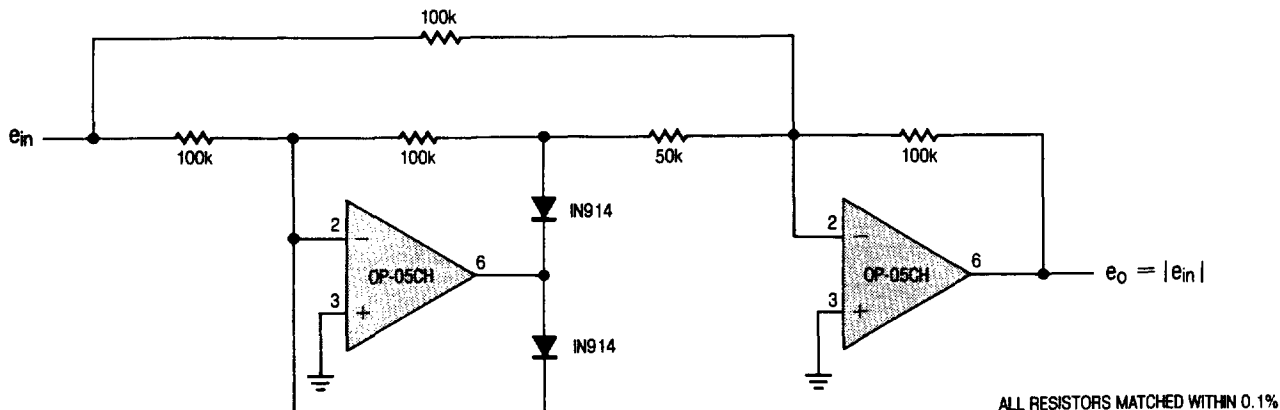
Application Tip

When the OP-05 is used as a replacement in 725, 108/108A, 308/308A applications, removal of external compensation is optional. For conventionally nulled 741 type applications, external trimming should be removed. Care should be taken to avoid thermocouple voltages caused by temperature variations between the input terminals or dissimilar metals.

† This circuit is also used as the burn-in configuration with supply voltages changed to ±20V, R1 = R3 = 10k, R2 = 200Ω, AV = 100.

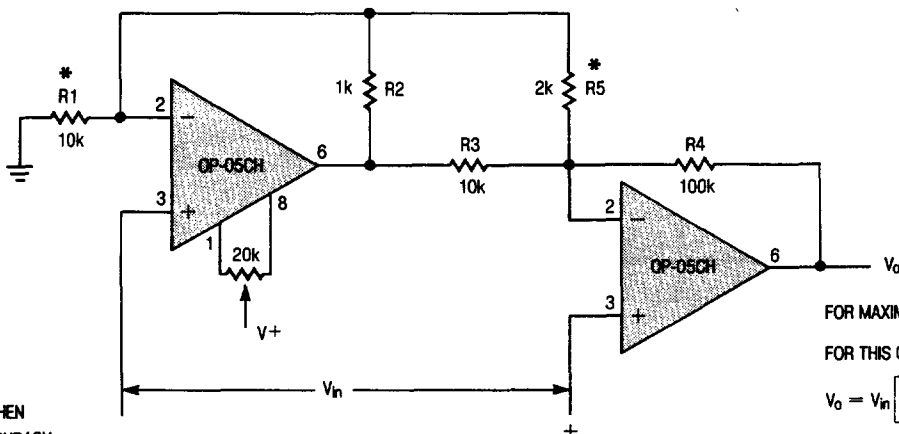
TYPICAL APPLICATIONS

Precision Absolute Value Circuit



ALL RESISTORS MATCHED WITHIN 0.1%

Two Op-Amp Instrumentation Amplifier



FOR MAXIMUM CMRR, $\frac{R2}{R1} = \frac{R3}{R4}$

FOR THIS CONDITION,

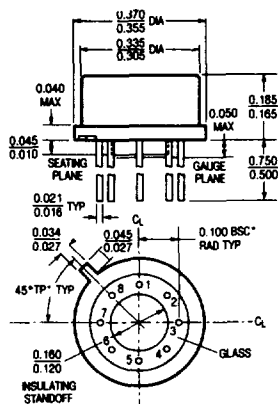
$$V_o = V_{in} \left[\frac{R4}{R3} \right] \left[1 + \frac{R2}{R1} + \frac{R2 + R3}{R5} \right]$$

$$\frac{V_o}{V_{in}} = 210 \text{ FOR VALUES SHOWN}$$

* ADJUST R1 FOR CMRR, THEN ADJUST R5 FOR GAIN ACCURACY. R5 DOES NOT AFFECT CMRR.

PACKAGE DESCRIPTION

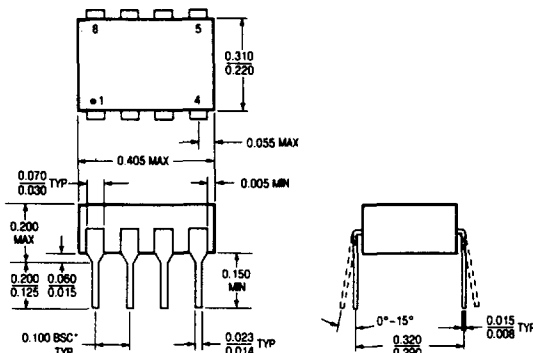
H Package
Metal Can



NOTE: DIMENSIONS IN INCHES

T_j max	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

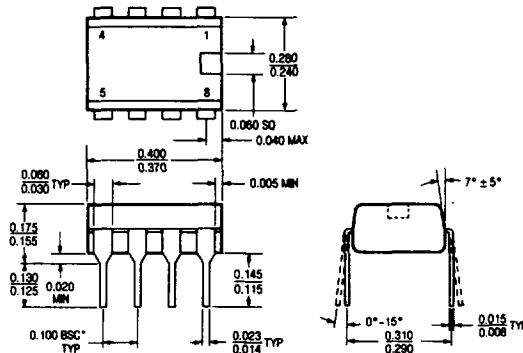
J8 Package
8 Lead Hermetic Dip



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE

T_j max	θ_{ja}
150°C	100°C/W

N8 Package
8 Lead Plastic



NOTE: DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED.
*LEADS WITHIN 0.007 OF TRUE POSITION (TP) AT GAUGE PLANE.

T_j max	θ_{ja}
100°C	130°C/W