Dual, Precision JFET High Speed Operational Amplifier

OP-249

FEATURES

- **Fast Slew Rate ..... 22V/μs Typ**
- **Settling Time (0.01%) ..... 1.2μs Max**
- **Offset Voltage ..... 300μV Max**
- **High Open-Loop Gain ..... 1000V/mV Min**
- **Low Total Harmonic Distortion ..... 0.002% Typ**
- **Improved Replacement for AD712, LT1057, OP-215, TL072, and MC34082**
- **Available in Die Form**

APPLICATIONS

- **Output Amplifier for Fast D/As**
- **Signal Processing**
- **Instrumentation Amplifiers**
- **Fast Sample/Holds**
- **Active Filters**
- **Low Distortion Audio Amplifiers**
- **Input Buffer for A/D Converters**
- **Servo Controllers**

GENERAL DESCRIPTION

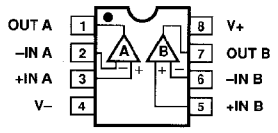
The OP-249 is a high-speed, precision dual JFET op amp, similar to the popular single op amp, the OP-42. The OP-249 outperforms available dual amplifiers by providing superior speed with excellent DC performance. Ultra-high open-loop gain (1kV/mV minimum), low offset voltage, and superb gain linearity, makes the OP-249 the industry's first true precision, dual high-speed amplifier.

With a slew rate of 22V/μs typical, and a fast settling time of less than 1.2μs maximum to 0.01%, the OP-249 is an ideal choice for high-speed bipolar D/A and A/D converter applications. The excellent DC performance of the OP-249 allows the full accuracy of high-resolution CMOS D/As to be realized.

Symmetrical slew rate, even when driving large loads, such as 600Ω, or 200pF of capacitance, and ultra-low distortion, make the OP-249 ideal for professional audio applications, active filters, high-speed integrators, servo systems, and buffer amplifiers.

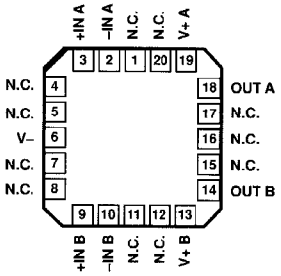
The OP-249 provides significant performance upgrades to the TL072, AD712, OP-215, MC34082 and the LT1057.

PIN CONNECTIONS

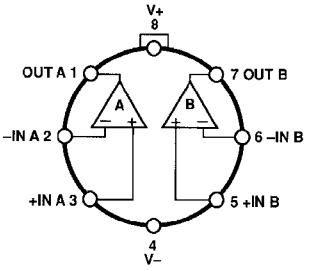


8-PIN CERDIP
(Z-Suffix)

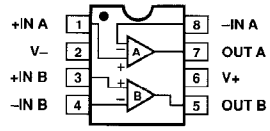
8-PIN EPOXY MINI-DIP
(P-Suffix)



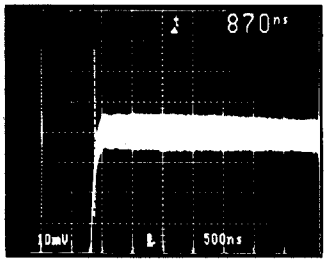
20-CONTACT LCC
(RC-Suffix)



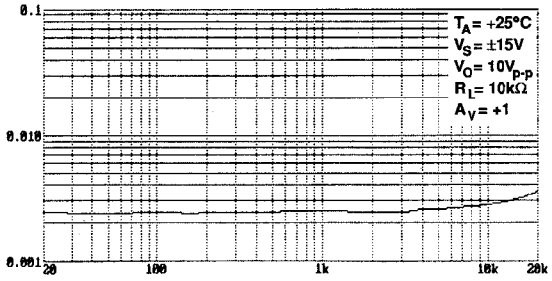
TO-99
(J-Suffix)



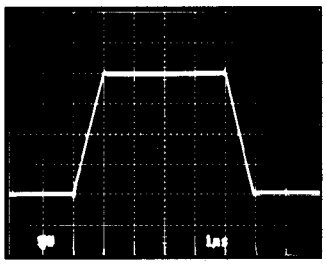
8-PIN SO
(S-Suffix)



FAST SETTLING
(0.01%)



LOW DISTORTION
A_V = +1, R_L = 10kΩ



EXCELLENT OUTPUT DRIVE
R_L = 600Ω

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

ORDERING INFORMATION †

PACKAGE				OPERATING TEMPERATURE RANGE
TO-99	CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-CONTACT	
OP249AJ*	OP249AZ*	–	OP249ARC/883	MIL
OP249EJ	–	–	–	XIND
OP249FJ	OP249FZ	–	–	XIND
–	–	OP249GP	–	XIND
–	–	OP249GS††	–	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

†† For availability and burn-in information on SO and PLCC packages, contact your local sales office.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... ±18V

Input Voltage (Note 2) ..... ±18V

Operating Temperature Range

OP-249A (J, Z, RC) ..... –55°C to +125°C

OP-249E,F (J, Z) ..... –40°C to +85°C

OP-249G (P, S) ..... –40°C to +85°C

Junction Temperature

OP-249 (J, Z, RC) ..... –65°C to +175°C

OP-249 (P, S) ..... –65°C to +150°C

Lead Temperature Range (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{jA} (Note 3)	Θ_{jC}	UNITS
TO-99 (J)	145	16	°C/W
8-Pin Hermetic DIP (Z)	134	12	°C/W
8-Pin Plastic DIP (P)	96	37	°C/W
20-Contact LCC (RC)	88	33	°C/W
8-Pin SO (S)	150	41	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. For supply voltages less than ±18V, the absolute maximum input voltage is

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	–	10^{12}||6	–	–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	–	35	–	–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	–	2	–	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz	–	75	–	–	75	–	–	75	–	$nV/\sqrt{Hz}$
		f_O = 100Hz	–	26	–	–	26	–	–	26	–	
		f_O = 1kHz	–	17	–	–	17	–	–	17	–	
		f_O = 10kHz	–	16	–	–	16	–	–	16	–	
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	–	0.003	–	–	0.003	–	$pA/\sqrt{Hz}$
Voltage Supply Range	V_S		±4.5	±15	±18	±4.5	±15	±18	±4.5	±15	±18	V

NOTES:
1 Long term offset voltage is guaranteed by a 1000 HR life test performed on 3 independent wafer lots at +125°C with a LTPD of 3.
2. Guaranteed by CMR test.
3. Settling-time is sample tested.
4. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	0.4	2.0	mV
Input Bias Current	I_B	V_{CM} = 0V, T_j = +25°C	–	40	75	pA
Input Offset Current	I_{OS}	V_{CM} = 0V, T_j = +25°C	–	10	25	pA
Input Voltage Range	IVR	(Note 1)	±11	+12.5 −12.0	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	90	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	12	50	µV/V
Large-Signal Voltage Gain	A_{VO}	V_O = ±10V R_L = 2kΩ	500	1100	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 −12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20	+36 −33	±50	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	mA
Slew Rate	SR	R_L = 2kΩ, C_L = 50pF	18	22	–	V/µs
Gain-Bandwidth Product	GBW	(Note 2)	–	4.7	–	MHz
Settling Time	t_s	10V Step 0.01%	–	0.9	1.2	µs
Phase Margin	Θ_0	0dB Gain	–	55	–	Deg

NOTES:
1. Guaranteed by CMR test.
2. Guaranteed by design.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Differential Input Impedance	Z_{IN}		–	10^{12}||6	–	Ω||pF
Open-Loop Output Resistance	R_O		–	35	–	Ω
Voltage Noise	$e_{n\ p\text{-}p}$	0.1Hz to 10Hz	–	2	–	$\mu V_{p\text{-}p}$
Voltage Noise Density	e_n	f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz	– – – –	75 26 17 16	– – – –	nV/√Hz
Current Noise Density	i_n	f_O = 1kHz	–	0.003	–	pA/√Hz
Voltage Supply Range	V_S		±4.5	±15	±18	V

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ +85°C for E/F grades, and –55°C ≤ T_A ≤ +125°C for A grade, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249A MIN	OP-249A TYP	OP-249A MAX	OP-249E MIN	OP-249E TYP	OP-249E MAX	OP-249F MIN	OP-249F TYP	OP-249F MAX	UNITS
Offset Voltage	V_{OS}		–	0.12	1.0	–	0.1	0.5	–	0.5	1.1	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	1	5	–	1	3	–	1.2	6	µV/°C
Input Bias Current	I_B	(Note 1)	–	4	20	–	0.25	3.0	–	0.3	4.0	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	4	–	0.01	0.7	–	0.02	1.2	nA
Input Voltage Range	IVR	(Note 2)	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	±11	+12.5 –12.5	–	V
Common-Mode Rejection	CMR	V_{CM} = ±11V	76	110	–	86	100	–	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±18V	–	5	50	–	5	50	–	7	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L = 2kΩ V_O = ±10V	500	1400	–	750	1400	–	250	1200	–	V/mV
Output Voltage Swing	V_O	R_L = 2kΩ	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	±12.0	+12.5 –12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±10	–	±60	±18	–	±60	±18	–	±60	mA
Supply Current	I_{SY}	No Load V_O = 0V	–	5.6	7.0	–	5.6	7.0	–	5.6	7.0	mA

NOTES:

1. T_j = 85°C for E/F Grades; T_j = 125°C for A Grade.
2. Guaranteed by CMR test.

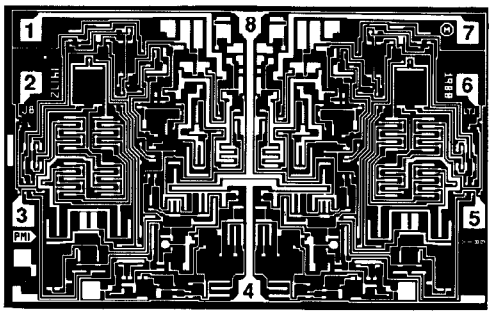
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-249G MIN	OP-249G TYP	OP-249G MAX	UNITS
Offset Voltage	V_{OS}		–	1.0	3.6	mV
Offset Voltage Temperature Coefficient	TCV_{OS}		–	6	25	µV/°C
Input Bias Current	I_B	(Note 1)	–	0.5	4.5	nA
Input Offset Current	I_{OS}	(Note 1)	–	0.04	1.5	nA
Input Voltage Range	IVR	(Note 2)	±11.0	+12.5 −12.5	–	V
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	76	95	–	dB
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	–	10.0	100	µV/V
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$ $V_O = \pm 10V$	250	1200	–	V/mV
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	+12.5 −12.5	–	V
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±18	–	±60	mA
Supply Current	I_{SY}	No Load $V_O = 0V$	–	5.6	7.0	mA

NOTES:

1. $T_j = 85°C$.
2. Guaranteed by CMR test.

DICE CHARACTERISTICS



1. OUT (A)
2. –IN (A)
3. +IN (A)
4. V–
5. +IN (B)
6. –IN (B)
7. OUT (B)
8. V+

DIE SIZE 0.072 x 0.112 inch, 8,064 sq. mils (1.83 x 2.84 mm, 5.2 sq. mm)

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_j = +25°C$, unless otherwise noted.

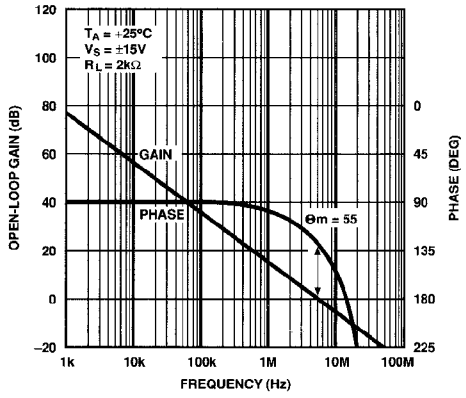
PARAMETER	SYMBOL	CONDITIONS	OP-249GBC LIMITS	UNITS
Offset Voltage	V_{OS}		0.5	mV MAX
Offset Voltage Temperature Coefficient	TCV_{OS}	$-40°C \le T_j \le 85°C$	6.0	µV/°C MAX
Input Bias Current	I_B	$V_{CM} = 0V$	225	pA MAX
Input Offset Current	I_{OS}	$V_{CM} = 0V$	75	pA MAX
Input Voltage Range	IVR	(Note 1)	±11	V MIN
Common-Mode Rejection	CMR	$V_{CM} = \pm 11V$	76	dB MIN
Power-Supply Rejection Ratio	PSRR	$V_S = \pm 4.5V$ to $\pm 18V$	100	µV/V MAX
Large-Signal Voltage Gain	A_{VO}	$R_L = 2k\Omega$	250	V/mV MIN
Output Voltage Swing	V_O	$R_L = 2k\Omega$	±12.0	V MIN
Short-Circuit Current Limit	I_{SC}	Output Shorted to Ground	±20/±60	mA MIN/MAX
Supply Current	I_{SY}	No Load $V_O = 0V$	7.0	mA MAX
Slew Rate	SR	$R_L = 2k\Omega$, $C_L = 50pF$	16.5	V/µs MIN

NOTES:
1. Guaranteed by CMR test.

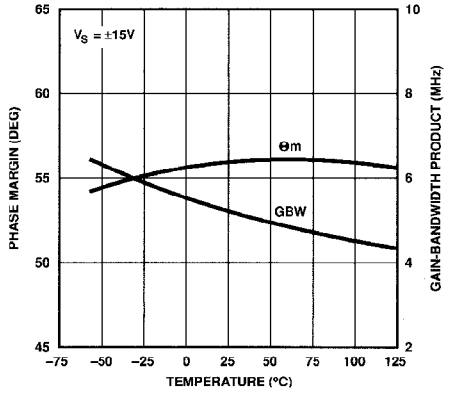
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

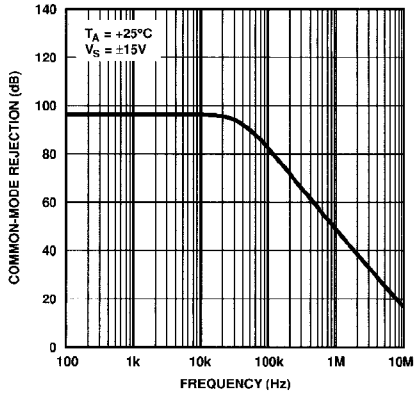
OPEN-LOOP GAIN, PHASE vs FREQUENCY



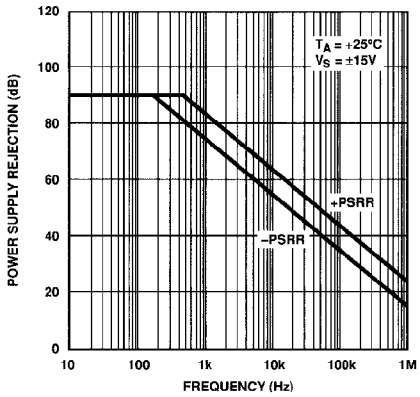
GAIN-BANDWIDTH PRODUCT, PHASE MARGIN vs TEMPERATURE



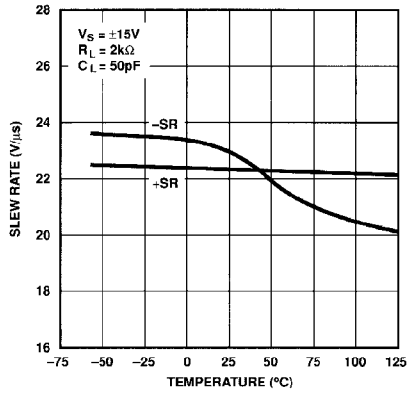
COMMON-MODE REJECTION vs FREQUENCY



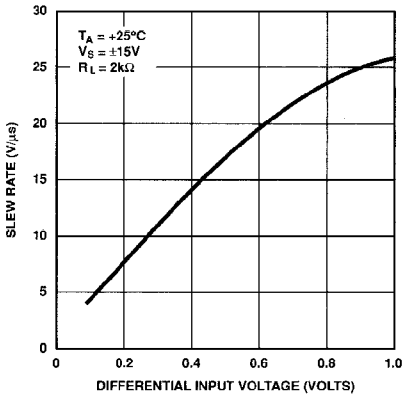
POWER SUPPLY REJECTION vs FREQUENCY



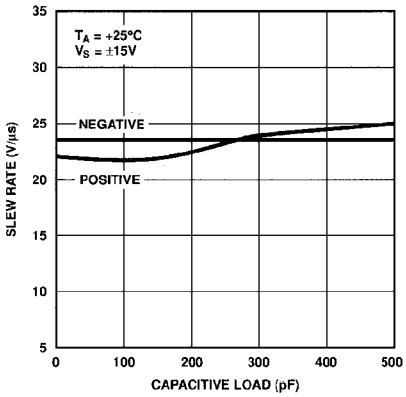
SLEW RATE vs TEMPERATURE



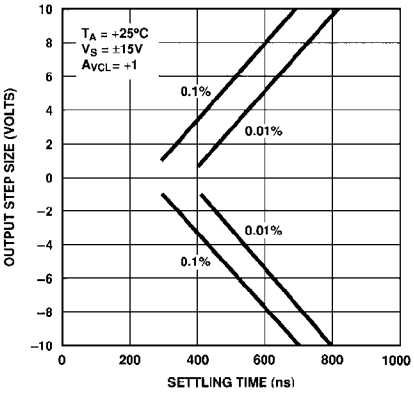
SLEW RATE vs DIFFERENTIAL INPUT VOLTAGE



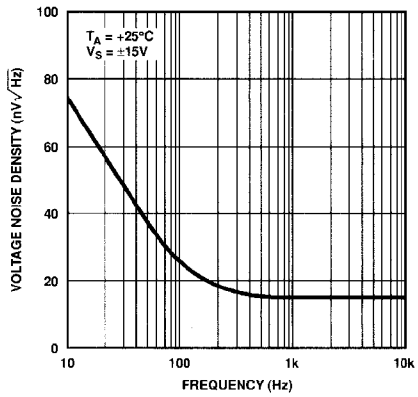
SLEW RATE vs CAPACITIVE LOAD



SETTLING TIME vs STEP SIZE

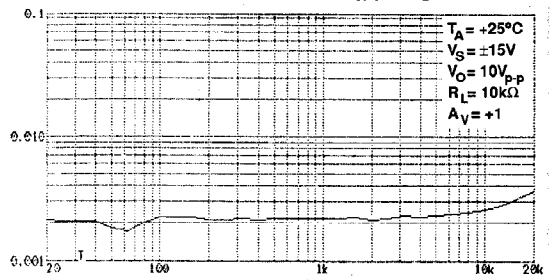


VOLTAGE NOISE DENSITY vs FREQUENCY

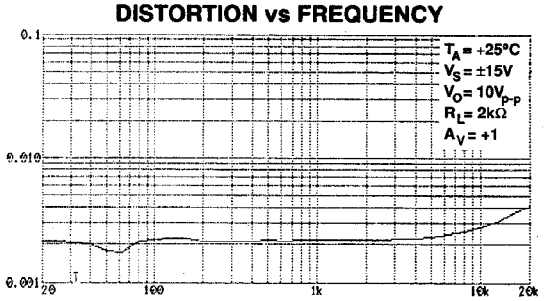


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

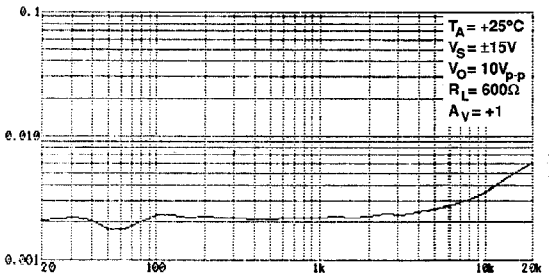
DISTORTION vs FREQUENCY



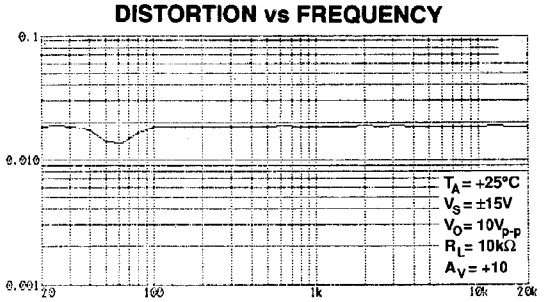
DISTORTION vs FREQUENCY



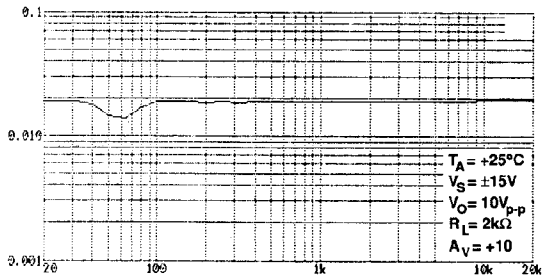
DISTORTION vs FREQUENCY



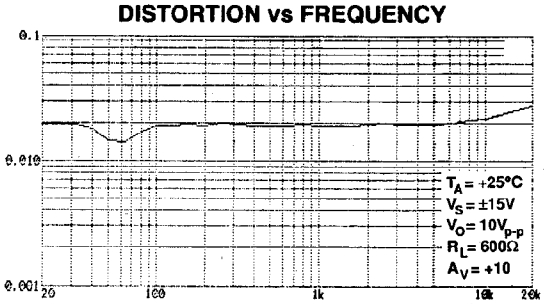
DISTORTION vs FREQUENCY



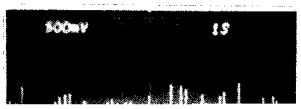
DISTORTION vs FREQUENCY



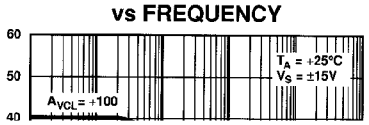
DISTORTION vs FREQUENCY



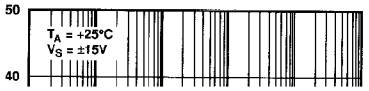
LOW FREQUENCY NOISE



CLOSED-LOOP GAIN vs FREQUENCY

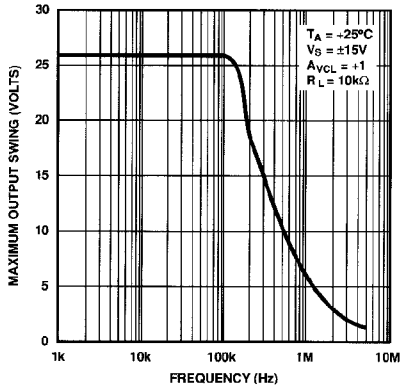


CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

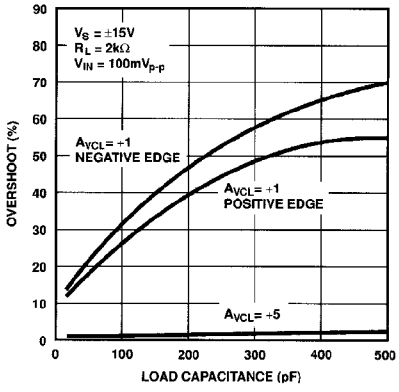


TYPICAL PERFORMANCE CHARACTERISTIC *Continued*

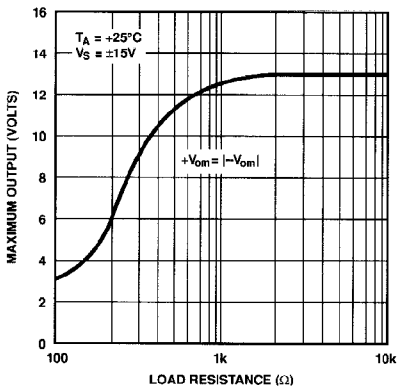
MAXIMUM OUTPUT SWING vs FREQUENCY



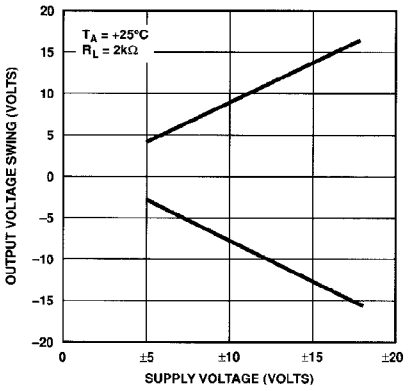
SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



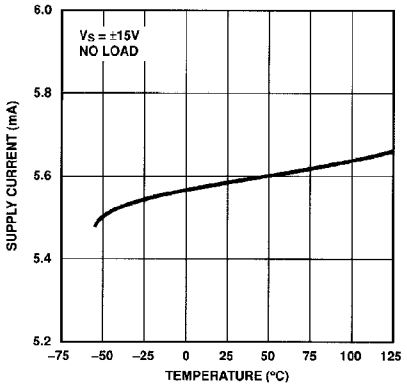
MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



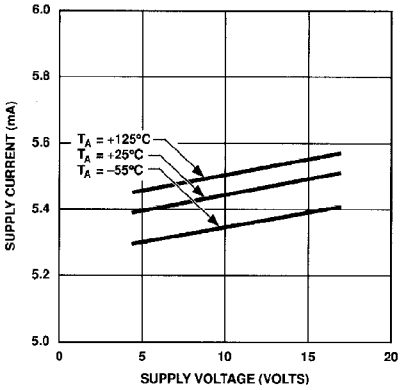
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE



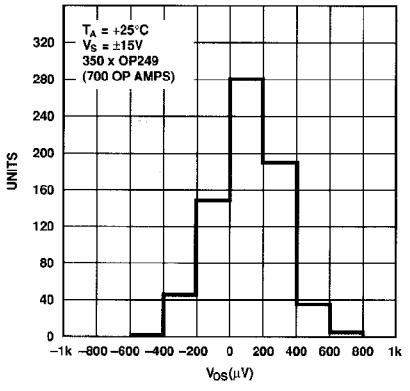
SUPPLY CURRENT vs TEMPERATURE



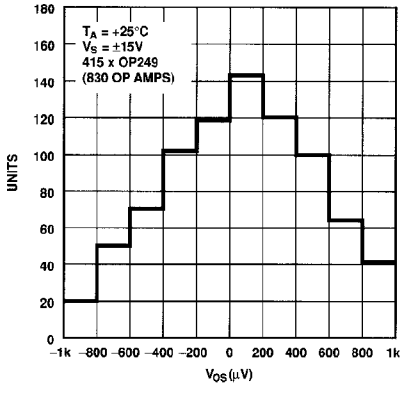
SUPPLY CURRENT vs SUPPLY VOLTAGE



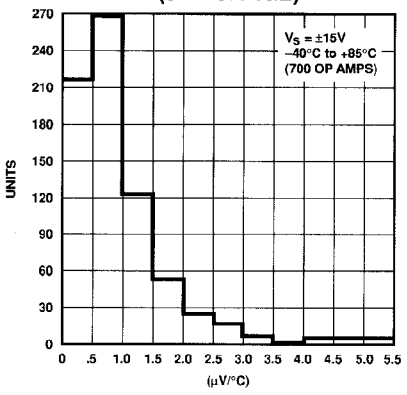
V_{OS} DISTRIBUTION (J PACKAGE)



V_{OS} DISTRIBUTION (P PACKAGE)

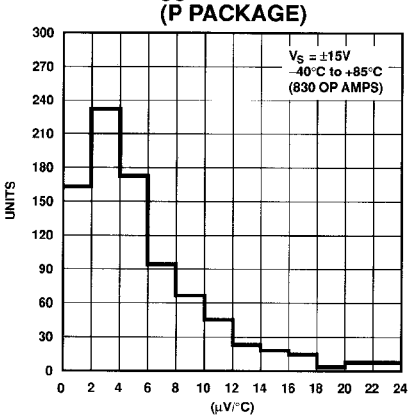


TCV_{OS} DISTRIBUTION (J PACKAGE)

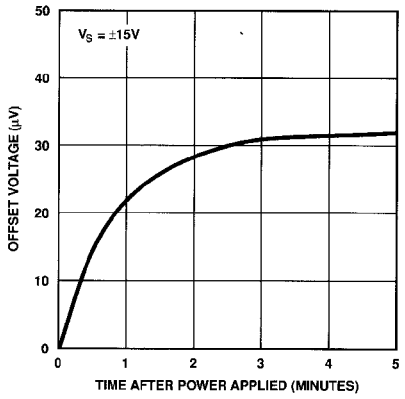


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

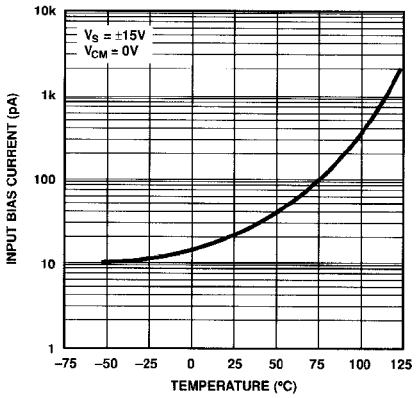
TCV_{OS} DISTRIBUTION (P PACKAGE)



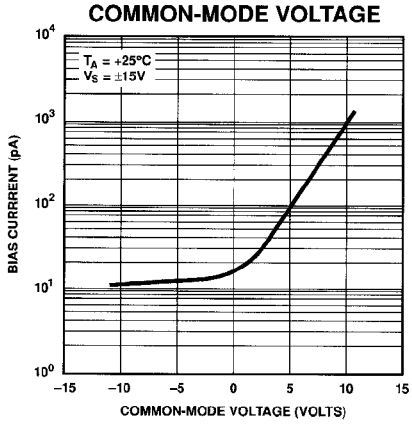
OFFSET VOLTAGE WARM-UP DRIFT



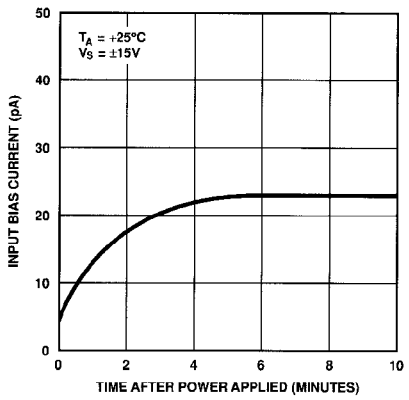
INPUT BIAS CURRENT vs TEMPERATURE



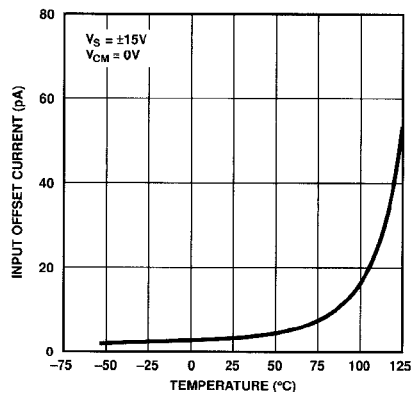
BIAS CURRENT vs COMMON-MODE VOLTAGE



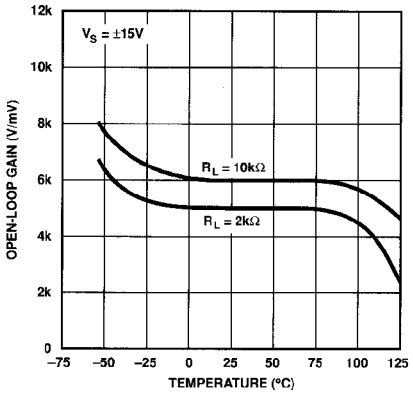
BIAS CURRENT WARM-UP DRIFT



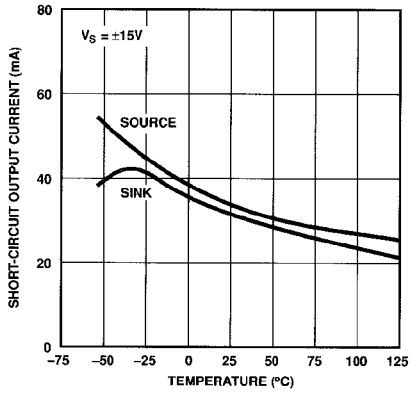
INPUT OFFSET CURRENT vs TEMPERATURE



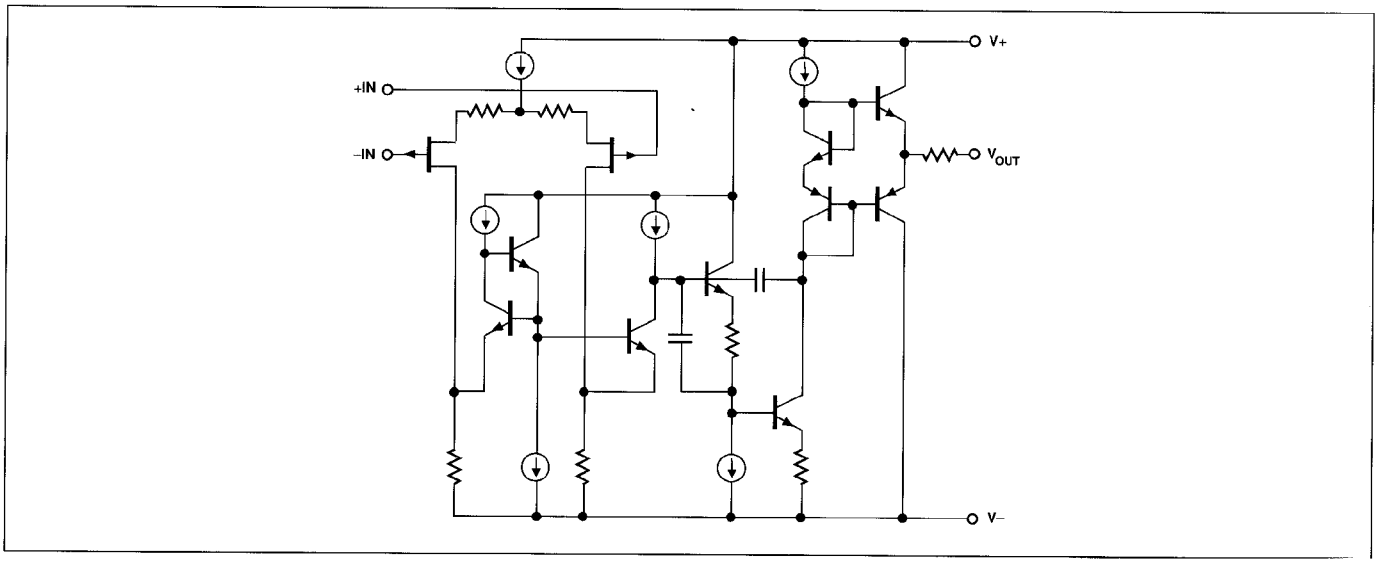
OPEN-LOOP GAIN vs TEMPERATURE



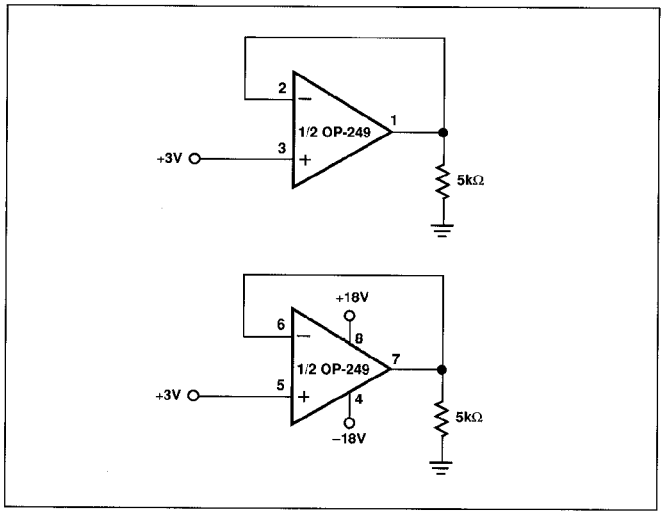
SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE



SIMPLIFIED SCHEMATIC (1/2 OP-249)



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

The OP-249 represents a reliable JFET amplifier design, featuring an excellent combination of DC precision and high speed. A rugged output stage provides the ability to drive a 600Ω load and still maintain a clean AC response. The OP-249 features a large-signal response that is more linear and symmetric than previously available JFET input amplifiers – compare the OP-249's large-signal reponse, as illustrated in Figure 1, to other industry standard dual JFET amplifiers.

Typically, JFET amplifier's slewing performance is simply specified as just a number of volts/µs. There is no discussion on the quality, i.e., linearity, symmetry, etc. of the slewing response.

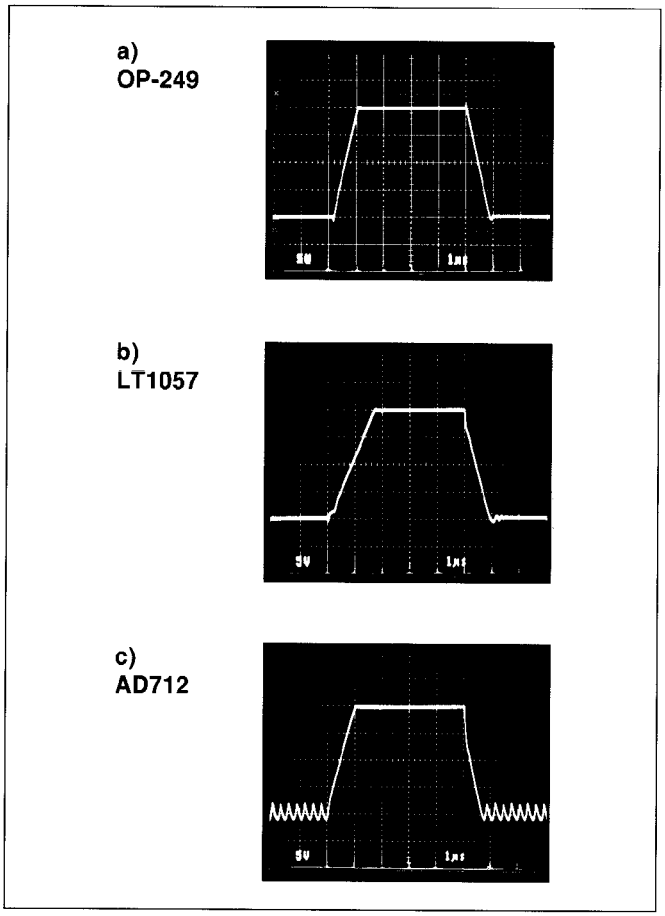


FIGURE 1: *Large-Signal Transient Response, $A_V = +1$, $V_{IN} = 20V_{p-p}$, $Z_L = 2k\Omega//200pF$, $V_S = \pm 15V$*

The OP-249 was carefully designed to provide symmetrically matched slew characteristics in both the negative and positive directions, even when driving a large output load.

An amplifier's slewing limitation determines the maximum frequency at which a sinusoidal output can be obtained without significant distortion. It is, however, important to note that the nonsymmetric slewing typical of previously available JFET amplifiers adds a higher series of harmonic energy content to the resulting response – and an additional DC output component. Examples of potential problems of nonsymmetric slewing behaviour could be in audio amplifier applications, where a natural, low-distortion sound quality is desired, and in servo or signal processing systems where a net DC offset cannot be tolerated. The linear and symmetric slewing feature of the OP-249 makes it an ideal choice for applications that will exceed the full-power-bandwidth range of the amplifier.

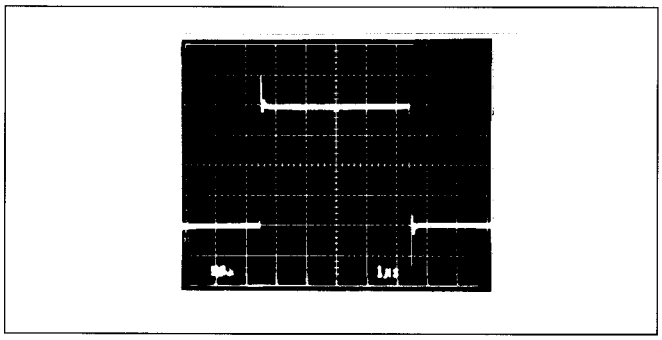


FIGURE 2: *Small-Signal Transient Response, A_V = +1, Z_L = 2kΩ//100pF, No Compensation, V_S = ±15V*

As with most JFET-input amplifiers, the output of the OP-249 may undergo phase inversion if either input exceeds the specified input voltage range. Phase inversion will not damage the amplifier, nor will it cause an internal latch-up condition.

Supply decoupling should be used to overcome inductance and resistance associated with supply lines to the amplifier. A 0.1µF and a 10µF capacitor should be placed between each supply pin and ground.

OPEN-LOOP GAIN LINEARITY

The OP-249 has both an extremely high open-loop gain of 1kV/mV minimum and constant gain linearity. This feature of the OP-249 enhances its DC precision, and provides superb accuracy in high closed-loop gain applications. Figure 3 illustrates the typical open-loop gain linearity – high gain accuracy is assured, even when driving a 600Ω load.

OFFSET VOLTAGE ADJUSTMENT

The inherent low offset voltage of the OP-249 will make offset adjustments unnecessary in most applications. However, where a lower offset error is required, balancing can be performed with simple external circuitry, as illustrated in Figures 4 and 5.

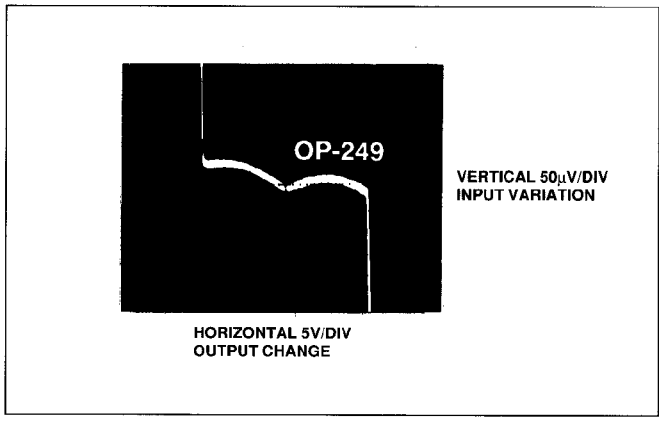


FIGURE 3: *Open-Loop Gain Linearity. Variation in Open-Loop Gain Results in Errors in High Closed-Loop Gain Circuits. R_L = 600Ω, V_S = ±15V*

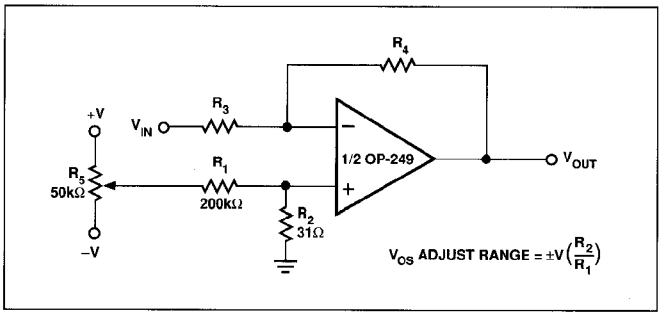


FIGURE 4: *Offset Adjust for Inverting Amplifier Configuration*

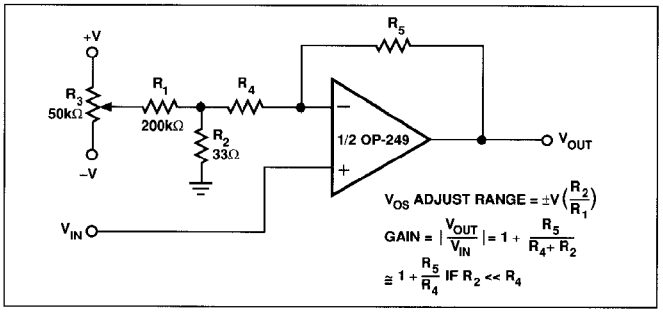


FIGURE 5: *Offset Adjust for Noninverting Amplifier Configuration*

In Figure 4, the offset adjustment is made by supplying a small voltage at the noninverting input of the amplifier. Resistors R_1 and R_2 attenuates the pot voltage, providing a ±2.5mV (with V_S = ±15V) adjustment range, referred to the input. Figure 5 illustrates offset adjust for the noninverting amplifier configuration, also providing a ±2.5mV adjustment range. As indicated in the equations in Figure 5, if R_4 is not much greater than R_2, there will be a resulting closed-loop gain error that must be accounted for.

SETTLING TIME

Settling time is the time between when the input signal begins to change and when the output permanently enters a prescribed error band. The error bands on the output are 5mV and 0.5mV, respectively, for 0.1% and 0.01% accuracy.

Figure 6 illustrates the OP-249's typical settling time of 870ns. Moreover, problems in settling response, such as thermal tails and long-term ringing are nonexistant.

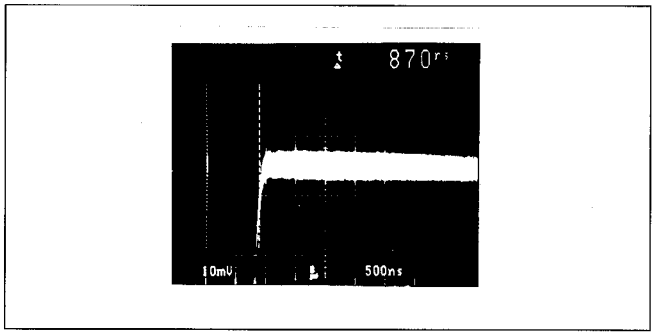


FIGURE 6: *Settling Characteristics of the OP-249 to 0.01%*

DAC OUTPUT AMPLIFIER

Unity-gain stability, a low offset voltage of 300µV typical, and a fast settling time of 870ns to 0.01%, makes the OP-249 an ideal amplifier for fast digital-to-analog converters.

For CMOS DAC applications, the low offset voltage of the OP-249 results in excellent linearity performance. CMOS DACs, such as the PM-7545, will typically have a code-dependent output resistance variation between 11kΩ and 33kΩ. The change in output resistance, in conjunction with the 11kΩ feedback resistor, will result in a noise gain change. This causes variations in the offset error, increasing linearity errors. The OP-249 features low offset voltage error, minimizing this effect and maintaining 12-bit linearity performance over the full scale range of the converter.

Since the DAC's output capacitance appears at the operational amplifiers inputs, it is essential that the amplifier is adequately compensated. Compensation will increase the phase margin, and ensure an optimal overall settling response. The required lead compensation is achieved with capacitor C in Figure 7.

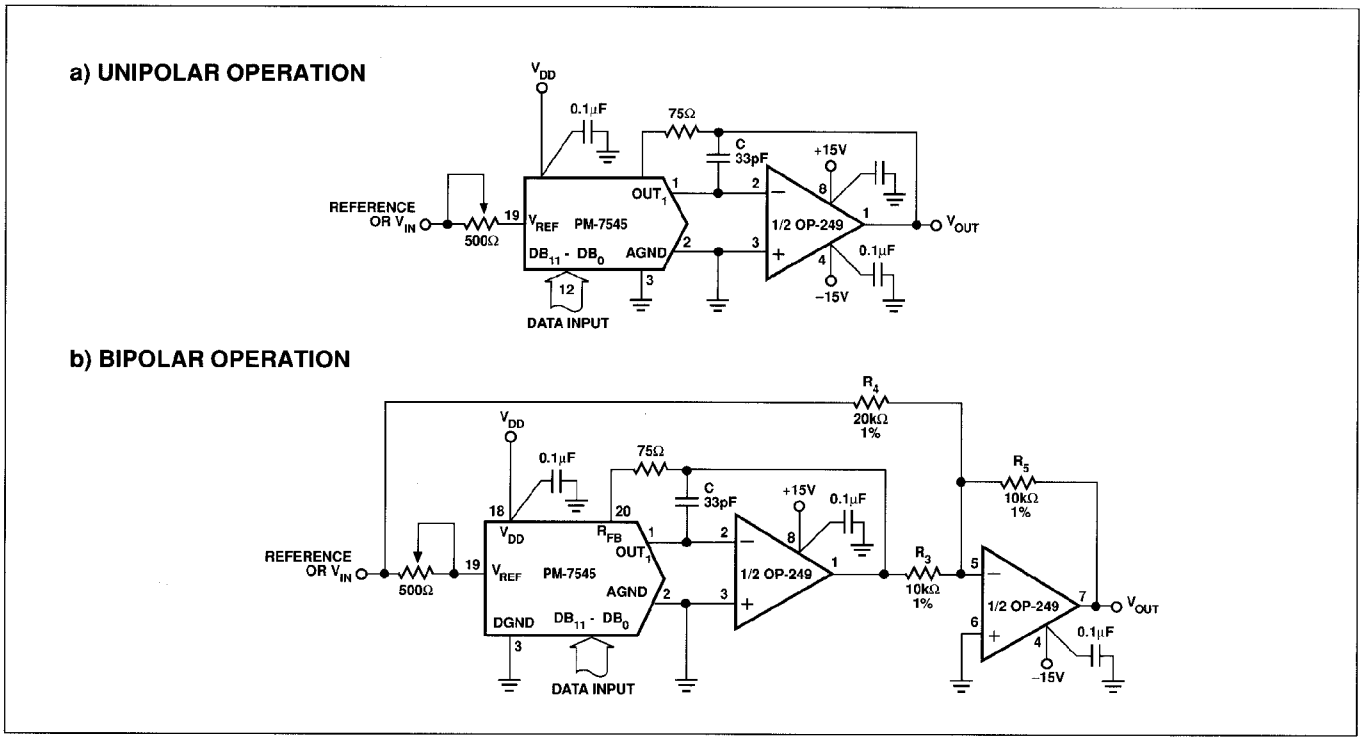


FIGURE 7: *Fast Settling and Low Offset Error of the OP-249 Enhances CMOS DAC Performance*

Figure 8 illustrates the effect of altering the compensation on the output response of the circuit in Figure 6a. Compensation is required to address the combined effect of the DAC's output capacitance, the op amp's input capacitance, and any stray capacitance. Slight adjustments to the compensation capacitor may be required to optimize settling response for any given application.

The settling time of the combination of the current output DAC and the op amp can be approximated by:

$$t_{S\ TOTAL} = \sqrt{(t_{S\ DAC})^2 + (t_{S\ AMP})^2}$$

The actual overall settling time is affected by the noise gain of the amplifier, the applied compensation, and the equivalent input capacitance at the amplifier's input.

DISCUSSION ON DRIVING A/D CONVERTERS

Settling characteristics of operational amplifiers also include an amplifier's ability to recover, i.e., settle, from a transient current output load condition. An example of this includes an op amp driving the input from a SAR type A/D converter. Although the comparison point of the converter is usually diode clamped, the input swing of plus-and-minus a diode drop still gives rise to a significant modulation of input current. If the closed-loop output impedance is low enough and bandwidth of the amplifier is sufficiently large, the output will settle before the converter makes a comparison decision which will prevent linearity errors or missing codes.

Figure 9 shows a settling measurement circuit for evaluating recovery from an output current transient. An output distrubing

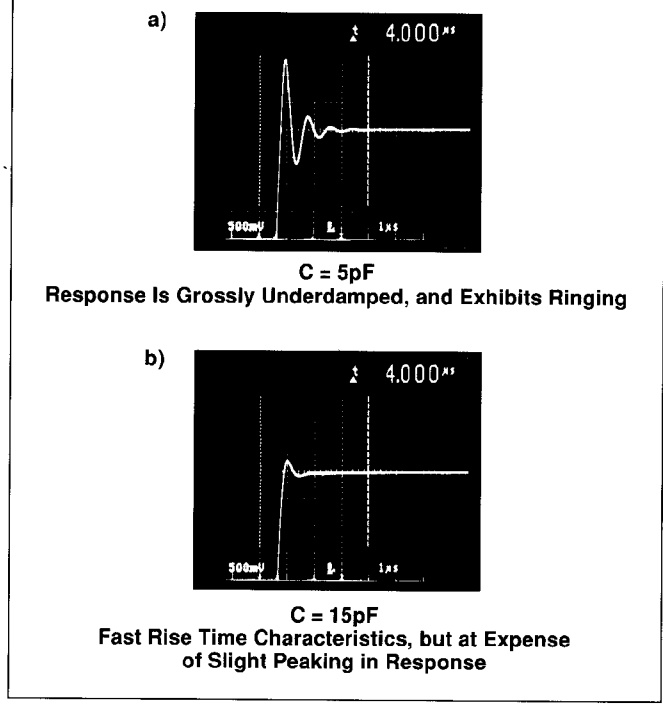


FIGURE 8: *Effect of Altering Compensation from Circuit in Figure 7a – PM-7545 CMOS DAC with 1/2 OP-249, Unipolar Operation. Critically Damped Response Will Be Obtained with C ≈ 33pF*

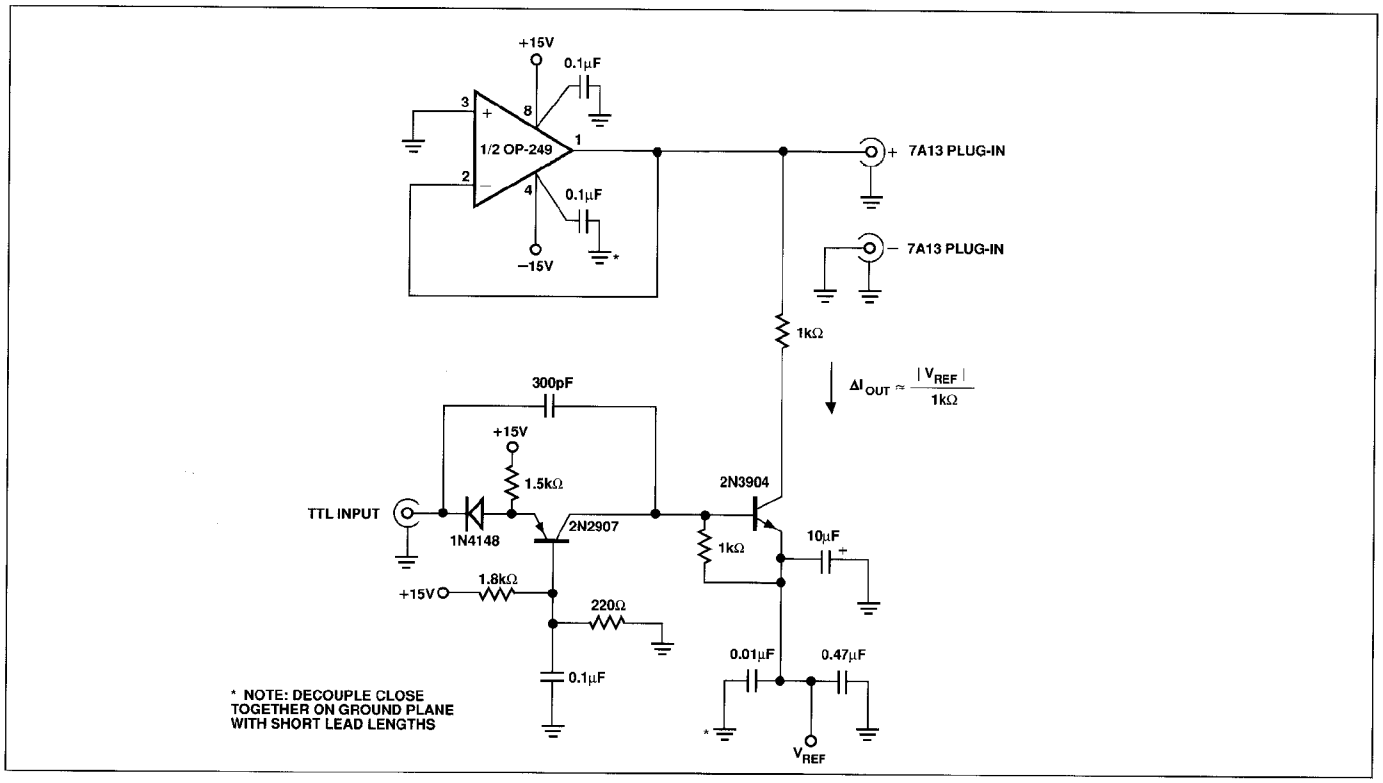


FIGURE 9: *Transient Output Impedance Test Fixture*

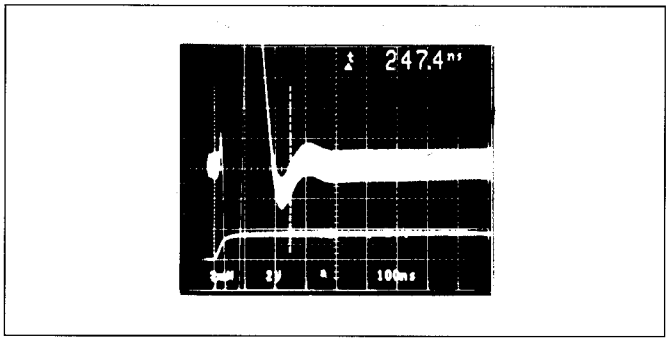


FIGURE 10: *OP-249's Transient Recovery Time from a 1mA Load Transient to 0.01%*

current generator provides the transient change in output load current of 1mA. As seen in Figure10, the OP-249 has extremely fast recovery of 274ns (to 0.01%), for a 1mA load transient. The performance makes it an ideal amplifier for data acquisition systems.

The combination of high speed and excellent DC performance of the OP-249 makes it an ideal amplifier for 12-bit data acquisition systems. Examining the circuit in Figure 11, one amplifier in the OP-249 provides a stable –5V reference voltage for the V_{REF} input of the ADC-912. The other amplifier in the OP-249 performs high-speed buffering of the A/D's input.

Examining the worst case transient voltage error (Figure 12) at the Analog In node of the A/D converter: the OP-249 recovers in less than 100ns. The fast recovery is due to both the OP-249's wide bandwidth and low DC output impedance.

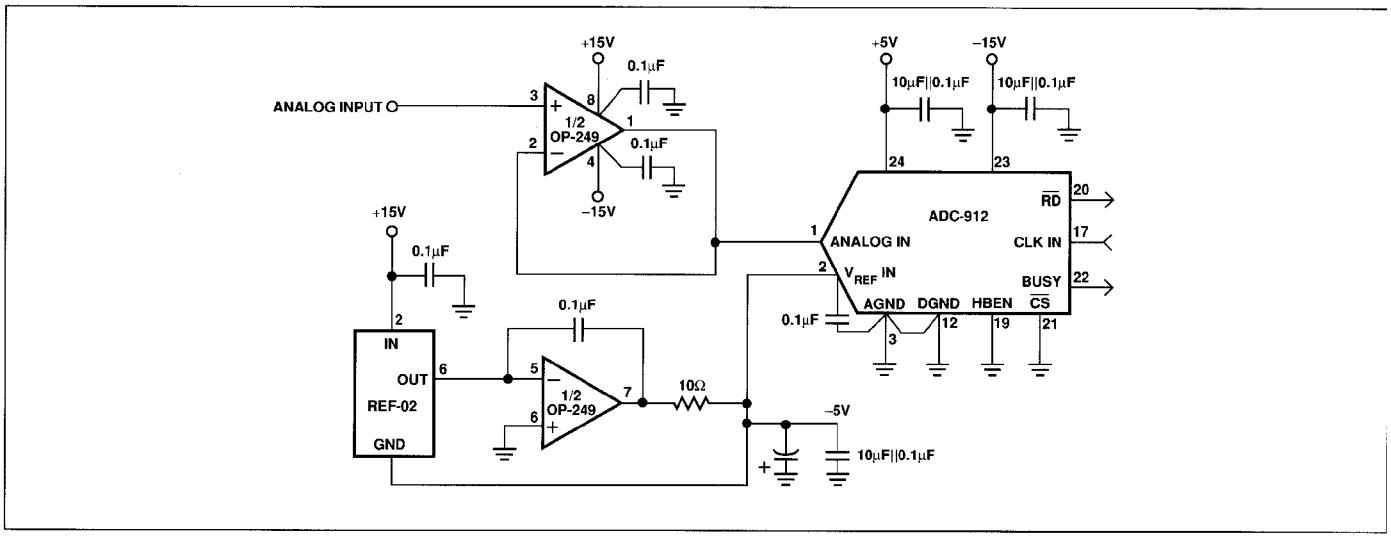


FIGURE 11: *OP-249 Dual Amplifiers Provide Both Stable –5V Reference Input, and Buffers Input to ADC-912*

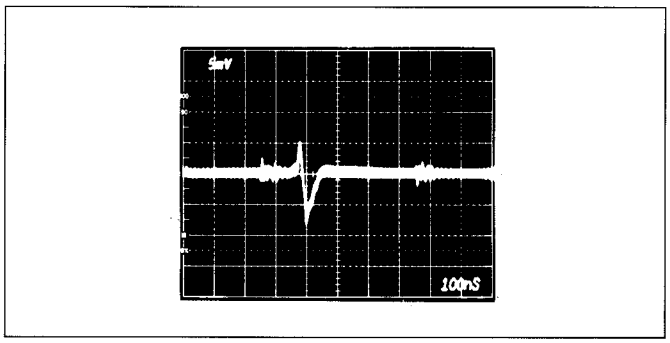


FIGURE 12: *Worst Case Transient Voltage, at Analog In, Occurs at the Half-Scale Point of the A/D. OP-249 Buffers the A/D Input from Figure 11, and Recovers in Less than 100ns*

OP-249 SPICE MACRO-MODEL

Figures 13 and 14 show the node and net list for a SPICE macro-model of the OP-249. The model is a simplified version of the actual device and simulates important DC parameters such as V_{OS}, I_{OS}, I_B, A_{VO}, CMR, V_O and I_{SY}. AC parameters such as slew rate, gain and phase reponse and CMR change with frequency are also simulated by the model.

The model uses typical parameters for the OP-249. The poles and zeros in the model were determined from the actual open and closed-loop gain and phase reponse of the OP-249. In this way the model presents an accurate AC representation of the actual device. The model assumes an ambient temperature of 25°C.

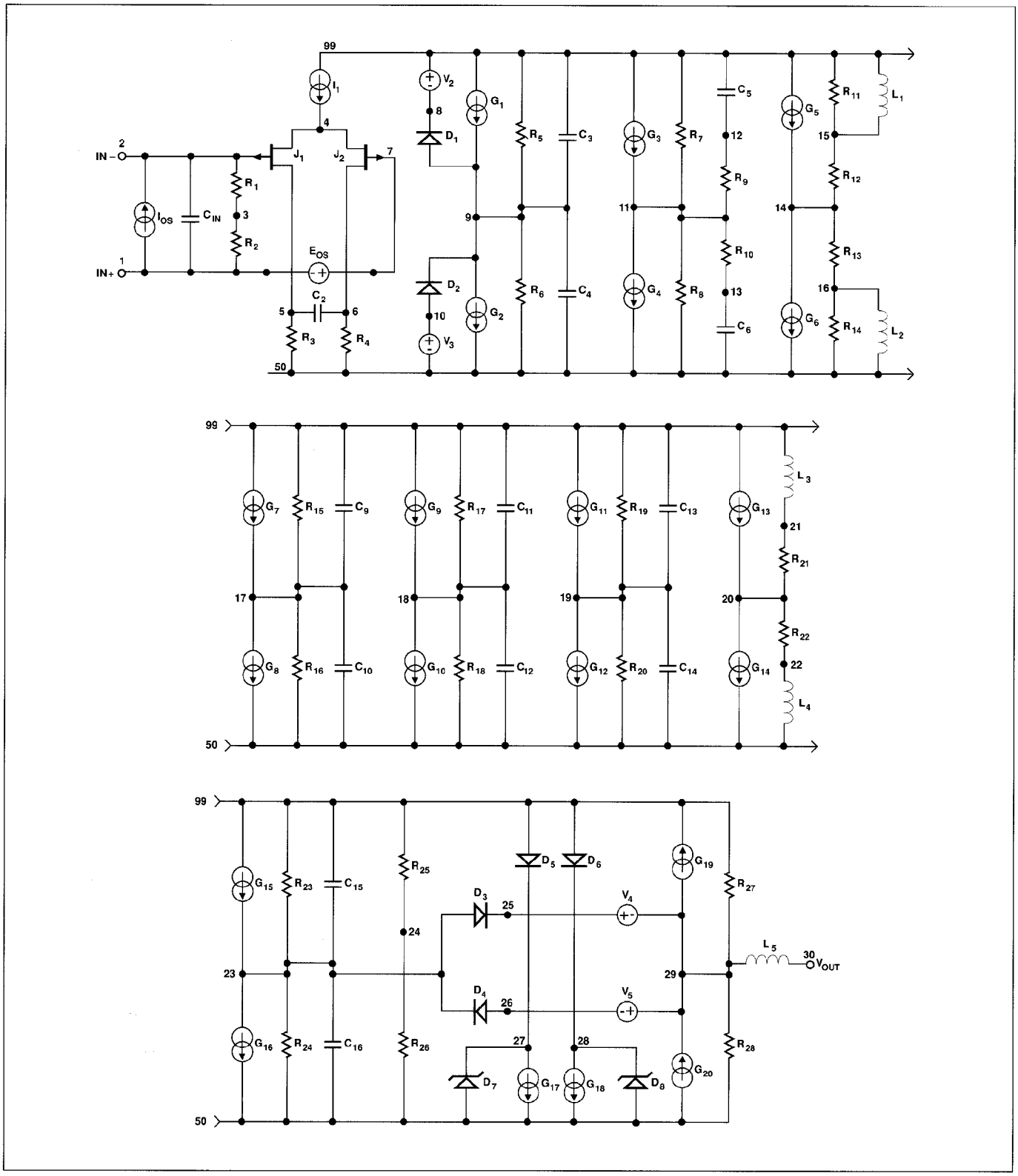


FIGURE 13: *OP-249 Macro-Model*

```
OP-249 MACRO-MODEL © PMI 1989
*
• subckt OP-249 1  2 30 99 50
*
INPUT STAGE & POLE AT 100MHz
*
r1   2   3        5E11
r2   1   3        5E11
r3   5   50       652.3
r4   6   50       652.3
cin  1   2        5E-12
c2   5   6        1.22E-12
i1   99  4        1E-3
ios  1   2        3.1E-12
eos  7   1        poly(1) 20 24 150E-6 1
j1   5   2   4    jx
j2   6   7   4    jx
*
* SECOND STAGE & POLE AT 12.2Hz
*
r5   9   99       326.1E6
r6   9   50       326.1E6
c3   9   99       40E-12
c4   9   50       40E-12
g1   99  9        poly(1) 5 6 4.25E-3 1.533E-3
g2   9   50       poly(1) 6 5 4.25E-3 1.533E-3
v2   99  8        2.9
v3   10  50       2.9
d1   9   8        dx
d2   10  9        dx
*
* POLE-ZERO PAIR AT 2MHz/4.0MHz
*
r7   11  99       1E6
r8   11  50       1E6
r9   11  12       1E6
r10  11  13       1E6
c5   12  99       37.79E-15
c6   13  50       37.79E-15
g3   99  11       9  24 1E-6
g4   11  50       24 9  1E-6
*
* ZERO-POLE PAIR AT 4MHz/8MHz
*
r11  99  15       1E6
r12  14  15       1E6
r13  14  16       1E6
r14  50  16       1E6
l1   99  15       19.89E-3
l2   50  16       19.89E-3
g5   99  14       11 24 1E-6
g6   14  50       24 11 1E-6
*
* POLE AT 20MHz
*
r15  17  99       1E6
*
* POLE AT 50MHz
*
r19  19  99       1E6
r20  19  50       1E6
c13  19  99       3.18E-15
c14  19  50       3.18E-15
g11  99  19       18 24 1E-6
g12  19  50       24 18 1E-6
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT 60kHz
*
r21  20  21       1E6
r22  20  22       1E6
l3   21  99       2.65
l4   22  50       2.65
g13  99  20       3  24 1.78E-11
g14  20  50       24 3  1.78E-11
*
* POLE AT 50MHz
*
r23  23  99       1E6
r24  23  50       1E6
c15  23  99       3.18E-15
c16  23  50       3.18E-15
g15  99  23       19 24 1E-6
g16  23  50       24 19 1E-6
*
* OUTPUT STAGE
*
r25  24  99       135E3
r26  24  50       135E3
r27  29  99       70
r28  29  50       70
l5   29  30       4E-7
g17  27  50       23 29 14.3E-3
g18  28  50       29 23 14.3E-3
g19  29  99       99 23 14.3E-3
g20  50  29       23 50 14.3E-3
v4   25  29       .4
v5   29  26       .4
d3   23  25       dx
d4   26  23       dx
d5   99  27       dx
d6   99  28       dx
d7   50  27       dy
d8   50  28       dy
*
* MODELS USED
*
• model jx PJF(BETA=1.175E-3  VTO=-2.000  IS=21E-12)
• model dx   D(IS=1E-15)
• model dy   D(IS=1E-15  BV=50)
• ends OP-249
```