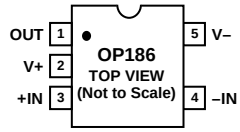
5 μA, Rail-to-Rail Output Operational Amplifier

OP186

FEATURES
Low Supply Current: 5.5 μA max
Single-Supply Operation: 2.2 V to 12 V
Wide Bandwidth: 160 kHz
Wide Input Voltage Range
Rail-to-Rail Output Swing
No Phase Reversal
Output Short Circuit Current: ±10 mA

APPLICATIONS
Portable Phones
Comparator
Battery Powered Instrumentation
Safety Monitoring
Remote Sensors
Low Voltage Strain Gauge Amplifiers

FUNCTIONAL BLOCK DIAGRAM
5-Lead SOT-23
(RT Suffix)



GENERAL DESCRIPTION

The OP186 is a single, low voltage, ultralow power single-supply, amplifier featuring rail-to-rail outputs. Specifications are guaranteed at +2.2 V, +2.7 V, and +5.0 V single supply as well as ±5 V dual supplies.

Fabricated on Analog Device's CBCMOS process, the OP186 features a bipolar input and an output that swings to within millivolts of the supplies while continuing to sink or source current all the way to the supplies.

Applications for these amplifiers include safety monitoring, portable equipment, battery and power supply control, and as signal conditioning and interface for transducers in very low power systems.

The output's ability to swing rail-to-rail and not increase supply current when the output is driven to a supply enables the OP186 to be used as a comparator in very low power systems.

The OP186 is specified over the extended industrial (–40°C to +125°C) temperature range. The OP186 is available in the SOT-23-5 package.

REV. 0

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OP186–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +2.2 V, V_{CM} = +1.1 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}[1]			0.8	5	mV
		0°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B			3	7	nA
		0°C ≤ T_A ≤ +125°C			10	nA
Input Offset Current	I_{OS}			0.1	2	nA
		0°C ≤ T_A ≤ +125°C			5	nA
Input Voltage Range	V_{CM}		0		1.2	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.2 V	65	90		dB
		0°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ , V_O = 0.3 V to 1.9 V	5	18		V/mV
		0°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			30		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.125	2.16		V
		0°C to +125°C	2.1			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		25	60	mV
		0°C to +125°C			75	mV
Short Circuit Limit	I_{SC}			±500		µA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.2 V to 12 V	78	95		dB
		0°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}			4	5	µA
		0°C ≤ T_A ≤ +125°C			5.5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 15 pF		60		V/ms
Turn-On Time		A_V = 1, V_O = 1		17		µs
		A_V = 20, V_O = 1		35		µs
Gain Bandwidth Product	GBP			150		kHz
Phase Margin	Φo			60		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		80		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

NOTE

[1]V_{OS} is tested under a no load condition.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = +2.7 V, V_{CM} = +1.35 V, T_A = +25°C unless otherwise noted)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}[2]			0.6	5	mV
		–40°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B			3	7	nA
		–40°C ≤ T_A ≤ +125°C			10	nA
Input Offset Current	I_{OS}			0.1	2	nA
		–40°C ≤ T_A ≤ +125°C			5	nA
Input Voltage Range	V_{CM}		0		1.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 1.7 V	65	90		dB
		–40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = 0.3 V to 2.4 V	5	22		V/mV
		–40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3.5		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			30		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.625	2.665		V
		–40°C to +125°C	2.6			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		22	50	mV
		–40°C to +125°C			75	mV
Short Circuit Limit	I_{SC}			±0.8		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	78	95		dB
		–40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}			4.2	5.5	µA
		–40°C ≤ T_A ≤ +125°C			7	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L =100 kΩ, C_L = 15 pF		61		V/ms
Turn-On Time		A_V = 1, V_O = 1		17		µs
		A_V = 20, V_O = 1		25		µs
Gain Bandwidth Product	GBP			155		kHz
Phase Margin	Φo			59		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 1 kHz		80		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

NOTES

[1]+2.7 V specifications are guaranteed by +2.2 V and ±5 V testing.

[2]V_{OS} is tested under a no load condition.

Specifications subject to change without notice.

OP186–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = +5.0 V, V_{CM} = +2.5 V, T_A = +25°C unless otherwise noted)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}[2]			0.6	5	mV
		–40°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B			3	7	nA
		–40°C ≤ T_A ≤ +125°C			10	nA
Input Offset Current	I_{OS}			0.1	2	nA
		–40°C ≤ T_A ≤ +125°C			5	nA
Input Voltage Range	V_{CM}		0		4	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4.0 V	65	90		dB
		–40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = 0.5 V to 4.5 V	5	40		V/mV
		–40°C ≤ T_A ≤ +125°C	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	–40°C ≤ T_A ≤ +125°C		3.3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			25		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.925	4.965		V
		–40°C ≤ T_A ≤ +125°C	4.9			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		20	50	mV
		–40°C ≤ T_A ≤ +125°C			75	mV
Short Circuit Limit	I_{SC}			±3.5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 12 V	78	95		dB
		–40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}			4.7	6	µA
		–40°C ≤ T_A ≤ +125°C			7.5	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 100 kΩ, C_L = 15 pF		62		V/ms
Gain Bandwidth Product	GBP			155		kHz
Phase Margin	Φo			59		Degrees
Saturation Recovery Time				60		µs
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		80		nV/√Hz
		f = 10 kHz		70		nV/√Hz
Current Noise Density	i_n			<1		pA/√Hz

NOTES

[1]+5 V specifications are guaranteed by +2.2 V and ±5 V testing.

[2]V_{OS} is tested under a no load condition.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = ±5.0 V, T_A = +25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}[1]			0.6	5	mV
		–40°C ≤ T_A ≤ +125°C			6	mV
Input Bias Current	I_B			3	7	nA
		–40°C ≤ T_A ≤ +125°C			10	nA
Input Offset Current	I_{OS}			0.1	2	nA
		–40°C ≤ T_A ≤ +125°C			5	nA
Input Voltage Range	V_{CM}		–5		+4	V
Common-Mode Rejection	CMRR	V_{CM} = –5.0 V to +4.0 V	65	90		dB
		–40°C ≤ T_A ≤ +125°C	60			dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 MΩ, V_O = ±4.0 V,	50	250		V/mV
		–40°C ≤ T_A ≤ +125°C	10			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			25		pA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			3		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing	V_O	R_L = 100 kΩ to GND	±4.95	±4.98		V
		–40°C to +125°C	±4.90			V
Short Circuit Limit	I_{SC}			±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.35 V to ±6 V	78	95		dB
		–40°C ≤ T_A ≤ +125°C	76			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		5.2	7	µA
		–40°C ≤ T_A ≤ +125°C			8	µA
DYNAMIC PERFORMANCE						
Slew Rate	±SR	R_L = 100 kΩ, C_L = 15 pF		62		V/ms
Gain Bandwidth Product	GBP			170		kHz
Phase Margin	Φo			58		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		6		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		80		nV/$\sqrt{Hz}$
		f = 10 kHz		70		nV/$\sqrt{Hz}$
Current Noise Density	i_n			<1		pA/$\sqrt{Hz}$

NOTE
[1]V_{OS} is tested under a no load condition.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . +16 V
Input Voltage . . . . . GND to V_S + 10 V
Differential Input Voltage[2] . . . . . ±3.5 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
RT Package . . . . . –65°C to +150°C
Operating Temperature Range
OP186G . . . . . –40°C to +125°C
Junction Temperature Range
RT Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]For supplies less than ±5 V the differential input voltage is limited to the supplies.

Package Type	θ_{JA}[1]	θ_{JC}	Units
5-Lead SOT-23 (RT)	230	140	°C/W

NOTE
[1]θ_{JA} is specified for worst case conditions, i.e., θ_{JA} is specified for device in socket for SOT packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP186GRT	–40°C to +125°C	5-Lead SOT-23	RT-5

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP186 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

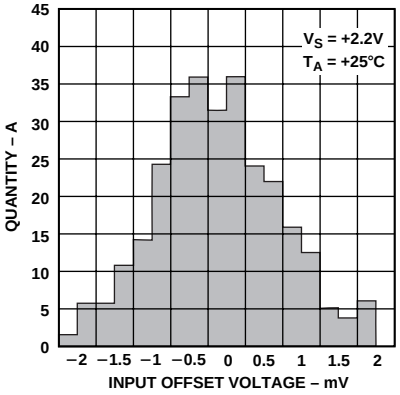


Figure 1. Input Offset Voltage Distribution

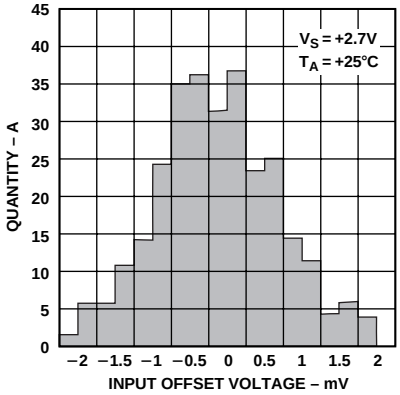


Figure 2. Input Offset Voltage Distribution

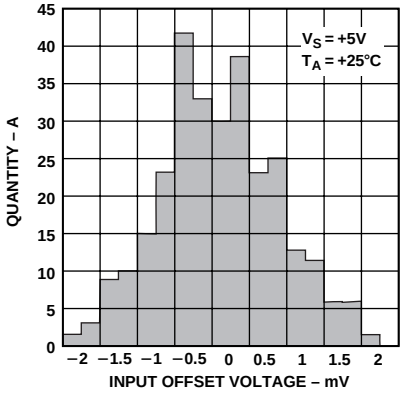


Figure 3. Input Offset Voltage Distribution

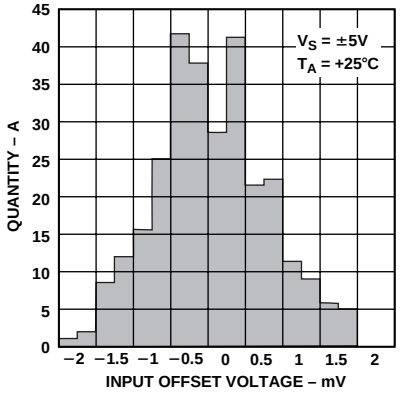


Figure 4. Input Offset Voltage Distribution

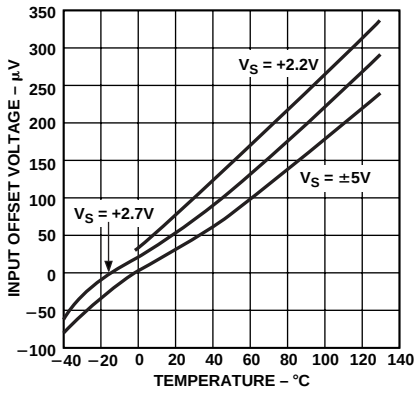


Figure 5. Input Offset Voltage vs. Temperature

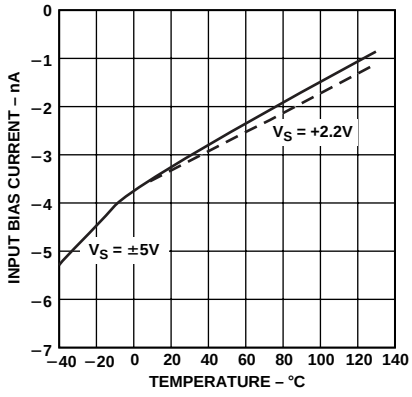


Figure 6. Input Bias Current vs. Temperature

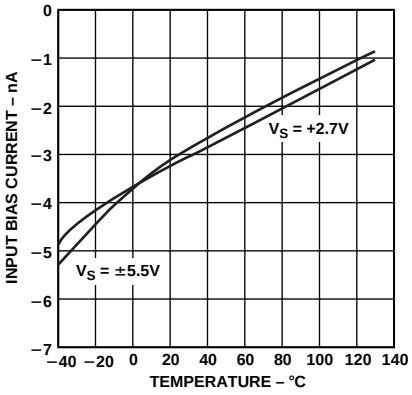


Figure 7. Input Bias Current vs. Temperature

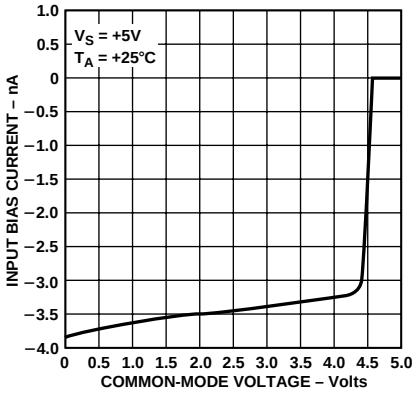


Figure 8. Input Bias Current vs. Common-Mode Voltage

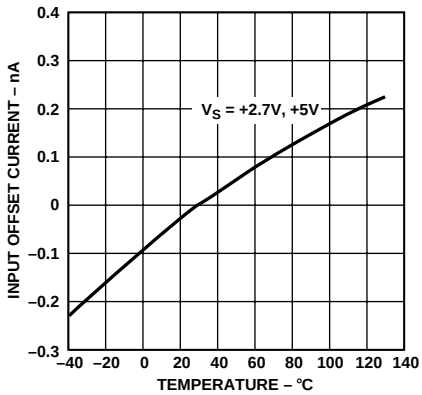


Figure 9. Input Offset Current vs. Temperature

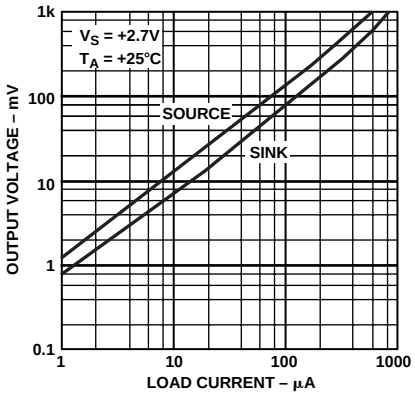


Figure 10. Output Voltage to Supply Rail vs. Load Current

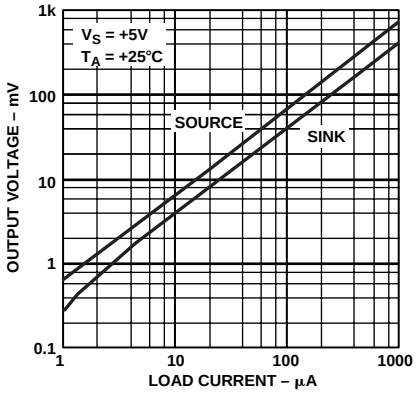


Figure 11. Output Voltage to Supply Rail vs. Load Current

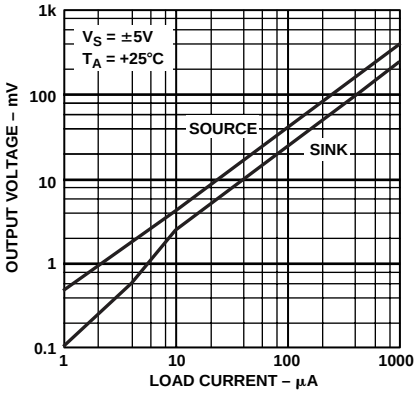


Figure 12. Output Voltage to Supply Rail vs. Load Current

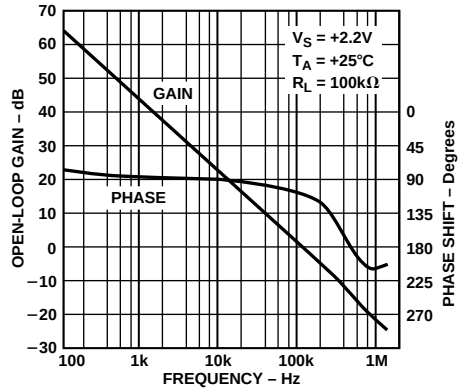


Figure 13. Open-Loop Gain and Phase vs. Frequency

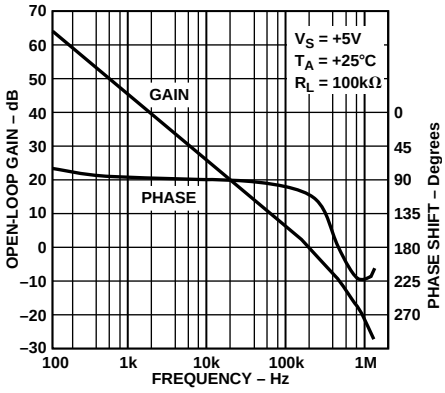


Figure 14. Open-Loop Gain and Phase vs. Frequency

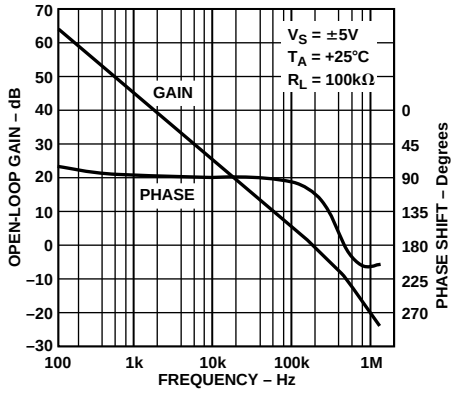


Figure 15. Open-Loop Gain and Phase vs. Frequency

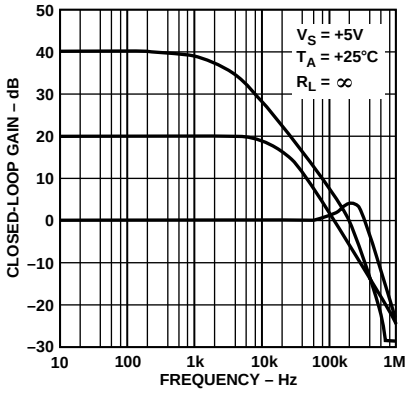


Figure 16. Closed-Loop Gain vs. Frequency

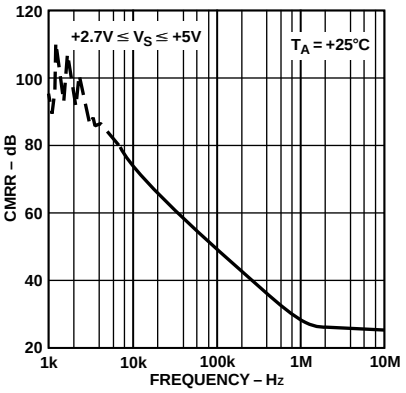


Figure 17. CMRR vs. Frequency

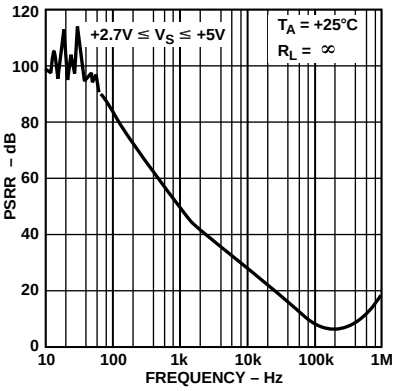


Figure 18. PSRR vs. Frequency

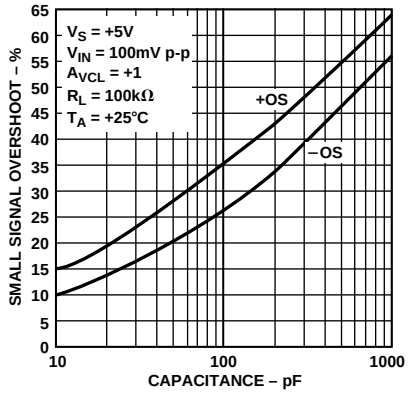


Figure 19. Small Signal Overshoot vs. Load Capacitance

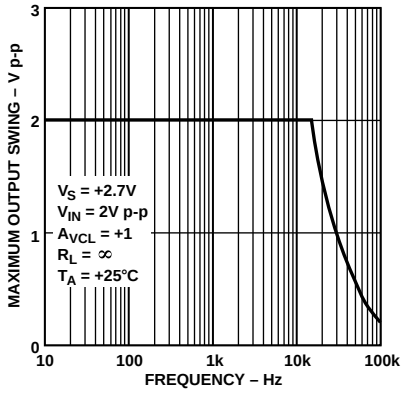


Figure 20. Maximum Output Swing vs. Frequency

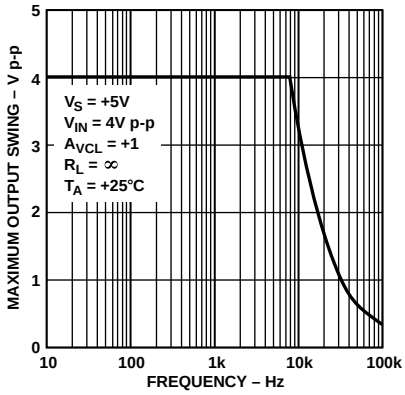


Figure 21. Maximum Output Swing vs. Frequency

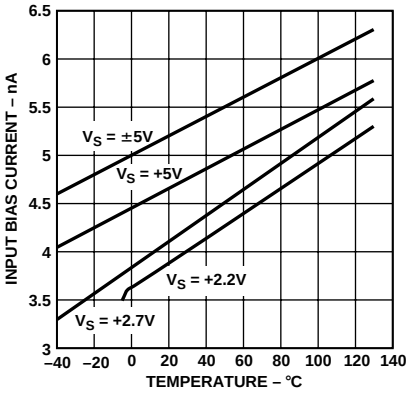


Figure 22. Bias Current vs. Temperature

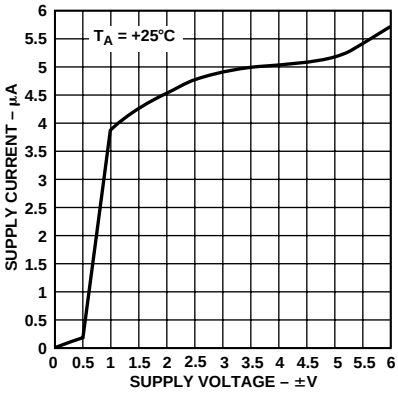


Figure 23. Supply Current vs. Supply Voltage

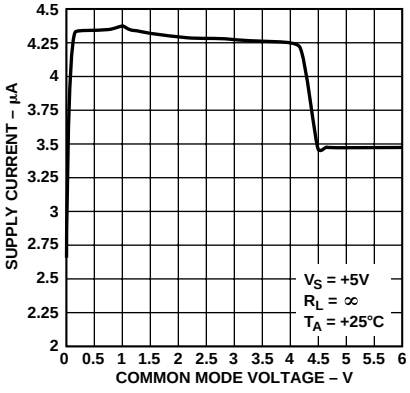


Figure 24. Supply Current vs. Common-Mode Voltage

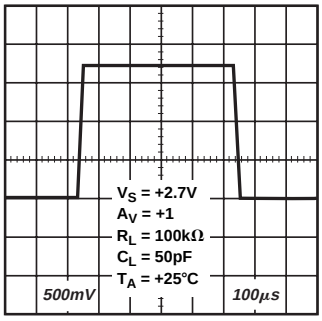


Figure 25. Large Signal Transient Response

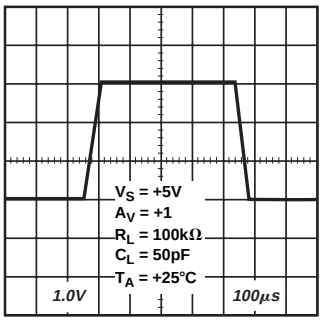


Figure 26. Large Signal Transient Response

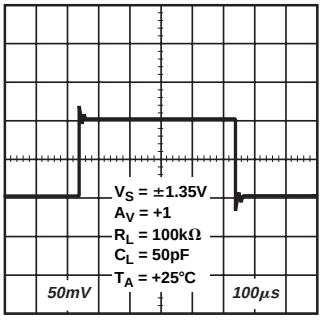


Figure 27. Small Signal Transient Response

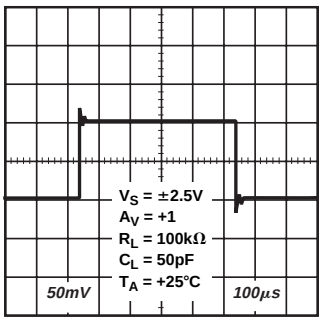


Figure 28. Small Signal Transient Response

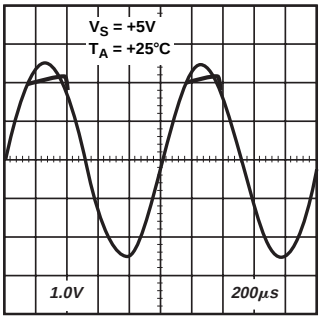


Figure 29. No Phase Reversal

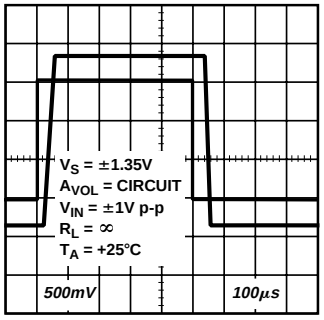


Figure 30. Saturation Recovery Time

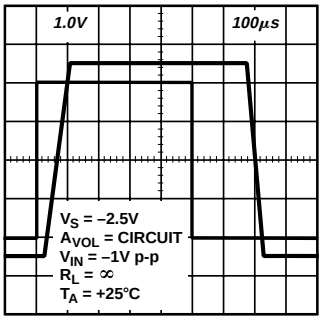


Figure 31. Saturation Recovery Time

APPLICATIONS

The OP186 is very similar in design to the OP181. Please see the OP181/OP281/OP481 data sheet for applications information.

Design of the OP186 was based on the OP181. The major difference is that the trim structures have been removed. This results in the offset of the OP186 being higher than the OP181. There are no other major changes to the circuit. Other performance differences, such as the higher bandwidth and slightly higher supply current, also result from the removal of the trim resistors.

SPICE MODEL

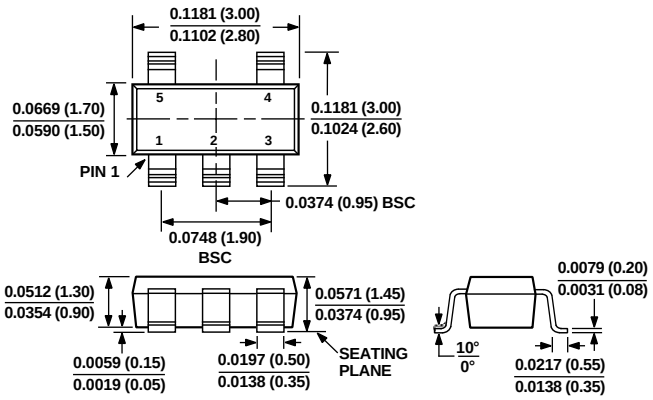
```
* OP186 SPICE Macro-model Typical Values
* 2/98, Ver. 1
* TAM / ADSC
*


* Copyright 1998 by Analog Devices
*
* Refer to “README.DOC” file for License State-
* ment.  Use of this
* model indicates your acceptance of the terms
* and provisions in
* the License Statement.
*
* Node Assignments
*               noninverting input
*               |    inverting input
*               |    |    positive supply
*               |    |    |    negative supply
*               |    |    |    |  output
*               |    |    |    |  |
*               |    |    |    |  |
.SUBCKT OP186   1    2    99   50 45
*
* INPUT STAGE
*
Q1   4  1 3 PIX
Q2   6  7 5 PIX
RC1  4 50 100E3
RC2  6 50 100E3
RE1  3  8 6.452E3
RE2  5  8 6.452E3
C1   4  6 50E-15
I1  99  8 1E-6
EOS  7  2 POLY(2) (12,98) (73,98) 800E-6 1 1
IOS  1  2 50E-12
V1  99  9 0.9
V2  99 10 0.9
D1   3  9 DX
D2   5 10 DX
*
* CMRR 90dB, ZERO AT 1kHz
*
ECM1 11 98 POLY(2) (1,98) (2,98) 0 .5 .5
RCM1 11 12 1.59E6
CCM1 11 12 100E-12
RCM2 12 98 50
*
* PSRR=100dB, ZERO AT 200Hz
*
RPS1 70  0 1E6
RPS2 71  0 1E6
CPS1 99 70 1E-5
CPS2 50 71 1E-5
EPSY 98 72 POLY(2) (70,0) (0,71) 0 1 1
RPS3 72 73 1.59E6
CPS3 72 73 500E-12
RPS4 73 98 15.9
*
* INTERNAL VOLTAGE REFERENCE
*
EREF 98  0 POLY(2) (99,0) (50,0) 0 .5 .5
GSY  99 50 POLY(1) (99,50) 2E-6 .1E-6
*
* POLE AT 600kHz; ZERO AT 900kHz
*
G1 98 20 (4,6) 11.3E-6
R1 20 98 88.46E3
R2 20 21 176.8E3
C2 21 98 1E-12
*
* GAIN STAGE
*
G4  98 30 (20,98) 19.54E-6
R7  30 98 111.6E6
CF  45 30 32E-12
D3  30 31 DX
D4  32 30 DX
V3  99 31 0.6
V4  32 50 0.6
*
* OUTPUT STAGE
*
M1  45 46 99 99 POX L=2u W=100u
M2  45 47 50 50 NOX L=2u W=98u
EG1 99 46 POLY(1) (98,30) 0.82 1
EG2 47 50 POLY(1) (30,98) 0.79 1
*
* MODELS
*
.MODEL POX PMOS (LEVEL=2, KP=10E-6,
+ VTO=-0.75, LAMBDA=0.01)
.MODEL NOX NMOS (LEVEL=2, KP=17E-6,
+ VTO=0.75,  LAMBDA=0.01)
.MODEL PIX PNP (BF=185,KF=1.6E-12,AF=1)
.MODEL DX D(IS=1E-14)
.ENDS OP186
```

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

5-Lead SOT-23
(RT Suffix)



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