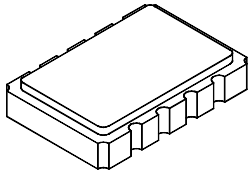
Preliminary

OP4017B

777.60 MHz Optical Timing Clock

- ***Quartz SAW Stabilized Differential Output Technology***
- ***Very Low Jitter Fundamental-Mode Operation at 777.60 MHz***
- ***Voltage Tunable for Phase Locked Loop Applications***
- ***Optical Timing Reference for Forward Error Correction Applications***

The OP4017B is a voltage-controlled SAW clock (VCSC) designed for phase-locked loop (PLL) applications in optical data communications systems. The differential outputs of the OP4017B are generated by high-Q, fundamental mode quartz surface acoustic wave (SAW) technology. This technique provides very low output jitter and phase noise, plus excellent immunity to power supply noise. The OP4017B differential outputs feature ±1% symmetry, and can be DC-configured to drive a wide range of high-speed logic families. The OP4017B is packaged in a hermetic metal-ceramic LCC.



SMC-8

Absolute Maximum Ratings

Rating	Value	Units
DC Suppy Voltage	0 to 5.5	Vdc
Tune Voltage	0 to 5.5	Vdc
Case Temperature	-55 to 100	°C

Electrical Characteristics

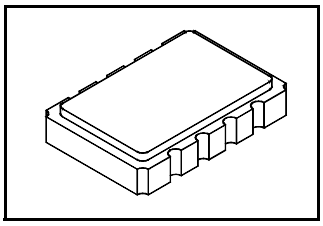
Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	Absolute Frequency	f_O	1		777.6		MHz
	Tuning Range		2		±100		ppm
	Tuning Voltage		1	0		3.3	Vdc
	Tuning Linearity		1, 8		±5		%
	Modulation Bandwidth				50		kHz
Q and $\overline{Q}$ Output	Voltage into 50 Ω (VSWR ≤ 1.2)	V_O	1,3	0.60		1.1	V_{P-P}
	Operating Load VSWR		1,3			2:1	
	Symmetry		3, 4, 5	49		51	%
	Harmonic Spurious		3, 4, 6			-15	dBc
	Nonharmonic Spurious		3, 4, 6, 7			-60	dBc
Phase Noise	@ 100 Hz offset		3, 6		-70		dBc/Hz
	@ 1 kHz offset		3, 6		-100		dBc/Hz
	@ 10 kHz offset		3, 6		-125		dBc/Hz
	Noise Floor		3, 6		-150		dBc/Hz
Q and $\overline{Q}$ Jitter	RMS Jitter		3, 4, 6, 7		1		ps
	No Noise on V_{CC}		3, 4, 6, 7		12		ps_{P-P}
	200 mV_{P-P} Noise, from 1 MHz to ½ f_O on V_{CC}		3		12		ps_{P-P}
Output DC Resistance (between Q & $\overline{Q}$)			1, 3	50			KΩ
DC Power Supply	Operating Voltage	V_{CC}	1, 3	3.13	3.3 or 5.0	5.25	Vdc
	Operating Current	I_{CC}	1, 3			70	mA
Operating Case Temperature		T_C	1, 3	-40°C		+85°C	°C
Lid Symbolization (YY=Year, WW=Week)		RFM OP4017B YYWW					

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.
COCOM CAUTION: Approval by the U.S. Department of Commerce is required prior to export of this device.

Notes:

1. Unless otherwise noted, all specifications include the combined effects of load VSWR, V_{CC} and T_C.
2. Net tuning range after tuning out the effects of initial manufacturing tolerances, VSWR pushing/pulling, V_{CC}, T_C and aging.
3. The internal design, manufacturing processes, and specifications of this device are subject to change without notice.
4. Specified only for a balanced load with a VSWR < 1.2 (50 ohms each side), and a V_{CC} = 3.0 Vdc.
5. Symmetry is defined as the width in (% of total period) measure at 50% of the peak-to-peak voltage of either output.
6. Jitter and other noise outputs due to power supply noise or mechanical vibration are not included in this specification except where noted.
7. Applies to period jitter of either differential output. Measured with a Tektronix CSA803 signal analyzer with at least 1000 samples.
8. See Figure 4.
9. One or more of the following United States patents apply: 4, 616,197; 4,670,681; 4,760,352.

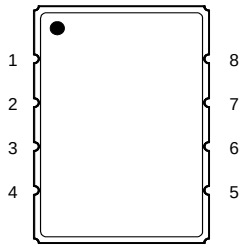
SMC-8 8-Terminal Surface Mount Case



Dimension	mm		Inches	
	MIN	MAX	MIN	MAX
A	13.46	13.97	0.530	0.550
B	9.14	9.66	0.360	0.380
C	1.93 Nominal		0.076 Nominal	
D	3.56 Nominal		0.141 Nominal	
E	2.24 Nominal		0.088 Nominal	
F	1.27 Nominal		0.050 Nominal	
G	2.54 Nominal		0.100 Nominal	
H	3.05 Nominal		0.120 Nominal	
J	1.93 Nominal		0.076 Nominal	
K	5.54 Nominal		0.218 Nominal	
L	4.32 Nominal		0.170 Nominal	
M	4.83 Nominal		0.190 Nominal	
N	0.50 Nominal		0.020 Nominal	

ELECTRICAL CONNECTIONS

Terminal Number	Connection
1	V_{CC}
2	Ground
3	Enable/Disable
4	Q Output
5	$\overline{Q}$ Output
6	Ground
7	
8	Tuning Input
LID	Ground

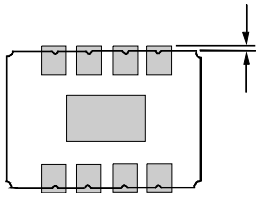


TOP VIEW

Typical Printed Circuit Board Land Pattern

A typical land pattern for a circuit board is shown on the right.

Grounding of the metallic center pad is optional.



Typically 0.01" to 0.05" or 0.25 mm to 1.25 mm (8 Places)

(The optimum value of this dimension is dependent on the PCB assembly process employed.)