OPA168x
SoundPlus 36-V, Single-Supply, 10-MHz, Rail-to-Rail Output Operational Amplifiers

1 Features

- THD+N, 50 mW, 32 Ω, 1 kHz, –109 dB
- Wide Supply Range:
  - 4.5 V to 36 V, ±2.25 V to ±18 V
- Low Offset Voltage: ±0.25 mV
- Low Offset Drift: ±0.5 µV/°C
- Gain Bandwidth: 10 MHz
- Low Input Bias Current: ±10 pA
- Low Quiescent Current: 1.6 mA per Amplifier
- Low Noise: 8 nV/√Hz
- EMI- and RFI-Filtered Inputs
- Input Range Includes Negative Supply
- Input Range Operates to Positive Supply
- Rail-to-Rail Output
- High Common-Mode Rejection: 120 dB
- Industry-Standard Packages:
  - SOIC-8 and SOIC-14
- *micro*Packages:
  - Dual in WSON-8, Quad in VQFN-16

2 Applications

- Headphone Driver
- Analog and Digital Mixers
- Audio Effects Processors
- Transducer Amplifiers
- Musical Instruments
- A/V Receivers
- DVD and Blu-Ray™ Players
- Car Audio Systems

3 Description

The OPA1688 and OPA1689 are a family of SoundPlus™ 36-V, single-supply, low-noise operational amplifiers capable of operating on supplies ranging from 4.5 V (±2.25 V) to 36 V (±18 V). This latest addition of high-voltage audio operational amplifiers, in conjunction with the OPA16xx devices provide a family of bandwidth, noise, and power options to meet the needs of a wide variety of applications. The OPA168x are available in micropackages, and offer low offset, drift, and quiescent current. These devices also offer wide bandwidth, fast slew rate, and high output current drive capability. The dual and quad versions all have identical specifications for maximum design flexibility.

Unlike most op amps that are specified at only one supply voltage, the OPA168x family is specified from 4.5 V to 36 V. Input signals beyond the supply rails do not cause phase reversal. The input can operate 100 mV below the negative rail and within 2 V of the top rail during normal operation. Note that these devices can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail.

The OPA168x series of op amps are specified from –40°C to 85°C.

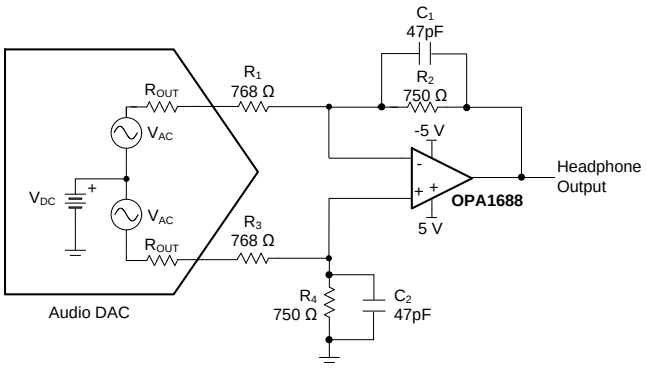
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1688	SOIC (8)	4.90 mm × 3.91 mm
	WSON (8)	3.00 mm × 3.00 mm
OPA1689(2)	SOIC (14)	8.65 mm × 3.91 mm
	VQFN (16)	3.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) Product-preview device.

Headphone Amplifier Circuit Configuration



Superior THD Performance
(f = 1 kHz, BW = 80 kHz, V_S = ±5 V)

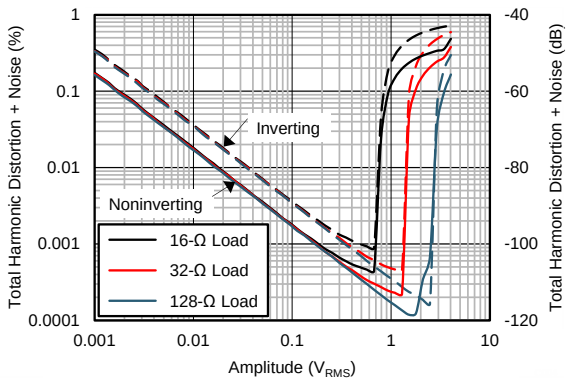


Table of Contents

4 Revision History

DATE	REVISION	NOTES
September 2015	*	Initial release.

5 Device Comparison Table

DEVICE(1)	PACKAGE
OPA1688 (dual)	SOIC-8, WSON-8
OPA1689 (quad)	SOIC-14, VQFN-16

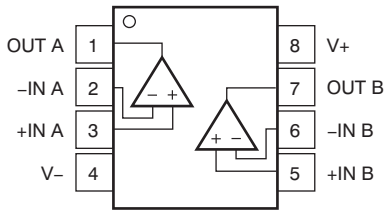
(1) The OPA1688 SOIC-8 and WSON-8 packages are production data. The OPA1689 SOIC-14 and VQFN-16 packages are product preview.

6 Device Family Comparison Table

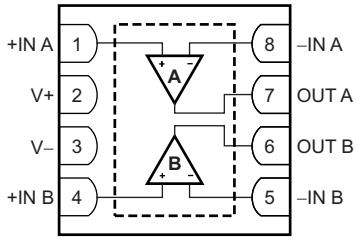
DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPA168x	1650 µA	10 MHz	8 nV/√Hz
OPA165x	2000 µA	18 MHz	4.5 nV/√Hz
OPA166x	1500 µA	22 MHz	3.3 nV/√Hz

7 Pin Configuration and Functions

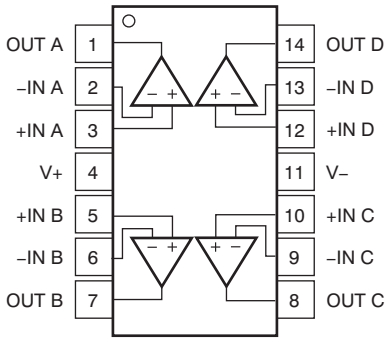
D Package: OPA1688
SOIC-8
Top View



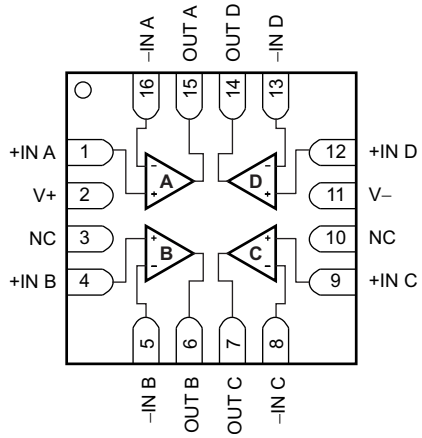
DRG Package: OPA1688
WSON-8
Top View



D Package: OPA1689
SOIC-14
Top View



RVA Package: OPA1689
VQFN-16
Top View



Pin Functions: OPA1688

PIN			I/O	DESCRIPTION
	OPA1688			
NAME	D (SOIC)	DRG (WSON)		
+IN A	3	1	I	Noninverting input, channel A
+IN B	5	4	I	Noninverting input, channel B
–IN A	2	8	I	Inverting input, channel A
–IN B	6	5	I	Inverting input, channel B
OUT A	1	7	O	Output, channel A
OUT B	7	6	O	Output, channel B
V+	8	2	—	Positive (highest) power supply
V–	4	3	—	Negative (lowest) power supply

Pin Functions: OPA1689

PIN			I/O	DESCRIPTION
	OPA1689			
NAME	D	RVA		
+IN A	3	1	I	Noninverting input, channel A
+IN B	5	4	I	Noninverting input, channel B
+IN C	10	9	I	Noninverting input, channel C
+IN D	12	12	I	Noninverting input, channel D
–IN A	2	16	I	Inverting input, channel A
–IN B	6	5	I	Inverting input, channel B
–IN C	9	8	I	Inverting input, channel C
–IN D	13	13	I	Inverting input, channel D
OUT A	1	15	O	Output, channel A
OUT B	7	6	O	Output, channel B
OUT C	8	7	O	Output, channel C
OUT D	14	14	O	Output, channel D
V+	4	2	—	Positive (highest) power supply
V–	11	11	—	Negative (lowest) power supply
NC	—	3, 10	—	No connection

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S				±20 (40, single supply)	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(3)		±0.5	V
	Current			±10	mA
Output short circuit(4)				Continuous	
Temperature	Temperature range		–55	150	°C
	Junction temperature			150	°C
	Storage, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings should be current limited to 10 mA or less.
(3) See the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		85	°C

8.4 Thermal Information: OPA1688

THERMAL METRIC(1)		OPA1688		UNIT
		D (SOIC)	DRG (WSON)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	36.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Thermal Information: OPA1689

THERMAL METRIC(1)		OPA1689		UNIT
		D (SOIC)	RVA (VQFN)	
		14 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	TBD	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.6 Electrical Characteristics

At T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS} , R_L = 2 kΩ		0.00005%		
				–126		dB
		G = 1, f = 1 kHz, V_O = 3.5 V_{RMS} , R_L = 600 Ω		0.000051%		
				–126		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 128 Ω		0.000153%		
				–116		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 32 Ω		0.000357%		
				–109		dB
		G = 1, f = 1 kHz, P_O = 10 mW, R_L = 16 Ω		0.000616%		
				–104		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	G = 1		10		MHz
SR	Slew rate	G = 1		8		V/µs
	Full-power bandwidth(1)	V_O = 1 V_{PP}		1.3		MHz
	Overload recovery time	V_{IN} × gain > V_S		200		ns
	Channel separation (dual)	f = 1 kHz		–120		dB
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1, 10-V step		3		µs
NOISE						
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz		2.5		μV_{PP}
e_n	Input voltage noise density(2)	f = 100 Hz		14		$nV/\sqrt{Hz}$
		f = 1 kHz		8		
i_n	Input current noise density	f = 1 kHz		1.8		$fA/\sqrt{Hz}$
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	T_A = 25°C		±0.25	±1.5	mV
		T_A = –40°C to 85°C			±1.6	
dV_{OS}/dT	V_{OS} over temperature(2)	T_A = –40°C to 85°C		±0.5	±2	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to 85°C		±1	±2.5	µV/V
	Channel separation, dc	At dc		0.1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	T_A = 25°C		±10	±20	pA
		T_A = –40°C to 85°C			±1.5	nA
I_{OS}	Input offset current	T_A = 25°C		±3	±7	pA
		T_A = –40°C to 85°C			±250	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range(3)		(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to 85°C	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to 85°C	104	120		
INPUT IMPEDANCE						
	Differential			100 || 7		MΩ || pF
	Common-mode			6 || 1.5		10^{12}Ω || pF

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) Common-mode range can extend to the top rail with reduced performance.

Electrical Characteristics (continued)

At T_A = 25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to 85°C	108	130		dB
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to 85°C		118		
OUTPUT						
V_O	Voltage output swing from rail	I_L = ±1 mA	(V–) + 0.1 V		(V+) – 0.1 V	mV
		V_S = 36 V, R_L = 10 kΩ		70	90	
		V_S = 36 V, R_L = 2 kΩ		330	400	
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A		60		Ω
I_{SC}	Short-circuit current			±75		mA
C_{LOAD}	Capacitive load drive		See the *Typical Characteristics*			pF
POWER SUPPLY						
V_S	Specified voltage range		4.5		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A		1.6	1.8	mA
		I_O = 0 A, T_A = –40°C to 85°C			2	
TEMPERATURE RANGE						
	Specified range		–40		85	°C
	Operating range		–55		125	°C

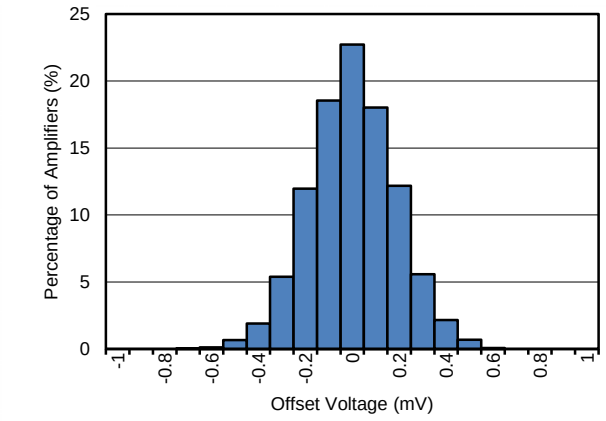
8.7 Typical Characteristics: Table of Graphs

Table 1. List of Typical Characteristics

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature (V_S = ±18 V)	Figure 3
Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)	Figure 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	Figure 5
Offset Voltage vs Power Supply	Figure 6
Input Bias Current vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 10
CMRR vs Temperature	Figure 11
PSRR vs Temperature	Figure 12
0.1-Hz to 10-Hz Noise	Figure 13
Input Voltage Noise Spectral Density vs Frequency	Figure 14
THD+N Ratio vs Frequency	Figure 15
THD+N vs Output Amplitude	Figure 16
THD+N vs Frequency	Figure 17
THD+N vs Amplitude	Figure 18
Quiescent Current vs Temperature	Figure 19
Quiescent Current vs Supply Voltage	Figure 20
Open-Loop Gain and Phase vs Frequency	Figure 21
Closed-Loop Gain vs Frequency	Figure 22
Open-Loop Gain vs Temperature	Figure 23
Open-Loop Output Impedance vs Frequency	Figure 24
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 25, Figure 26
Positive Overload Recovery	Figure 27, Figure 28
Negative Overload Recovery	Figure 29, Figure 30
Small-Signal Step Response (10 mV, G = –1)	Figure 31
Small-Signal Step Response (10 mV, G = 1)	Figure 32
Small-Signal Step Response (100 mV, G = –1)	Figure 33
Small-Signal Step Response (100 mV, G = 1)	Figure 34
Large-Signal Step Response (10 V, G = –1)	Figure 35
Large-Signal Step Response (10 V, G = 1)	Figure 36
Large-Signal Settling Time (10-V Positive Step)	Figure 37
Large-Signal Settling Time (10-V Negative Step)	Figure 38
No Phase Reversal	Figure 39
Short-Circuit Current vs Temperature	Figure 40
Maximum Output Voltage vs Frequency	Figure 41
EMIRR vs Frequency	Figure 42
Channel Separation vs Frequency	Figure 43

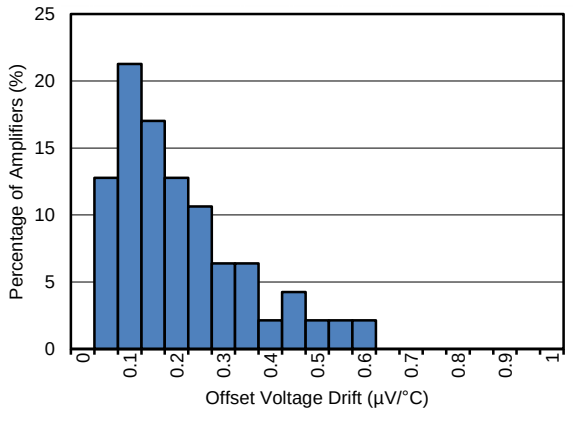
8.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



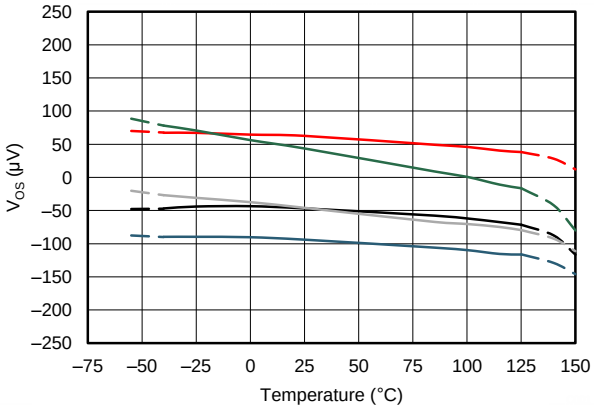
Distribution taken from 5185 amplifiers

Figure 1. Offset Voltage Production Distribution



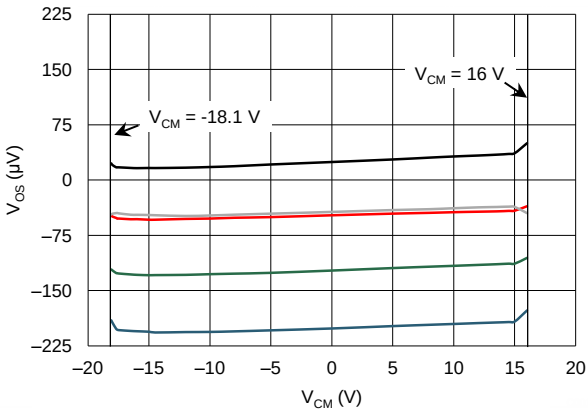
Distribution taken from 47 amplifiers,
temperature = –40°C to 125°C

Figure 2. Offset Voltage Drift Production Distribution



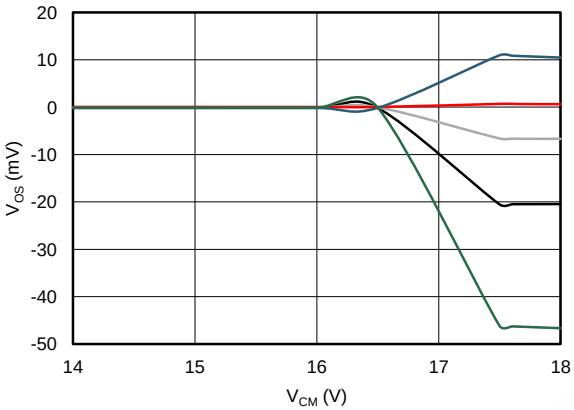
5 typical units shown, V_S = ±18 V

Figure 3. Offset Voltage vs Temperature (V_S = ±18 V)



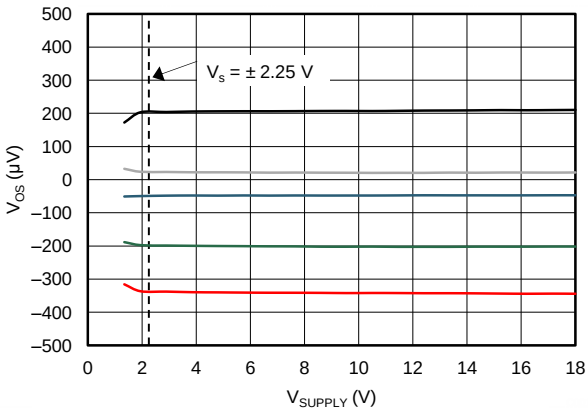
5 typical units shown, V_S = ±18 V

Figure 4. Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)



5 typical units shown, V_S = ±18 V

Figure 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)



5 typical units shown, V_S = ±2.25 V to ±18 V

Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

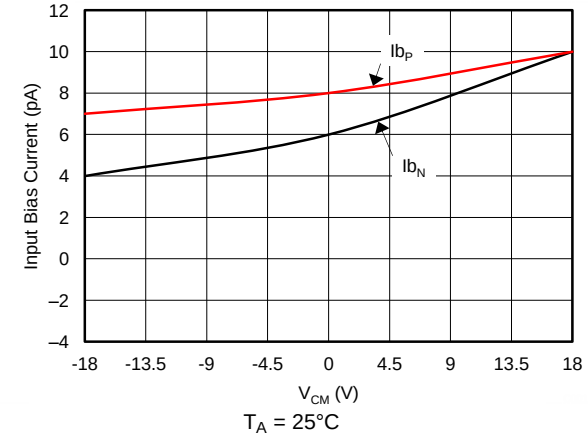


Figure 7. Input Bias Current vs Common-Mode Voltage

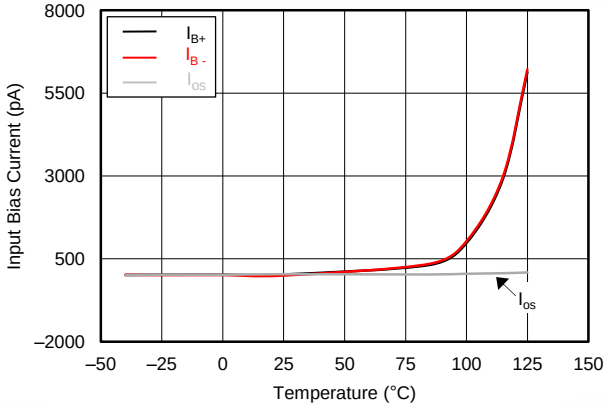


Figure 8. Input Bias Current vs Temperature

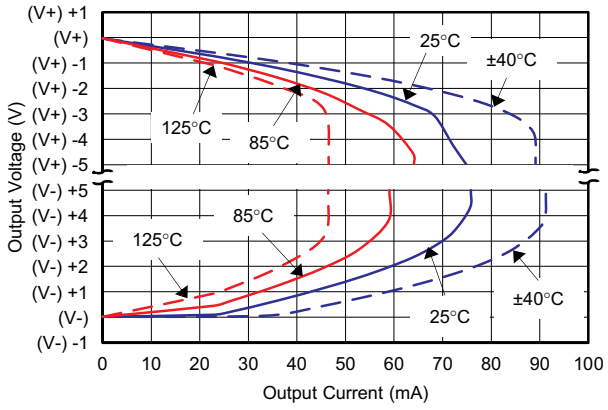


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

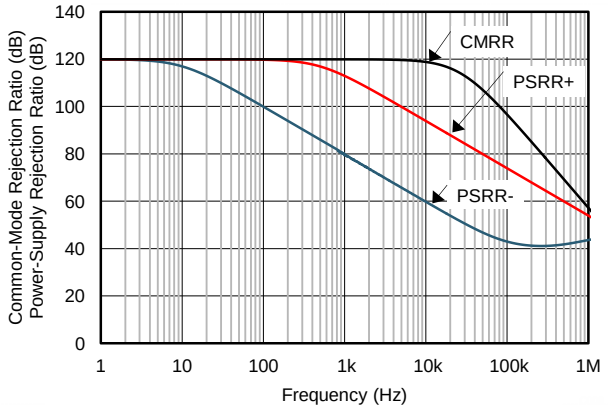


Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)

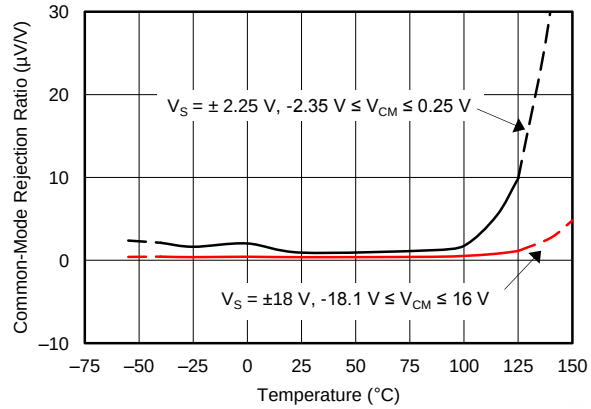


Figure 11. CMRR vs Temperature

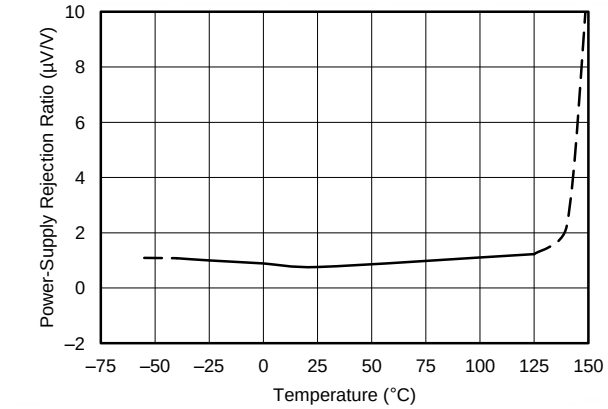
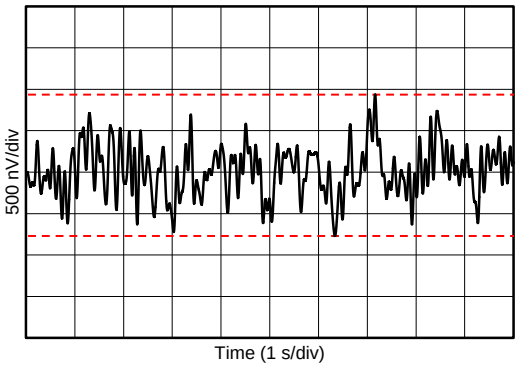


Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



Peak-to-peak noise = 1.70 μV_{PP}

Figure 13. 0.1-Hz to 10-Hz Noise

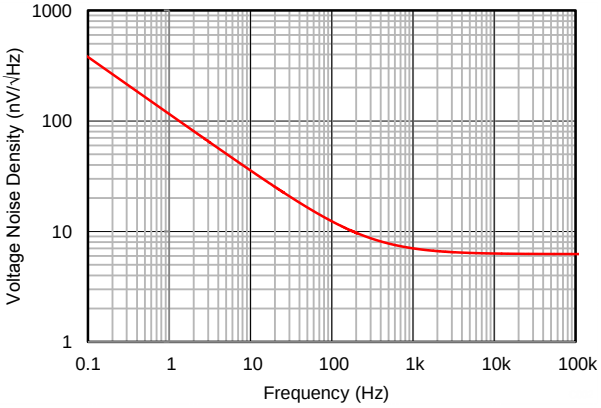
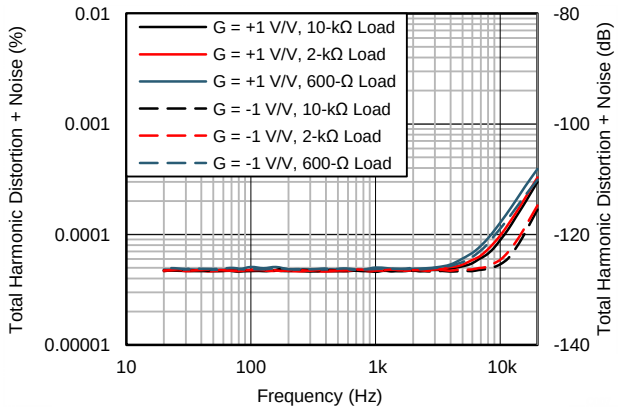
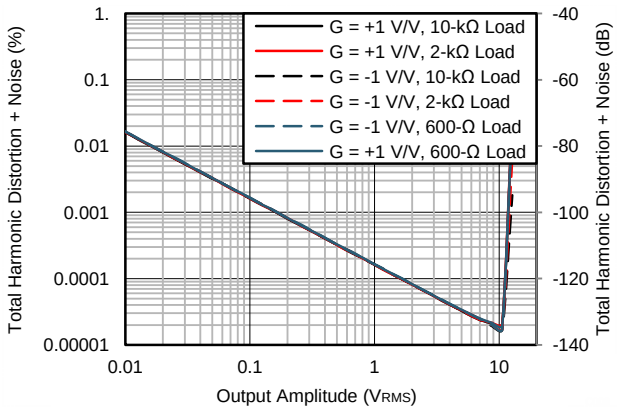


Figure 14. Input Voltage Noise Spectral Density vs Frequency



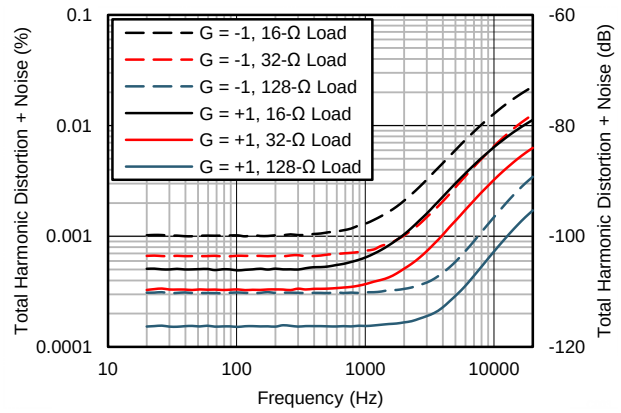
V_{OUT} = 3.5 V_{RMS}, BW = 50 kHz

Figure 15. THD+N Ratio vs Frequency



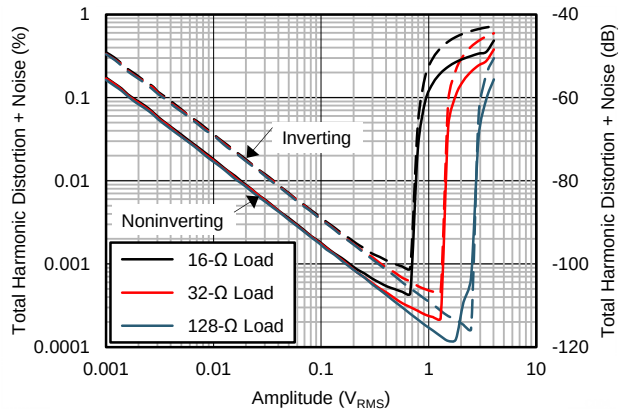
f = 1 kHz, BW = 80 kHz

Figure 16. THD+N vs Output Amplitude



P_{OUT} = 10 mW, BW = 80 kHz, V_S = ±5 V

Figure 17. THD+N vs Frequency



f = 1 kHz, BW = 80 kHz, V_S = ±5 V

Figure 18. THD+N vs Amplitude

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

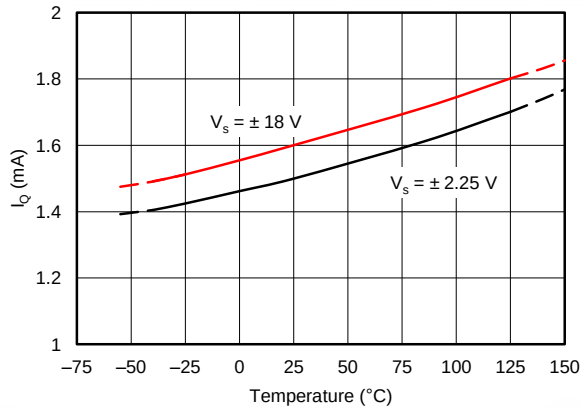


Figure 19. Quiescent Current vs Temperature

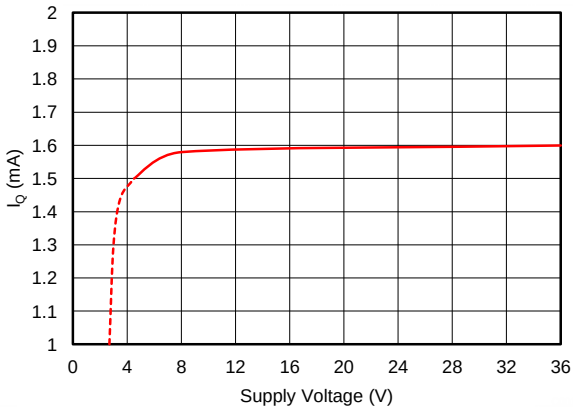
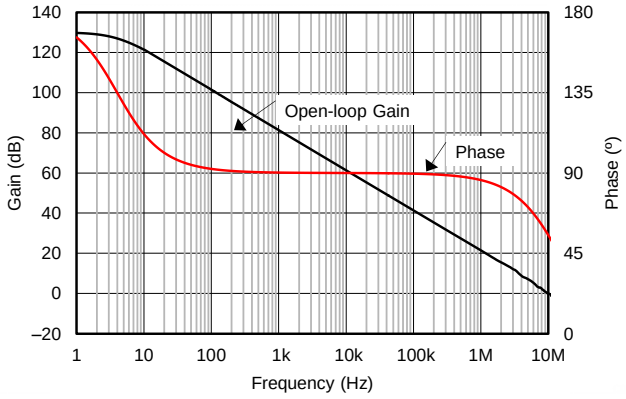


Figure 20. Quiescent Current vs Supply Voltage



C_{LOAD} = 15 pF

Figure 21. Open-Loop Gain and Phase vs Frequency

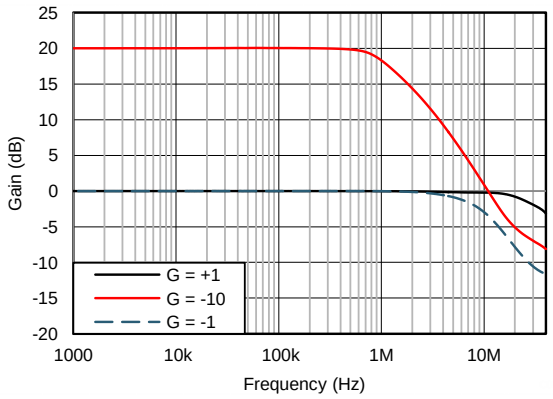
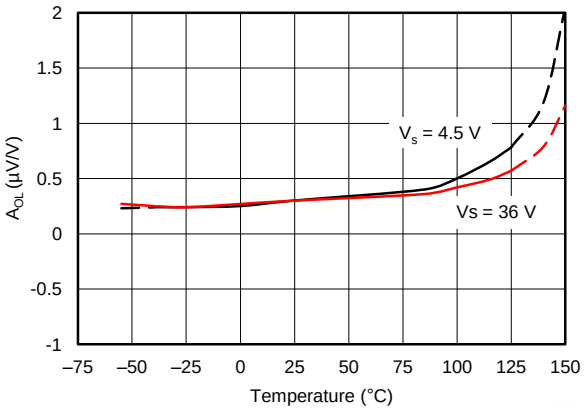


Figure 22. Closed-Loop Gain vs Frequency



R_L = 10 kΩ

Figure 23. Open-Loop Gain vs Temperature

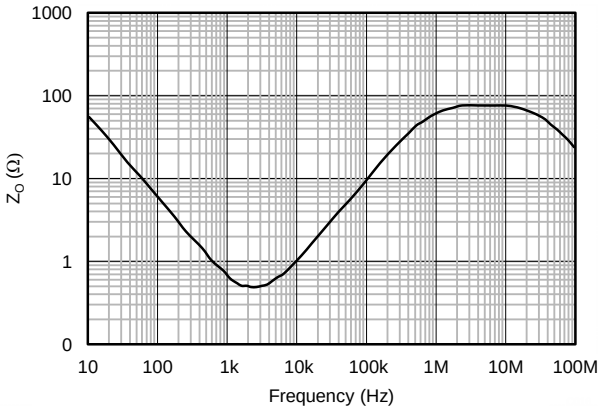


Figure 24. Open-Loop Output Impedance vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

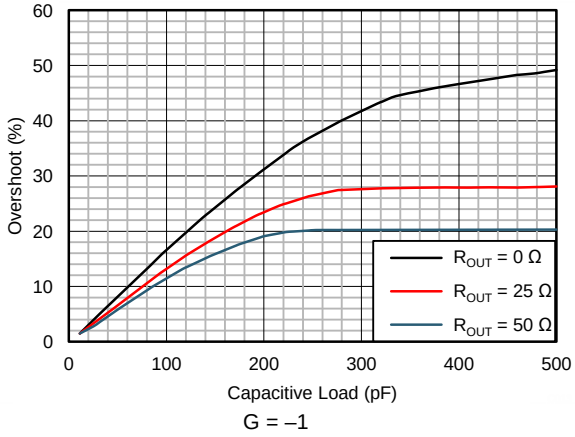


Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

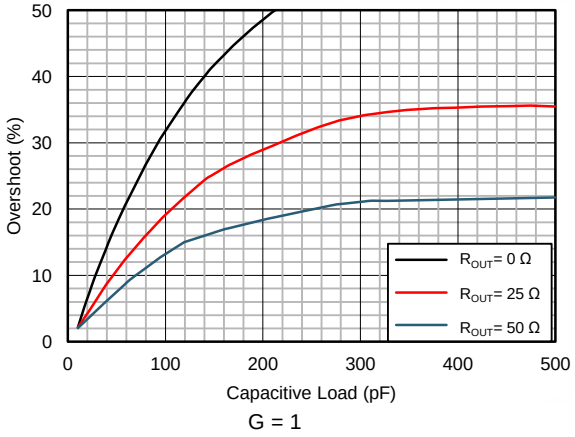


Figure 26. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

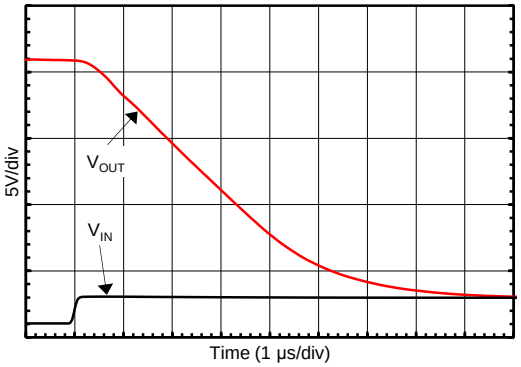


Figure 27. Positive Overload Recovery

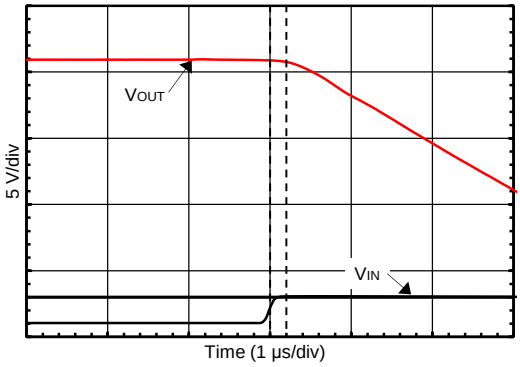


Figure 28. Positive Overload Recovery (Zoomed In)

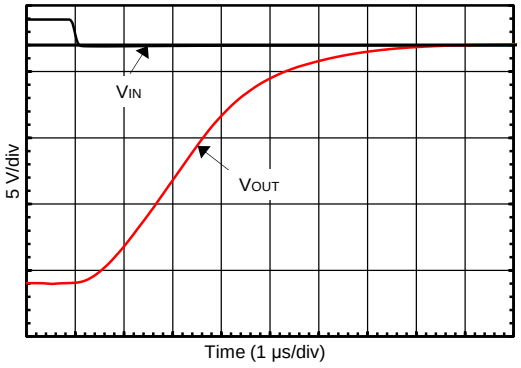


Figure 29. Negative Overload Recovery

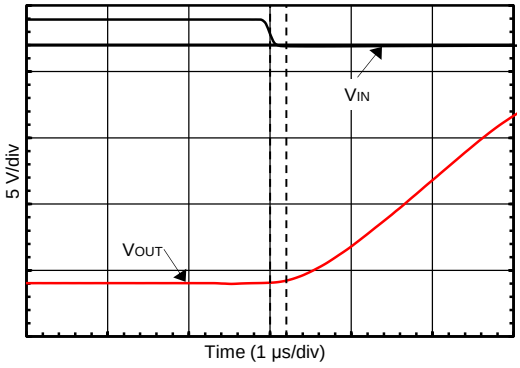
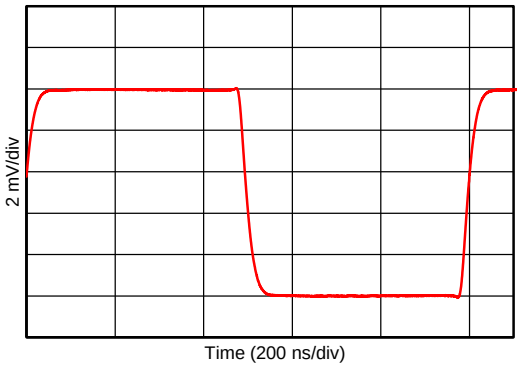


Figure 30. Negative Overload Recovery (Zoomed In)

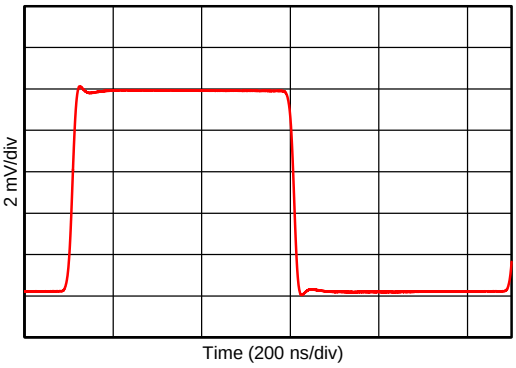
Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



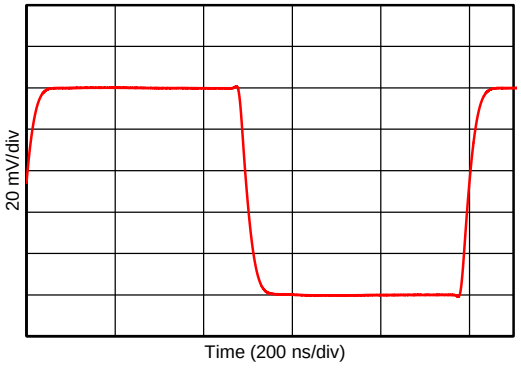
R_L = 1 kΩ, C_L = 10 pF

Figure 31. Small-Signal Step Response (10 mV, G = –1)



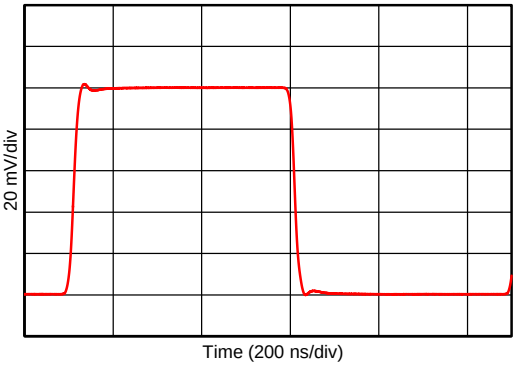
C_L = 10 pF

Figure 32. Small-Signal Step Response (10 mV, G = 1)



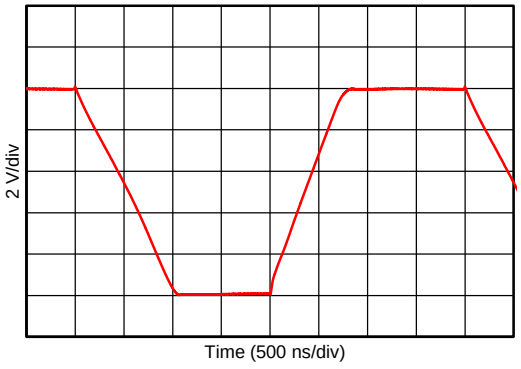
R_L = 1 kΩ, C_L = 10 pF

Figure 33. Small-Signal Step Response (100 mV, G = –1)



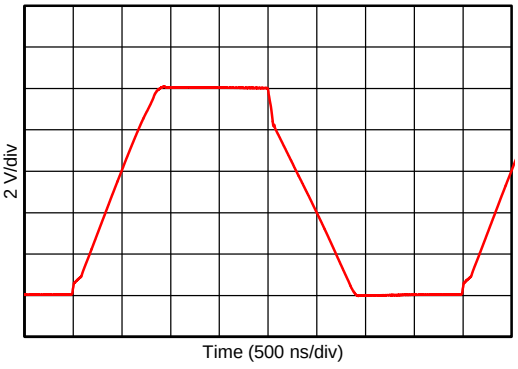
C_L = 10 pF

Figure 34. Small-Signal Step Response (100 mV, G = 1)



R_L = 1 kΩ, C_L = 10 pF

Figure 35. Large-Signal Step Response (10 V, G = –1)

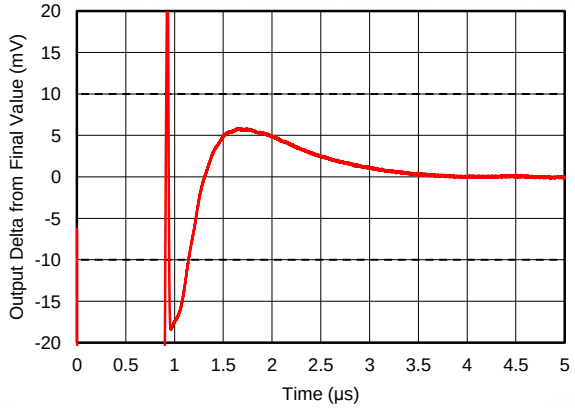


C_L = 10 pF

Figure 36. Large-Signal Step Response (10 V, G = 1)

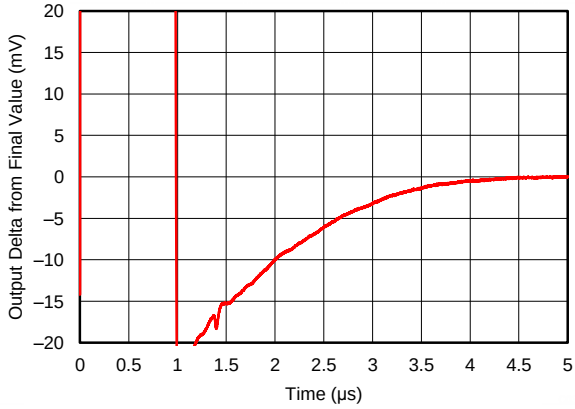
Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.



G = 1, C_L = 10 pF, 0.1% settling = ±10 mV

Figure 37. Large-Signal Settling Time (10-V Positive Step)



G = 1, C_L = 10 pF, 0.1% settling = ±10 mV

Figure 38. Large-Signal Settling Time (10-V Negative Step)

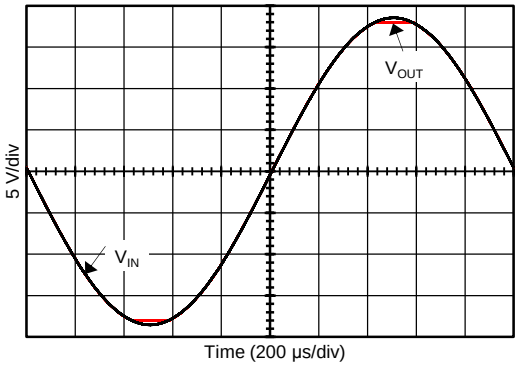


Figure 39. No Phase Reversal

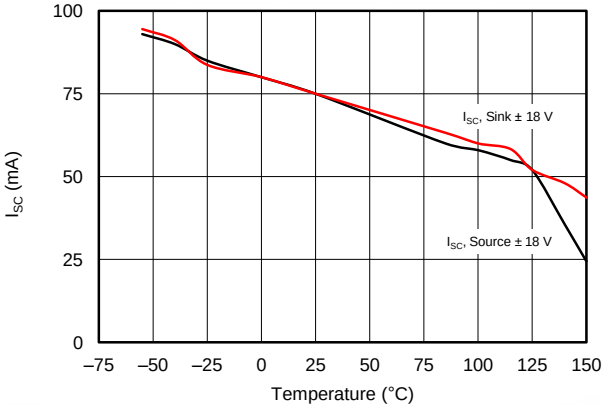


Figure 40. Short-Circuit Current vs Temperature

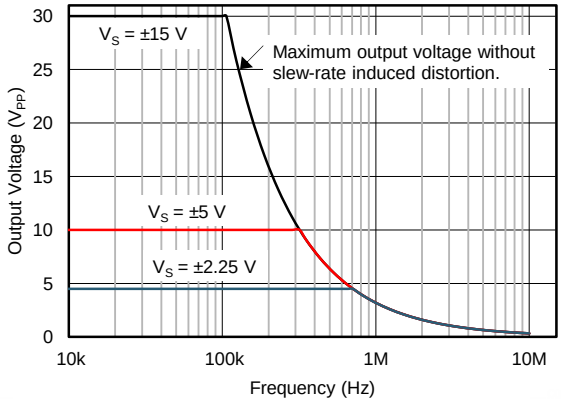
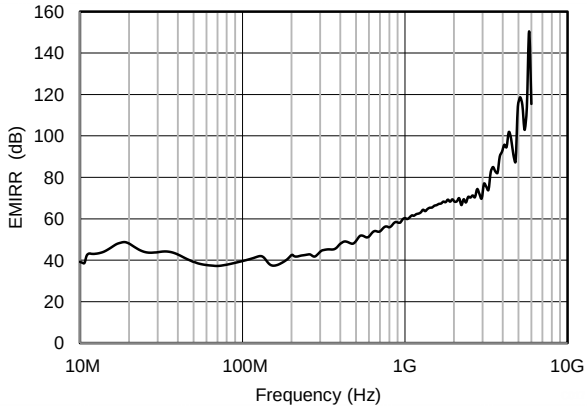


Figure 41. Maximum Output Voltage vs Frequency



P_{RF} = –10 dBm, V_{SUPPLY} = ±18 V, V_{CM} = 0 V

Figure 42. EMIRR vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

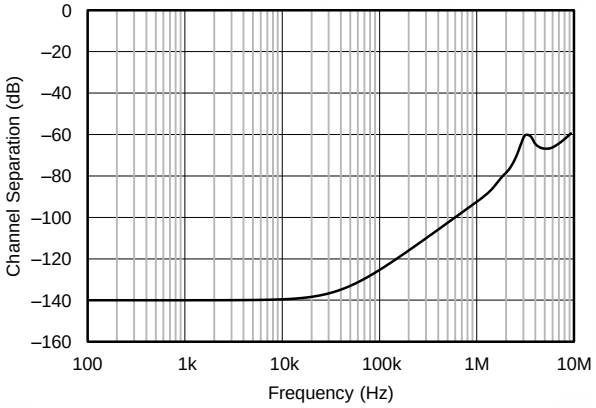


Figure 43. Channel Separation vs Frequency

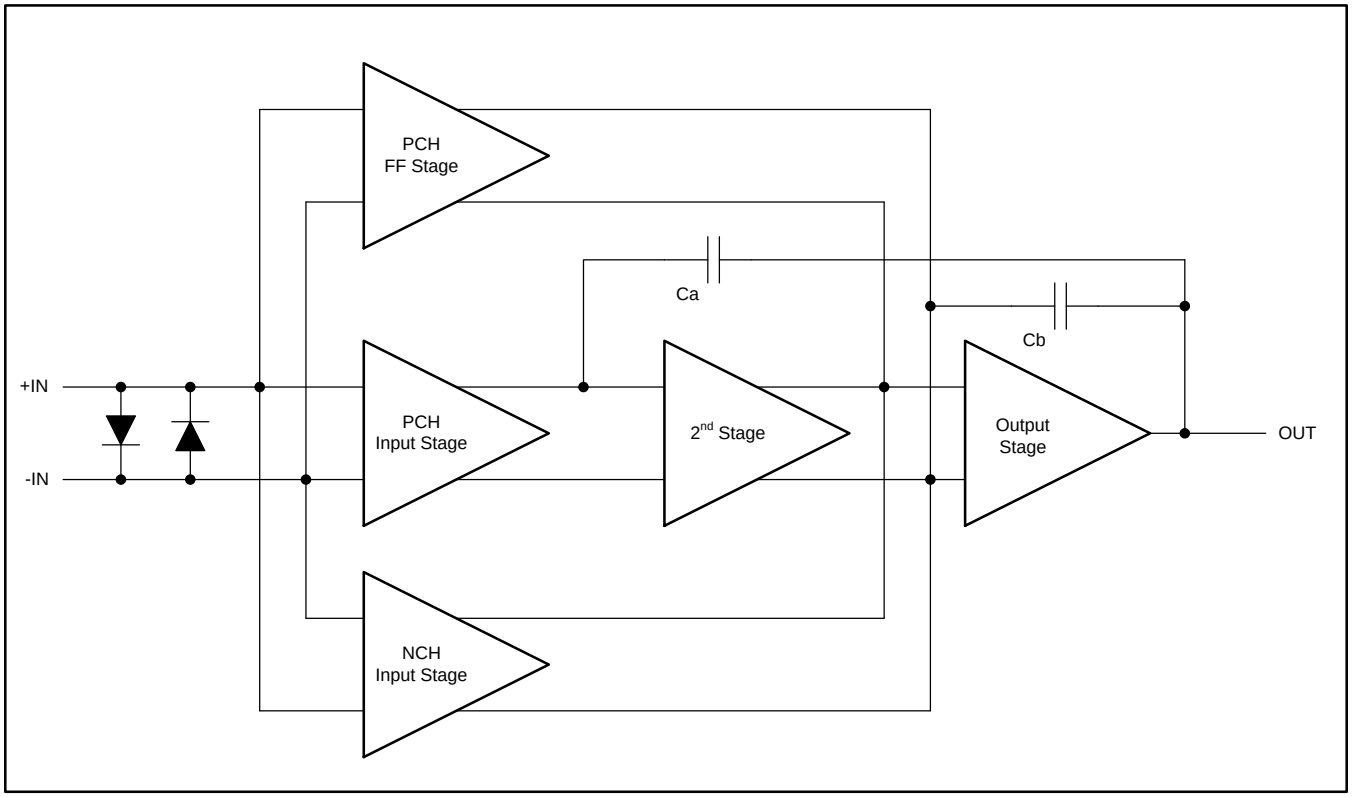
9 Detailed Description

9.1 Overview

The OPA168x family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL}, and superior THD.

The *Functional Block Diagram* section shows the simplified diagram of the OPA168x design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

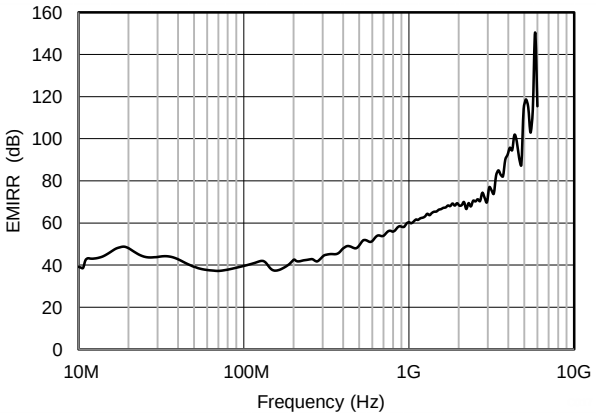
9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 EMI Rejection

The OPA168x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPA168x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 44 shows the results of this testing on the OPA168x. Table 2 shows the EMIRR IN+ values for the OPA168x at particular frequencies commonly encountered in real-world applications. Applications listed in Table 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in application report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.



P_{RF} = –10 dBm, V_{SUPPLY} = ±18 V, V_{CM} = 0 V

Figure 44. EMIRR Testing

Table 2. OPAx168x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, and ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, and UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, and L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, and S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, and S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, and C-band (4 GHz to 8 GHz)	114 dB

9.3.2 Phase-Reversal Protection

The OPA168x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA168x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 45.

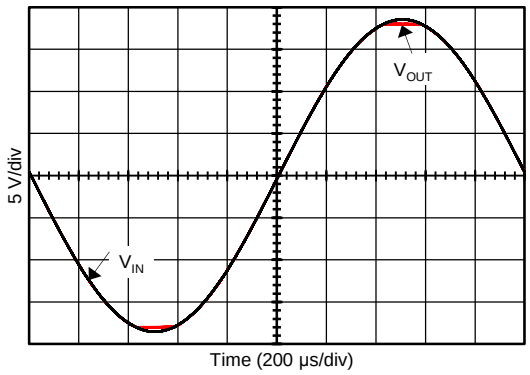


Figure 45. No Phase Reversal

9.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPA168x are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. Figure 46 and Figure 47 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}; see application bulletin SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

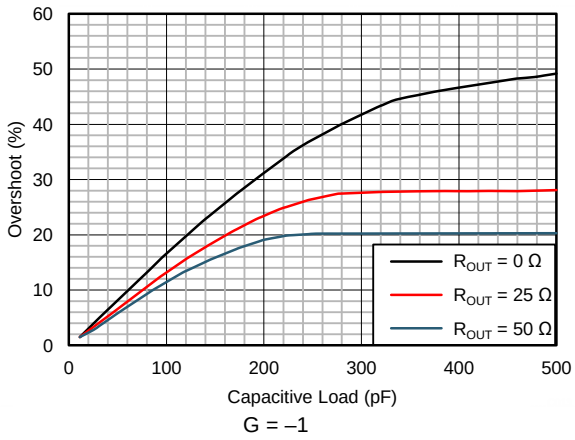


Figure 46. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

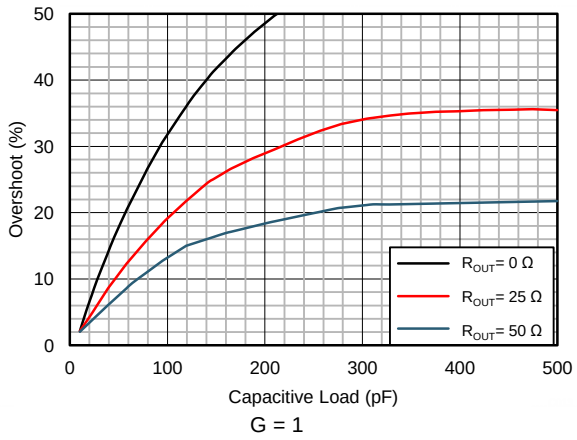


Figure 47. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

9.4 Device Functional Modes

9.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPA168x series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in Table 3.

Table 3. Typical Performance Range (V_S = ±18 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
Offset voltage vs temperature (T_A = –40°C to 85°C)		10		µV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/µs
Noise at f = 1 kHz		22		nV/√Hz

9.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 48 illustrates the ESD circuits contained in the OPA168x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

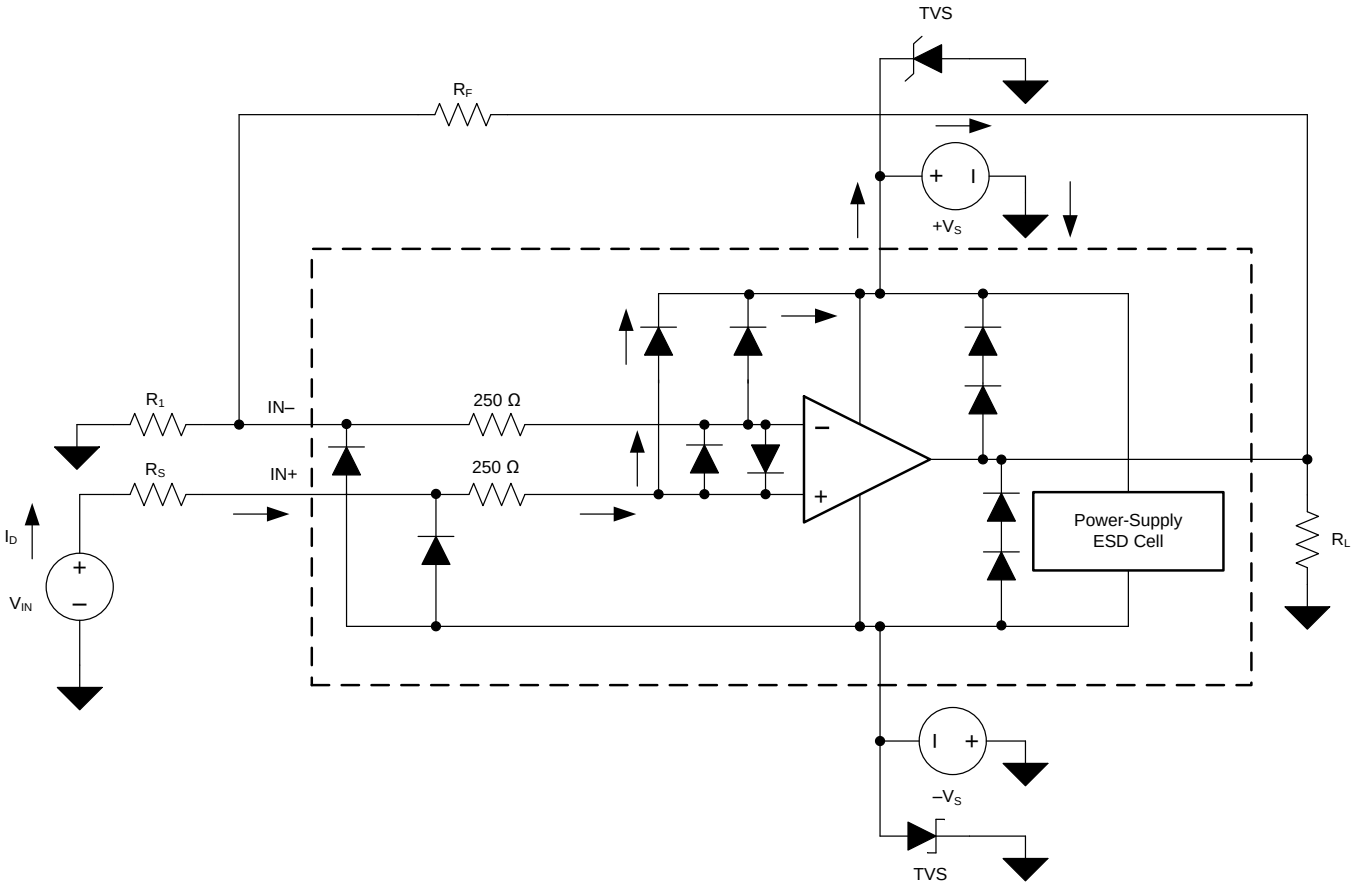


Figure 48. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA168x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (Figure 48), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 48 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies ($+V_S$ or $–V_S$) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply pins; see Figure 48. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

The OPA168x input pins are protected from excessive differential voltage with back-to-back diodes; see Figure 48. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPA168x. Figure 48 illustrates an example configuration that implements a current-limiting feedback resistor.

9.4.3 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either resulting from the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPA168x is approximately 200 ns.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The OPA168x family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

10.2 Typical Application

This application example highlights only a few of the circuits where the OPA168x can be used.

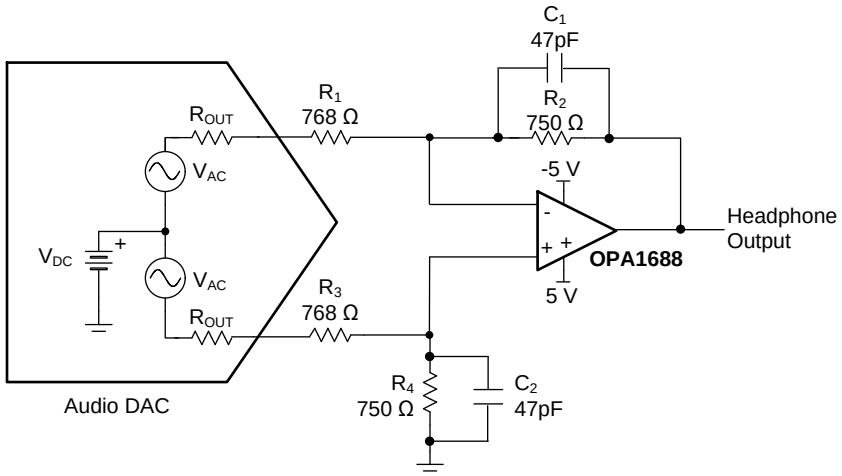


Figure 49. Headphone Amplifier Circuit Configuration for Audio DACs that Output a Differential Voltage (Single Channel Shown)

10.2.1 Design Requirements

The design requirements are:

- Supply voltage: 10 V (±5 V)
- Headphone loads: 16 Ω to 600 Ω
- THD+N: > 100 dB (1-kHz fundamental, 1 V_{RMS} in 32 Ω, 22.4-kHz measurement bandwidth)
- Output power (before clipping): 50 mW into 32 Ω

Typical Application (continued)

10.2.2 Detailed Design Procedure

The OPA168x family offers an excellent combination of specifications for headphone amplifier circuits (such as low noise, low distortion, capacitive load stability, and relatively high output current). Furthermore, the low-power supply current and small package options make the OPA1688 an exceptionally good choice for headphone amplifiers in portable devices. A common headphone amplifier circuit for audio digital-to-analog converters (DACs) with differential voltage outputs is illustrated in Figure 49. This circuit converts the differential voltage output of the DAC to a single-ended, ground-referenced signal and provides the additional current necessary for low-impedance headphones. For $R_2 = R_4$ and $R_1 = R_3$, the output voltage of the circuit is given by Equation 1:

$$V_{OUT} = 2 \times V_{AC} \frac{R_2}{R_1 + R_{OUT}} \quad (1)$$

where

- R_{OUT} is the output impedance of the DAC and
- $2 \times V_{AC}$ is the unloaded differential output voltage

The output voltage required for headphones depends on the headphone impedance as well as the headphone efficiency. Both values can be provided by the headphone manufacturer, with headphone efficiency usually given as a sound pressure level (SPL) produced with 1 mW of input power and denoted by the Greek letter η. The SPL at other input power levels can be calculated from the efficiency specification using Equation 2:

$$\text{SPL (dB)} = \eta + 10 \log\left(\frac{P_{IN}}{1\ \text{mW}}\right) \quad (2)$$

Note that at extremely high power levels, the accuracy of this calculation decreases as a result of secondary effects in the headphone drivers. Figure 50 allows the SPL produced by a pair of headphones of a known sensitivity to be estimated for a given input power.

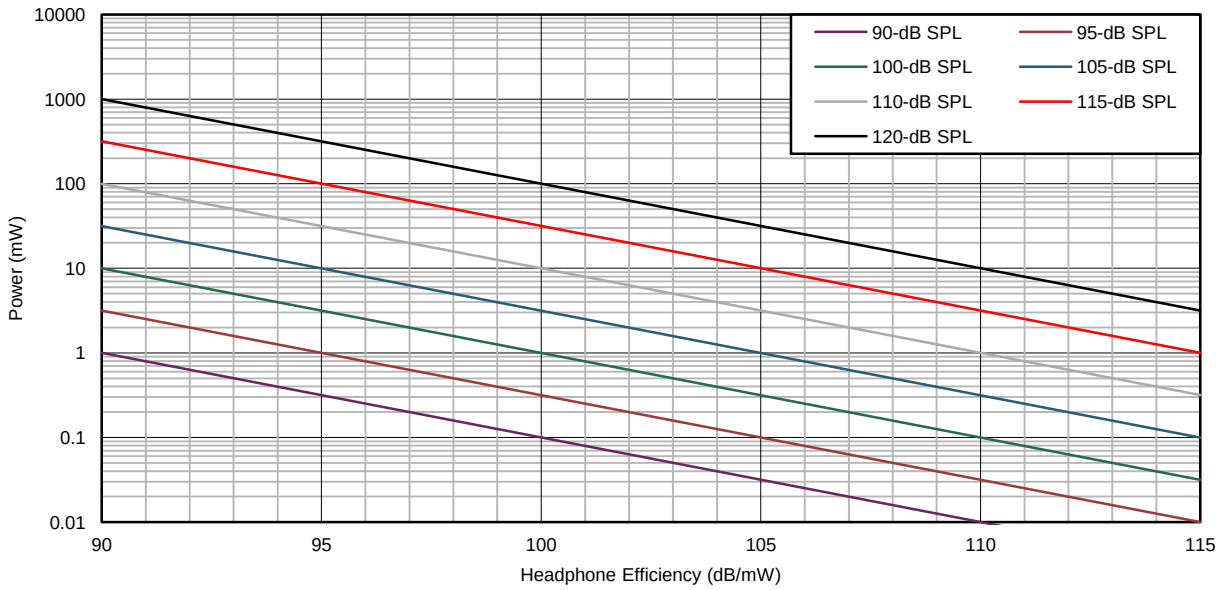


Figure 50. SPLs Produced for Various Headphone Efficiencies and Input Power Levels

Typical Application (continued)

For example, a pair of headphones with a 95-dB/mW sensitivity given a 3-mW input signal produces a 100-dB SPL. If these headphones have a nominal impedance of 32 Ω, then the voltage and current from the headphone amplifier is as described in Equation 3 and Equation 4, respectively:

$$V = \sqrt{P_{IN} \times R_{HP}} = \sqrt{3\ mW \times 32\ \Omega} = 310\ mV_{RMS} \quad (3)$$

$$I = \sqrt{\frac{P_{IN}}{R_{HP}}} = \sqrt{\frac{3\ mW}{32\ \Omega}} = 9.68\ mA_{RMS} \quad (4)$$

Headphones can present a capacitive load at high frequencies that can destabilize the headphone amplifier circuit. Many headphone amplifiers use a resistor in series with the output to maintain stability; however this solution also compromises audio quality. The OPA168x family is able to maintain stability into large capacitive loads; therefore, a series output resistor is not necessary in the headphone amplifier circuit. TINA-TI™ simulations illustrate that the circuit in Figure 49 has a phase margin of approximately 50 degrees with a 400-pF load connected directly to the amplifier output.

10.2.3 Application Curves

The headphone amplifier circuit in Figure 49 is tested with three common headphone impedances: 16 Ω, 32 Ω, and 600 Ω. The total harmonic distortion and noise (THD+N) for increasing output voltages is given in Figure 51. This measurement is performed with a 1-kHz input signal and a measurement bandwidth of 22.4 kHz. The maximum output power and THD+N before clipping are given in Table 4. The maximum output power into low-impedance headphones is limited by the output current capabilities of the amplifier. For high-impedance headphones (600 Ω), the output voltage capabilities of the amplifier are the limiting factor. The circuit in Figure 49 is tested using ±5-V supplies that are common in many portable systems. However, using higher supply voltages increases the output power into 600-Ω headphones.

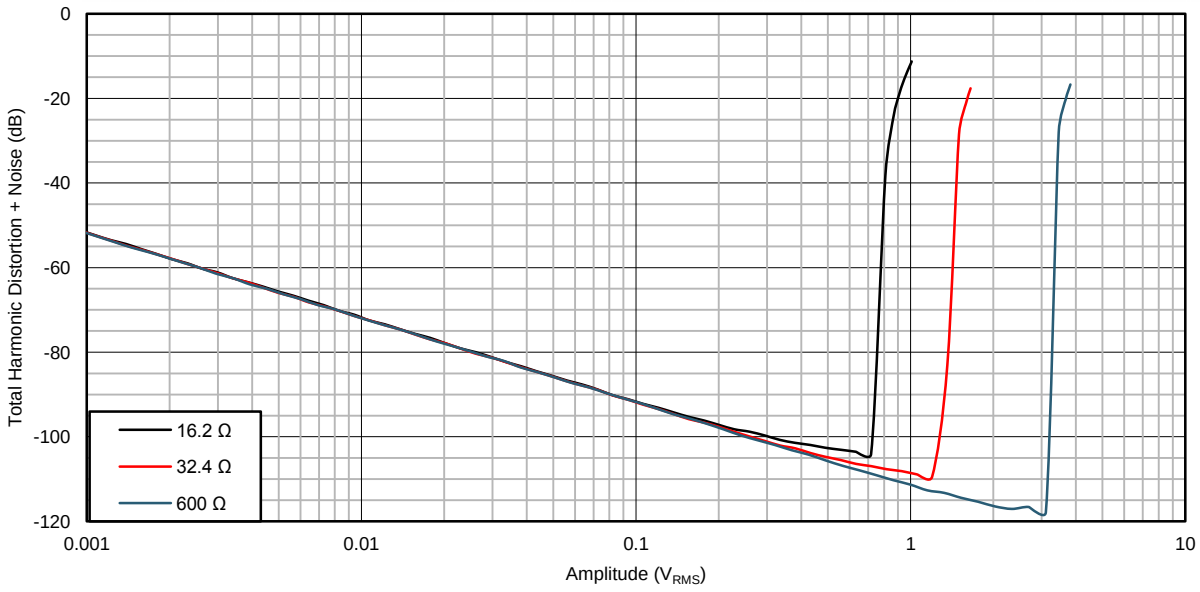


Figure 51. THD+N for Increasing Output Voltages Into Three Load Impedances (Input Signal = 1 kHz, Measurement Bandwidth = 22.4 kHz)

Typical Application (continued)

Table 4. Maximum Output Power and THD+N Before Clipping for Different Load Impedances

LOAD IMPEDANCE (Ω)	MAXIMUM OUTPUT POWER BEFORE CLIPPING (mW)	THD+N AT MAXIMUM OUTPUT POWER (dB)
16	32	–104.1
32	50	–109.5
600	16	–117.8

Figure 52, Figure 53, and Figure 54 further illustrate the exceptional performance of the OPA1688 as a headphone amplifier.

Figure 52 shows the THD+N over frequency for a 500-mV_{RMS} output signal into the same three load impedances previously tested.

Figure 53 and Figure 54 show the output spectrum of the OPA1688 at low (1 mW) and high (50 mW) output power levels into a 32-Ω load. The distortion harmonics in both cases are approximately 120 dB below the fundamental.

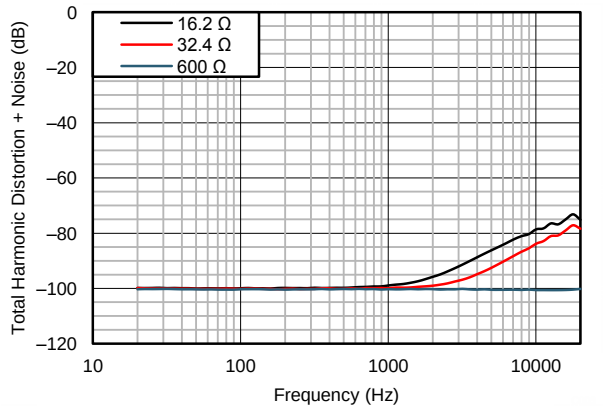


Figure 52. THD+N Measured over Frequency (90-kHz Measurement Bandwidth) for a 500-mV_{RMS} Output Level

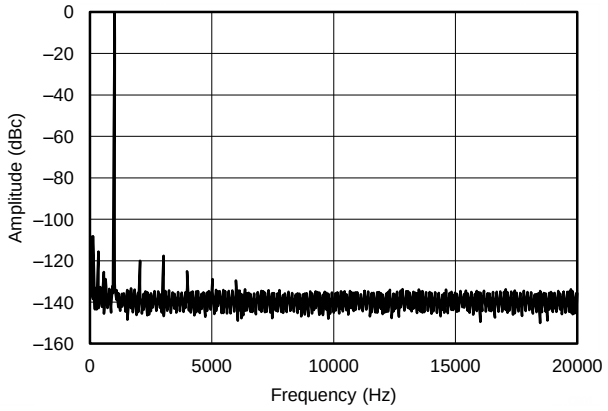


Figure 53. Output Spectrum of a 1-mW, 1-kHz Tone into a 32-Ω Load (The third harmonic is dominant at a level of –117.6 dB relative to the fundamental.)

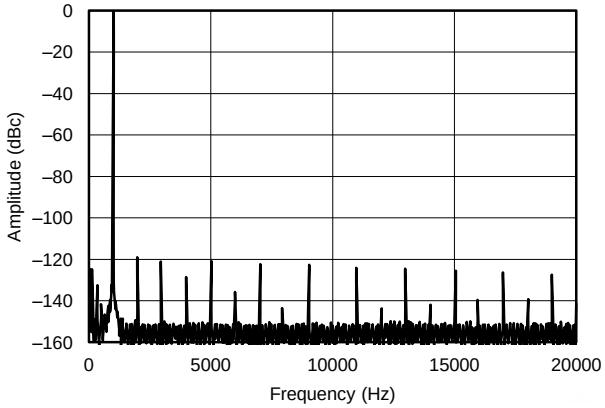


Figure 54. Output Spectrum of a 50-mW, 1-kHz Tone Into a 32-Ω Load, Immediately Below the Onset of Clipping (The highest harmonic is the second harmonic at –119 dB below the fundamental.)

11 Power Supply Recommendations

The OPA168x is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

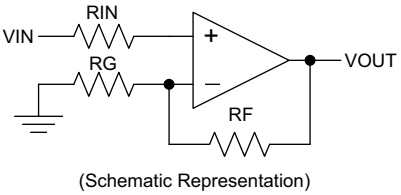
12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 55, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

12.2 Layout Example



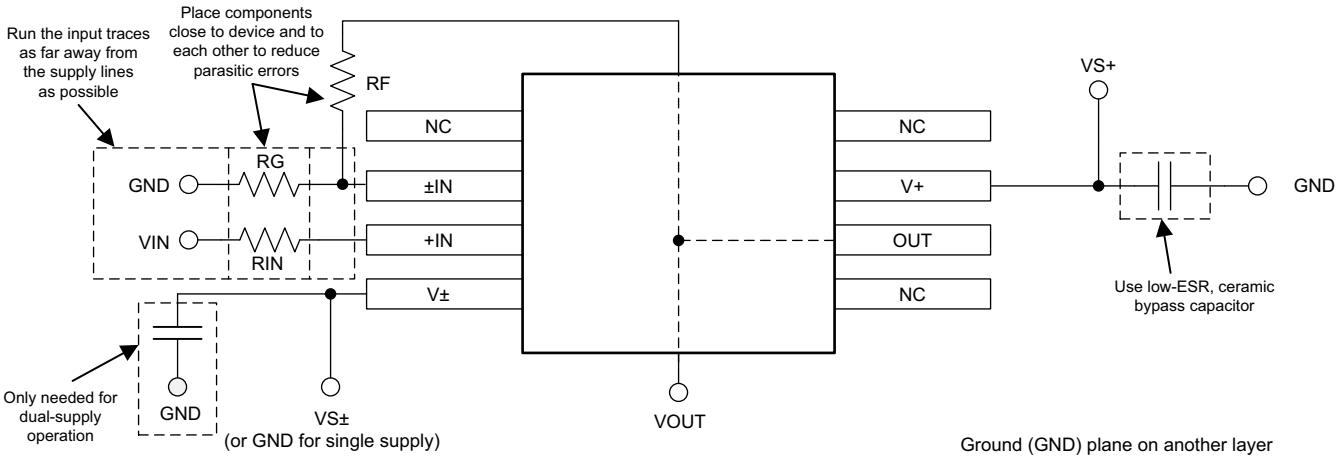


Figure 55. Operational Amplifier Board Layout for a Noninverting Configuration

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

13.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

13.2 Documentation Support

13.2.1 Related Documentation

SBOA015 (AB-028) — *Feedback Plots Define Op Amp AC Performance*

SBOA128 — *EMI Rejection Ratio of Operational Amplifiers*

SLOA089 — *Circuit Board Layout Techniques*

SLOD006 — *Op Amps for Everyone*

TIPD128 — *Capacitive Load Drive Solution using an Isolation Resistor*

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1688	Click here	Click here	Click here	Click here	Click here
OPA1689	Click here	Click here	Click here	Click here	Click here

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
SoundPlus is a trademark of Texas Instruments, Inc.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Blu-Ray is a trademark of Blu-ray Disc Association (BDA).
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1688ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1688A	Samples
OPA1688IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	O1688A	Samples
OPA1688IDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1688	Samples
OPA1688IDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1688	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

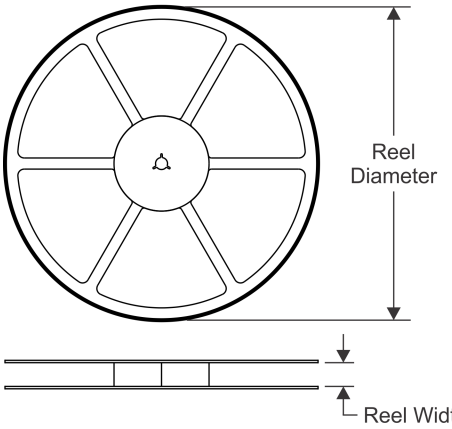
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

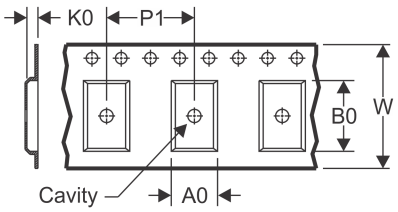
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

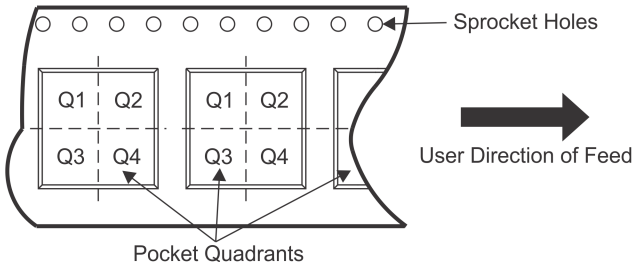


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

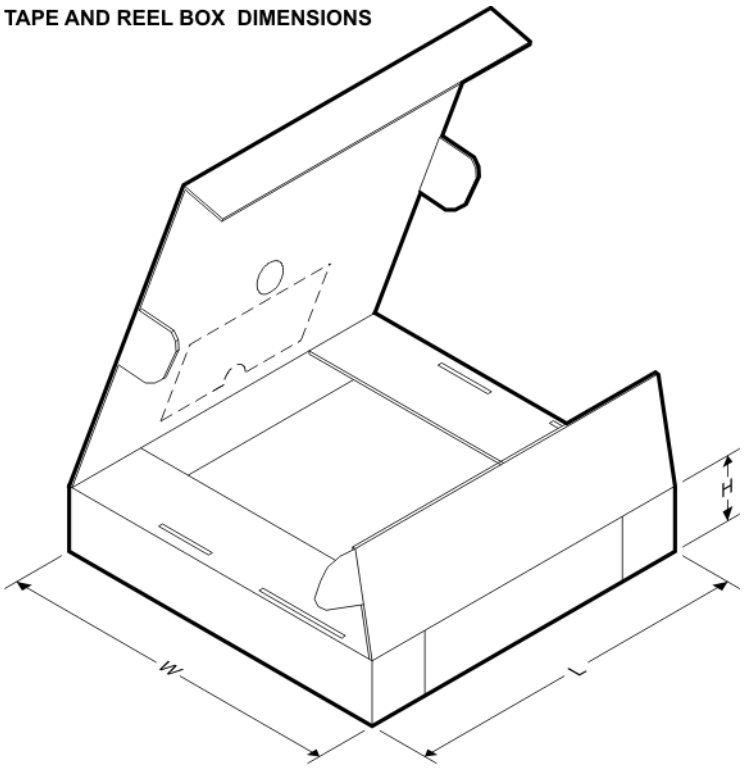
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

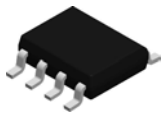
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1688IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1688IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA1688IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1688IDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1688IDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA1688IDRGT	SON	DRG	8	250	210.0	185.0	35.0

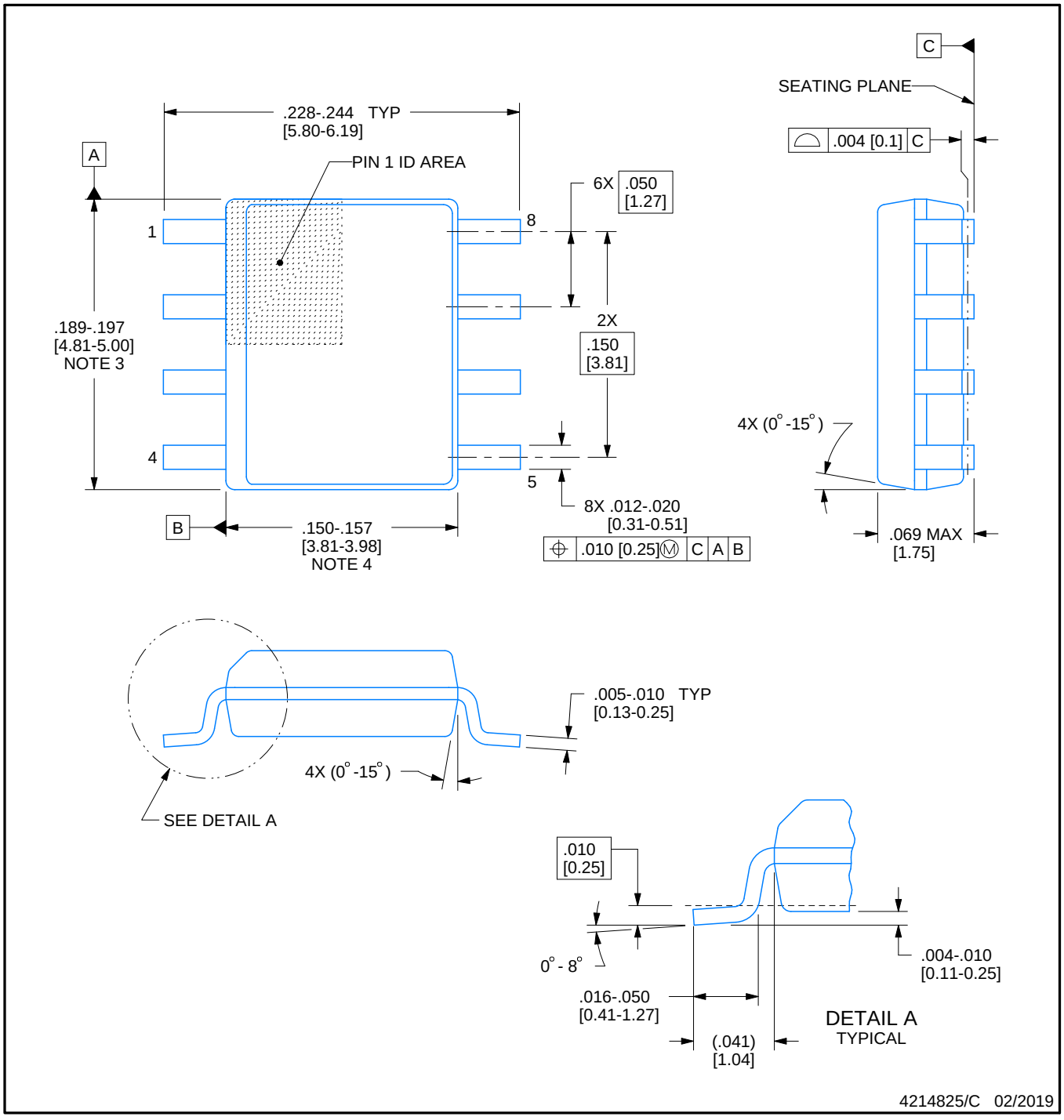


PACKAGE OUTLINE

D0008A

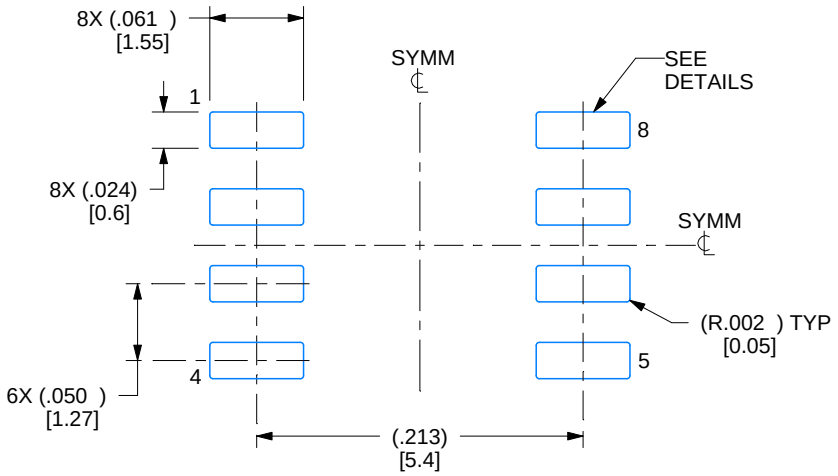
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

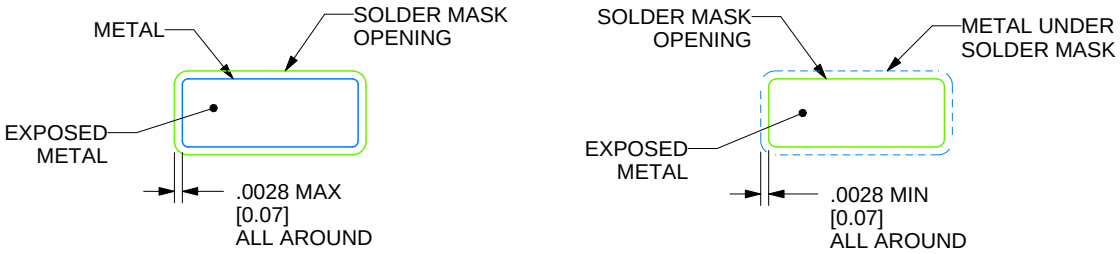


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

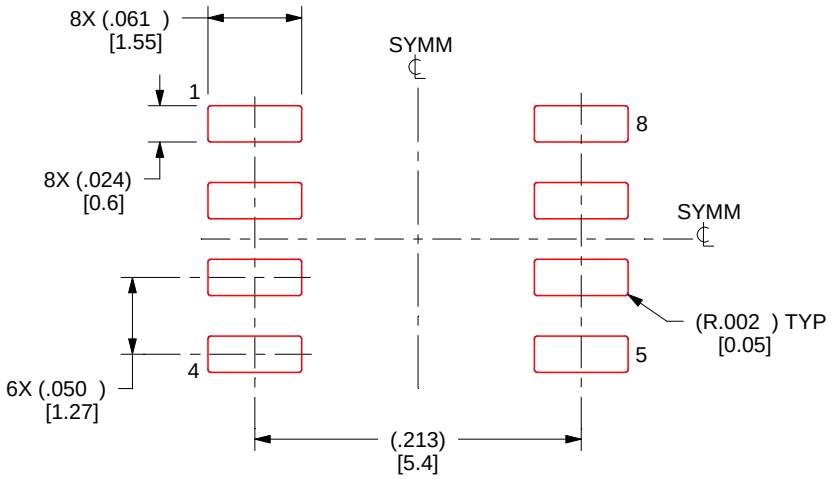
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



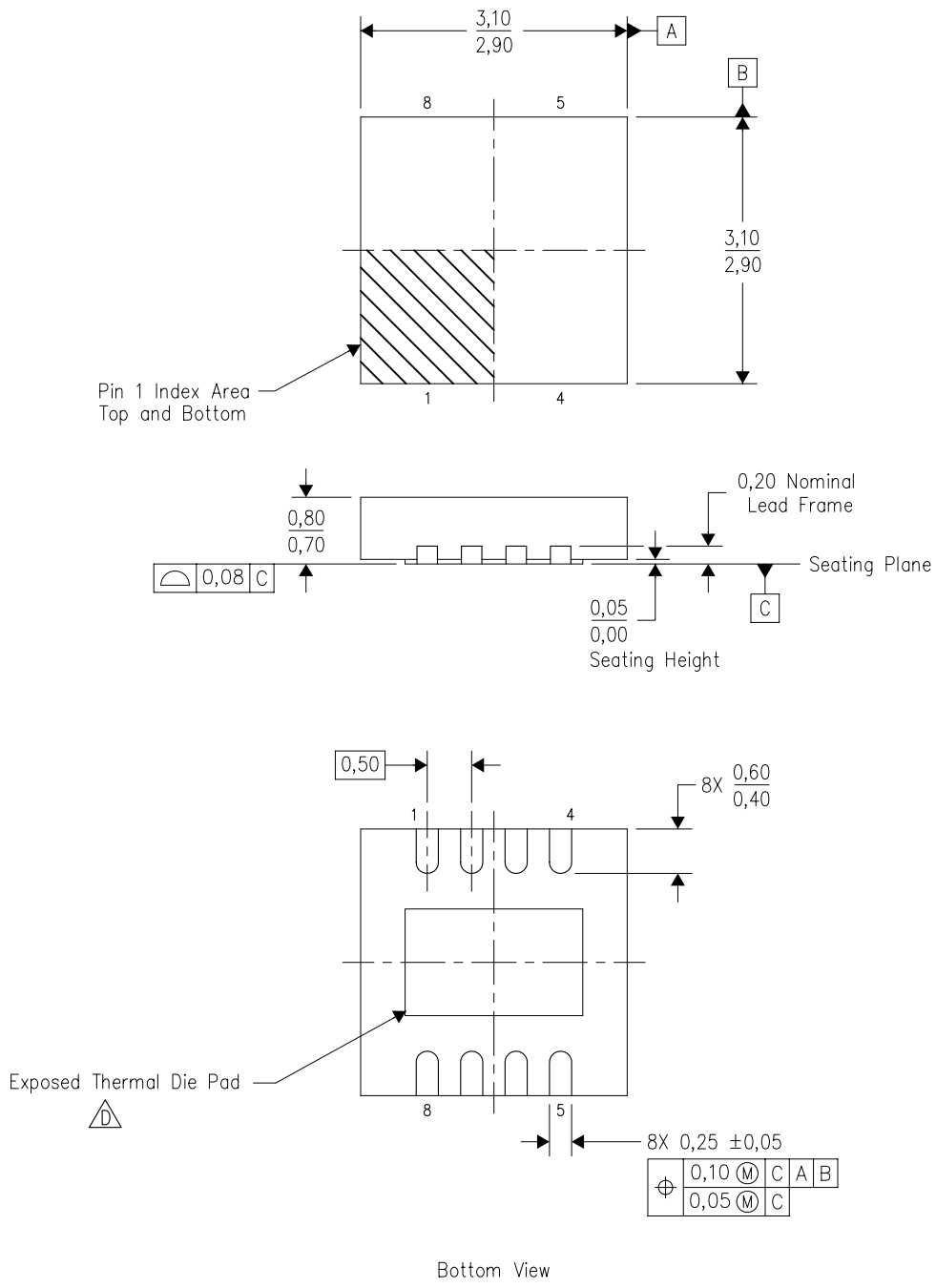
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

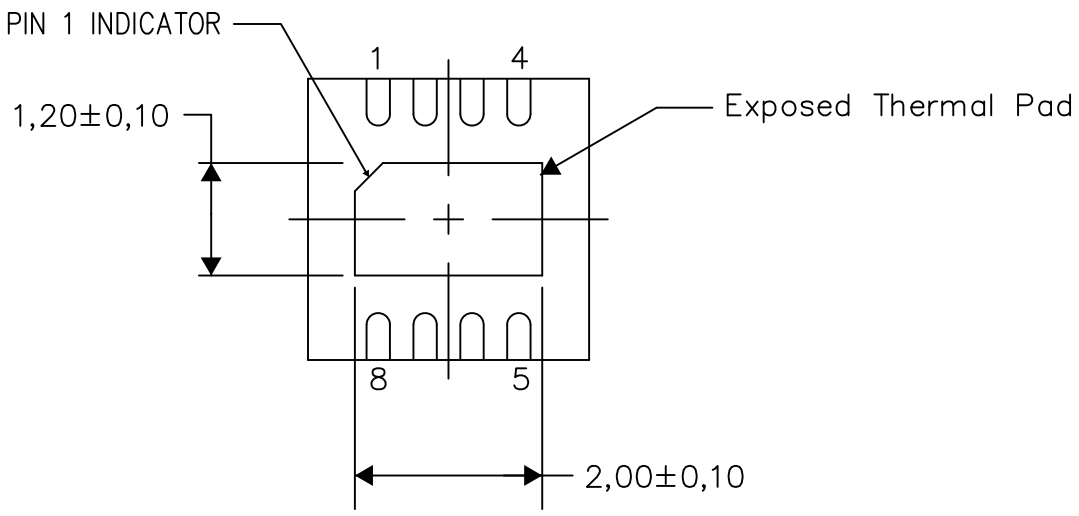
DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



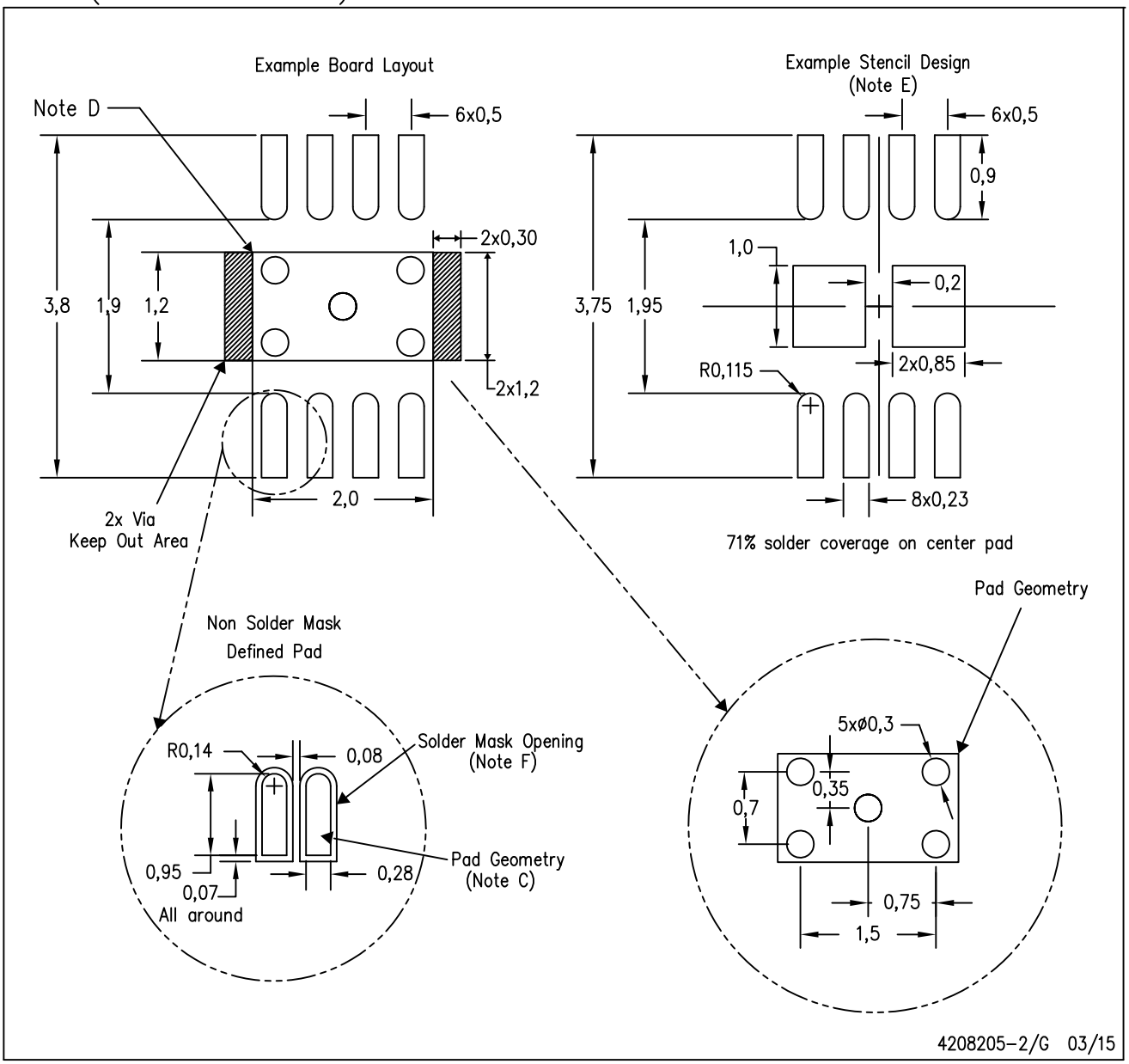
Bottom View

Exposed Thermal Pad Dimensions

4206881–2/I 03/15

NOTE: All linear dimensions are in millimeters

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–SM–782 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265