OPA1692 Low-Power, Low-Noise and Low-Distortion SoundPlus™ Audio Operational Amplifiers

1 Features

- Low Noise: 4.2 nV/√Hz at 1 kHz
- Low Distortion: –127 dB at 1 kHz
- Low Quiescent Current:
  650 µA per Channel
- Slew Rate: 23 V/µs
- Wide Gain Bandwidth: 5.1 MHz
- Unity-Gain Stable
- Rail-to-Rail Output
- Wide Supply Range:
  ±1.75 V to ±18 V, or 3.5 V to 36 V

2 Applications

- Wireless Microphones
- Wireless Audio Monitoring Systems
- Portable Radios and Headsets
- Portable Audio Effects Processors
- Portable Recording Systems
- USB Audio Peripherals

3 Description

The OPA169x operational amplifiers achieve a new level of performance for low-power amplifiers with a low 4.2-nV/√Hz noise density and distortion of –127 dB at 1 kHz. This op amps offer rail-to-rail output swing to within 200 mV of the power supplies with a 2-kΩ load, which increases headroom and maximizes dynamic range. These devices have a high output drive capability of ±50 mA.

The OPA169x operational amplifiers operate over a wide supply range of ±1.75 V to ±18 V, or 3.5 V to 36 V (on 650 µA of supply current per channel), are unity-gain stable, and provide excellent dynamic behavior over a wide range of load conditions.

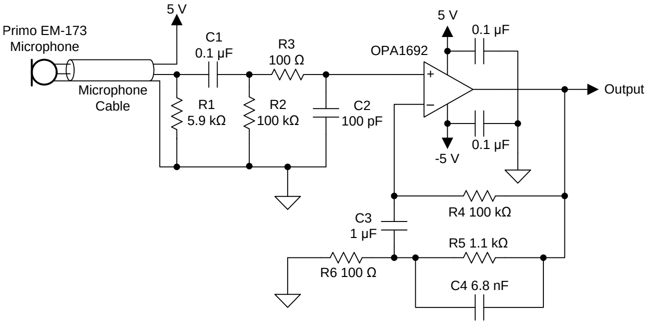
The OPA169x op amps are specified for a temperature range of –40°C to 125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA1692	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Preamplifier for 3-Wire Electret Microphones



THD + N vs Frequency (3 V_{RMS}, 2-kΩ Load)

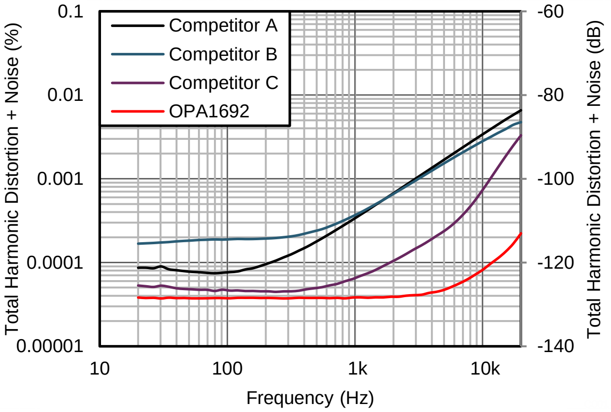


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

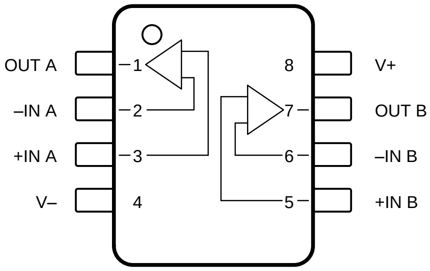
Changes from Revision B (September 2018) to Revision C	Page
• Changed -40℃ to 125℃ Iq to 975 µA	6

Changes from Revision A (December 2017) to Revision B	Page
• Changed I_{OS} VCM = 0 MAX from "±10" to "±15" nA	5
• Changed I_{OS} TA = –40°C to 125°C MAX from "±15" to "±20" nA.	5

Changes from Original (June 2017) to Revision A	Page
• Changed status of data sheet from Advance Information to Production Data	1

5 Pin Configuration and Functions

OPA1692 D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Not to scale

Pin Functions: OPA1692

PIN		I/O	DESCRIPTION
NAME	**NO.**		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage, V_S = (V+) – (V–)		40	V
	Input	(V–) – 0.5	(V+) + 0.5	
Current	Input (all pins except power-supply pins)	–10	10	mA
	Output short-circuit(2)	Continuous	Continuous	
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		200	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage	Single supply	3.5		36	V
		Split supply	±1.75		±18	
T_A	Operating temperature		–40		85	°C

6.4 Thermal Information: OPA1692

THERMAL METRIC(1)		OPA1692		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	123.6	162.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	56.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.0	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.0	6.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.3	81.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise	G = 1, f = 20 kHz, RL = 2kΩ, VO = 3 VRMS			-118		dB
		G = 1, f = 1 kHz, R_L = 2kΩ, V_O = 3 V_{RMS}			–127		dB
IMD	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	SMPTE/DIN two-tone, 4:1 (60 Hz and 7 kHz)		0.00005%		
	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}			-126		dB
	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	CCIF twin-tone (19 kHz and 20 kHz)		0.0002		
	Intermodulation distortion	G = 1, V_O = 3 V_{RMS}	CCIF twin-tone (19 kHz and 20 kHz)		-114		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = 100			5.1		MHz
SR	Slew rate	G = –1			23		V/µs
	Full power bandwidth (1)	V_O = 1 V_P			3.66		MHz
	Overload recovery time	G = –10			250		ns
	Channel separation (dual and quad)	f = 1 kHz			–145		dB
NOISE							
e_n	Input voltage noise	f = 0.1 to 10 Hz			130		nV_{PP}
e_n	Input voltage noise	f = 20 Hz to 20 kHz			3.9		$µV_{PP}$
	Input voltage noise density	f = 1 kHz			4.2		nV/rtHz
		f = 100 Hz			4.5		
I_n	Input current noise density	f = 1 kHz			0.37		pA/rtHz
		f = 100 Hz			0.4		
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±1.75 V to ±18 V			±0.25	±0.8	mV
V_{OS}	Input offset voltage	V_S = ±1.75 V to ±18 V				±1.0	mV
		V_S = ±1.75 V to ±18 V, T_A = –40°C to +125°C (2)			0.5	5	µV/°C
PSRR	Power-supply rejection ratio	V_S = ±1.75 V to ±18 V			0.1	1.5	µV/V
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C (2)				2.25	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			300	550	nA
		T_A = –40°C to +125°C				600	nA
I_{OS}	Input offset current	V_{CM} = 0 V			±2	±15	nA
		TA = –40°C to +125°C				±20	nA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 1.5		(V+) – 0.5	V
CMRR	Common-mode rejection ratio	(V–) + 1.5 V ≤ V_{CM} ≤ (V+) – 0.5 V			0.1	1	uV/V
CMRR	Common-mode rejection ratio	TA = –40°C to +125°C				4	uV/V
INPUT IMPEDANCE							
	Differential Resistance				350		kΩ
	Differential Capacitance				1.5		pF
	Common-Mode Resistance				350		MΩ
	Common-Mode Capacitance				1.6		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	TA = –40°C to +125°C		110	140		dB
A_{OL}	Open-loop voltage gain	(V–) + 0.2 V ≤ V_O ≤ (V+) – 0.2 V, R_L = 2 kΩ		120	140		dB

(1) Full-power bandwidth = SR / (2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.

Electrical Characteristics (continued)

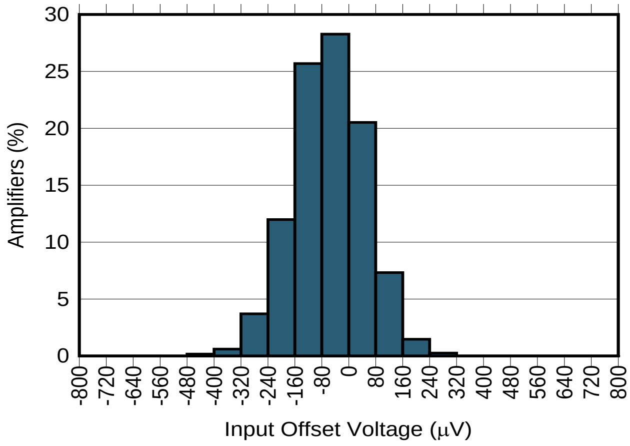
at T_A = 25°C, V_S = ±18 V, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	Voltage output	R_L = 2 kΩ	-17.8		17.8	V
I_{OUT}	Output current				See *Figure 46* , *Figure 47*	mA
Z_O	Open-loop output impedance				See *Figure 14*	Ω
I_{SC}	Short-circuit current(3)			±50		mA
C_{LOAD}	Capacitive load drive			200		pF
POWER SUPPLY						
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A		650	750	µA
		I_{OUT} = 0 A, T_A = –40°C to +125°C(2)		650	975	µA

(3) One channel at a time.

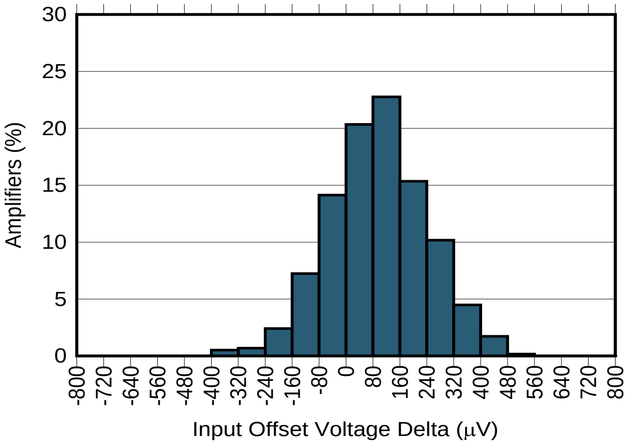
6.6 Typical Characteristics

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)



N = 1160 Mean = –139.2 µV Std. Dev. = 105.4 µV

Figure 1. Input Offset Voltage Distribution



N = 580 Mean = 17 µV Std. Dev. = 145.2 µV

Figure 2. Input Offset Voltage Matching (Ch. A – Ch. B)

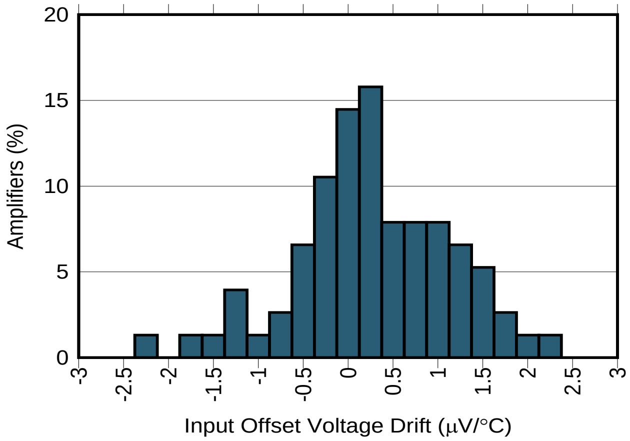
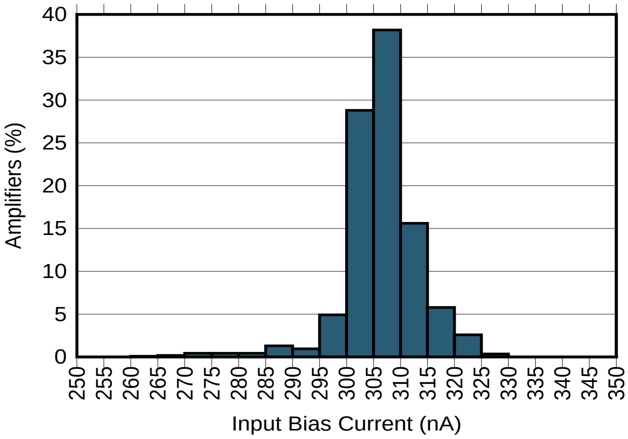
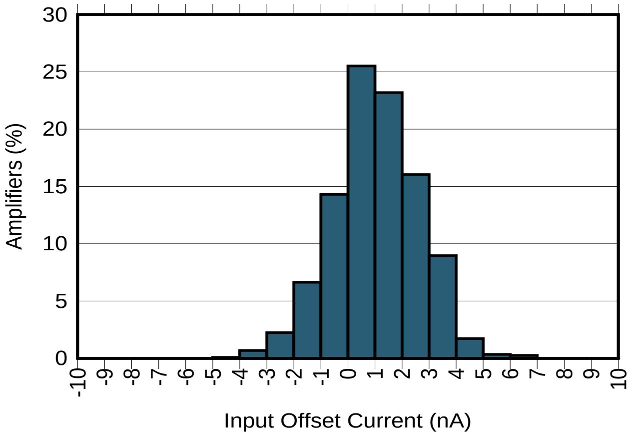


Figure 3. Offset Voltage Drift Distribution



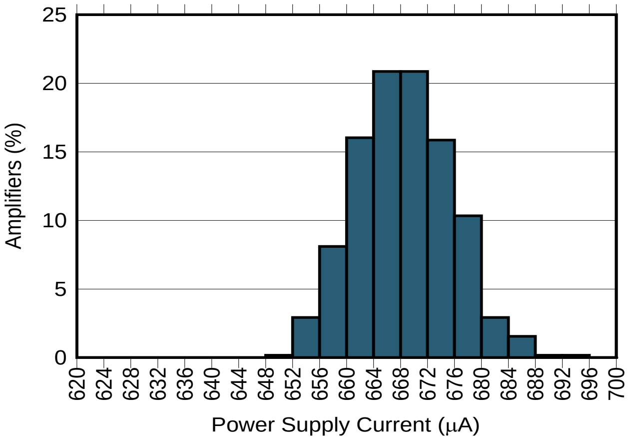
N = 1160 Mean = 301.5 nA Std. Dev. = 7.03 nA

Figure 4. Input Bias Current Distribution



N = 1160 Mean = 0.07 nA Std. Dev. = 1.58 nA

Figure 5. Input Offset Current Distribution



N = 1160 Mean = 664.6 µA Std. Dev. = 6.98 µA

Figure 6. Power Supply Current Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

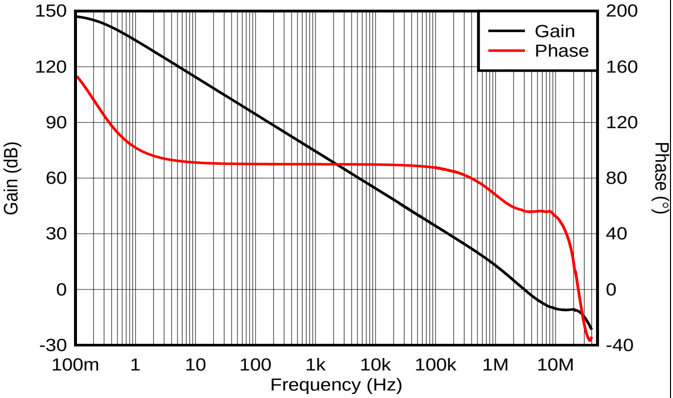


Figure 7. Open-Loop Gain and Phase vs Frequency

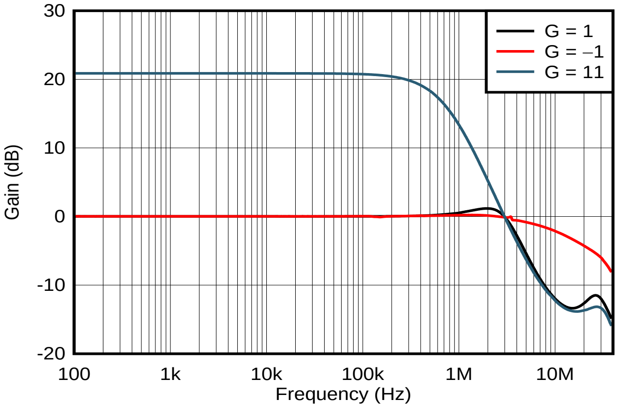


Figure 8. Closed-Loop Gain vs Frequency

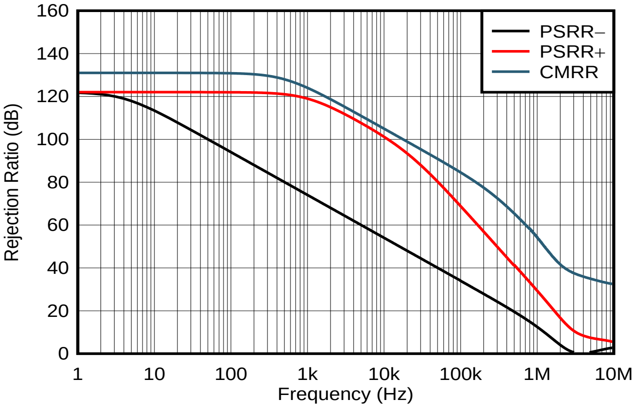


Figure 9. CMRR and PSRR vs Frequency (Referred to Input)

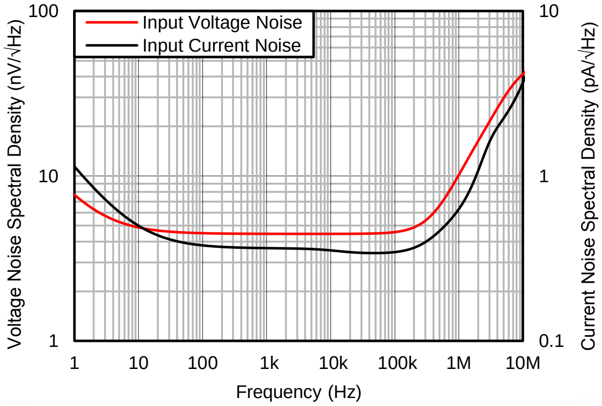


Figure 10. Input Voltage Noise Spectral Density

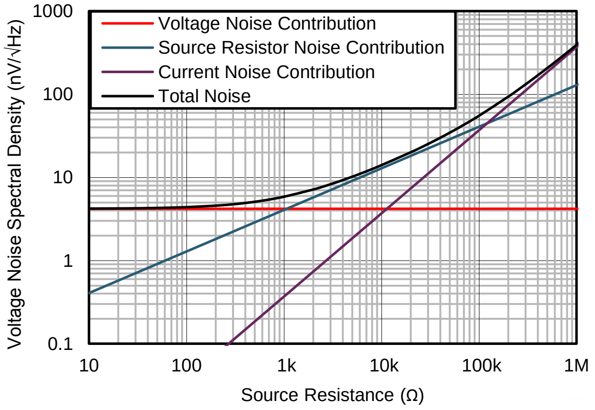


Figure 11. Voltage Noise vs Source Resistance

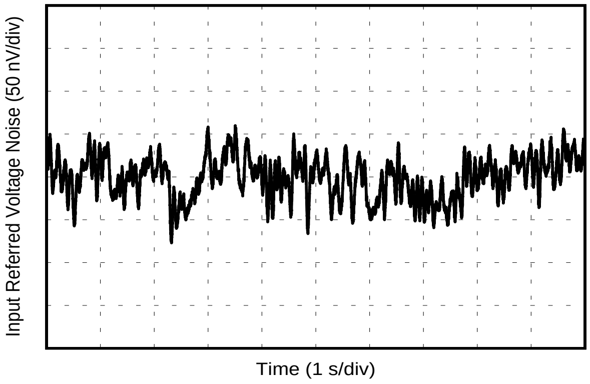


Figure 12. 0.1-Hz to 10-Hz Voltage Noise

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

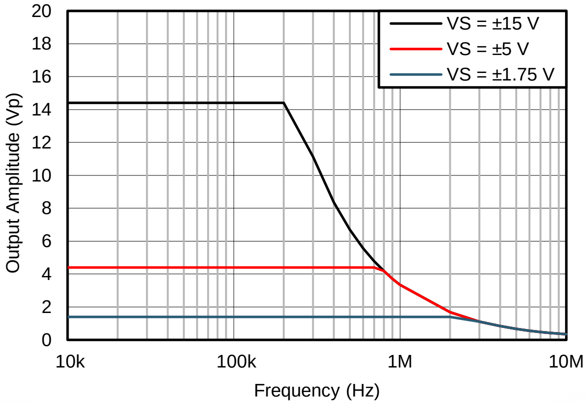


Figure 13. Maximum Output Voltage vs Frequency

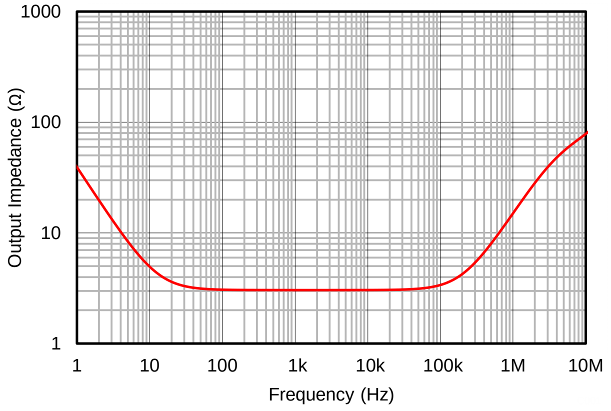
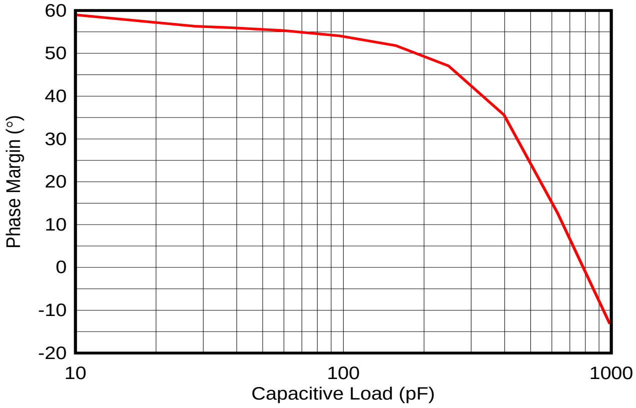
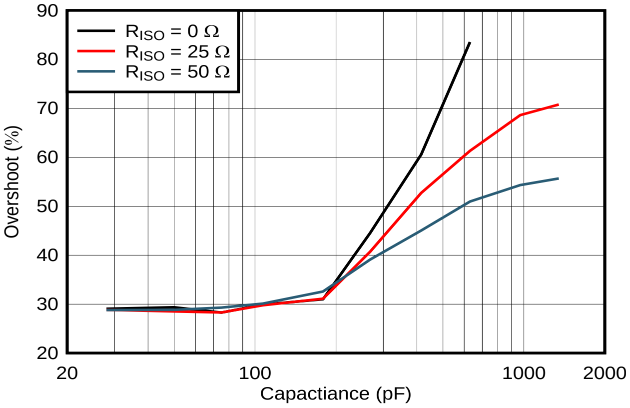


Figure 14. Open-Loop Output Impedance vs Frequency



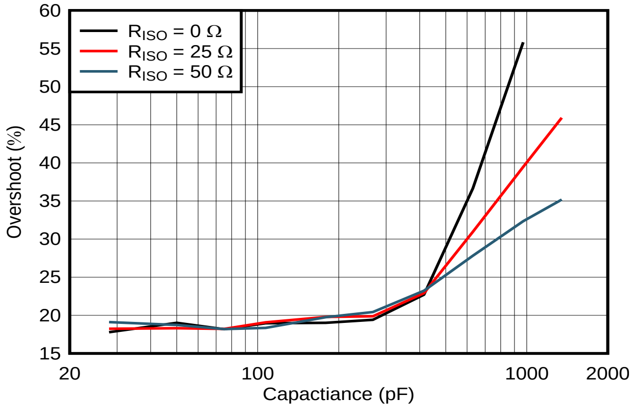
G = 1

Figure 15. Phase Margin vs Capacitive Load



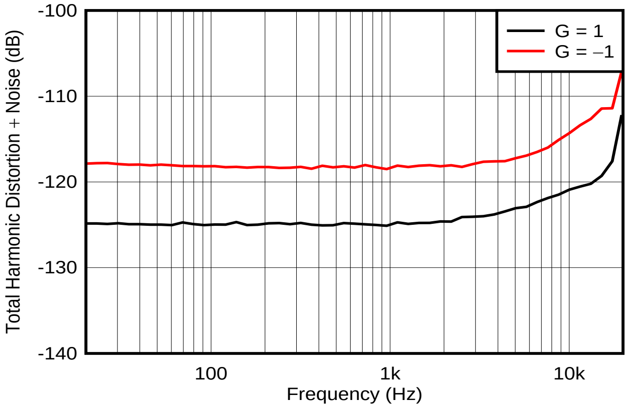
G = 1 10-mV input step

Figure 16. Overshoot vs Capacitive Load



G = –1 10-mV input step

Figure 17. Overshoot vs Capacitive Load

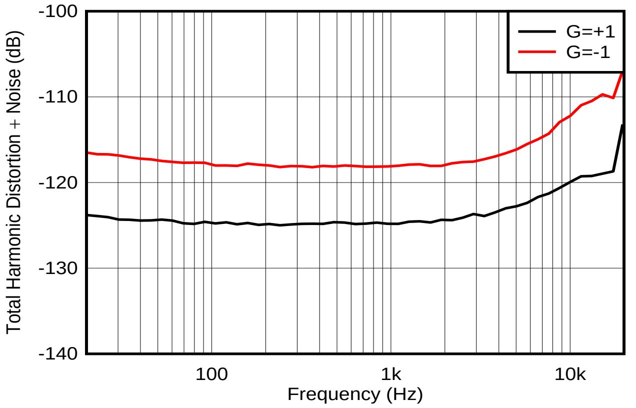


V_{OUT} = 3 V_{RMS} 80-kHz bandwidth

Figure 18. THD + N Ratio vs Frequency

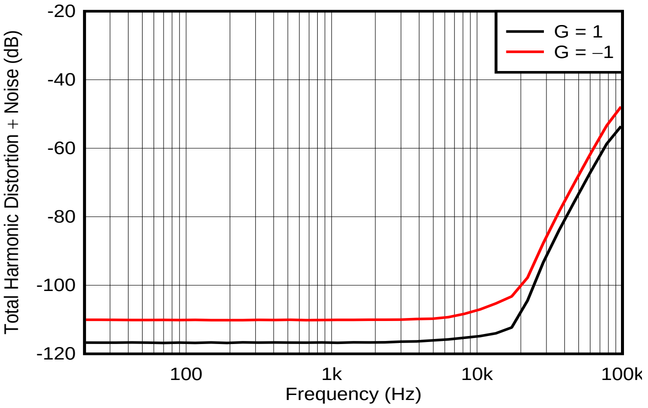
Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)



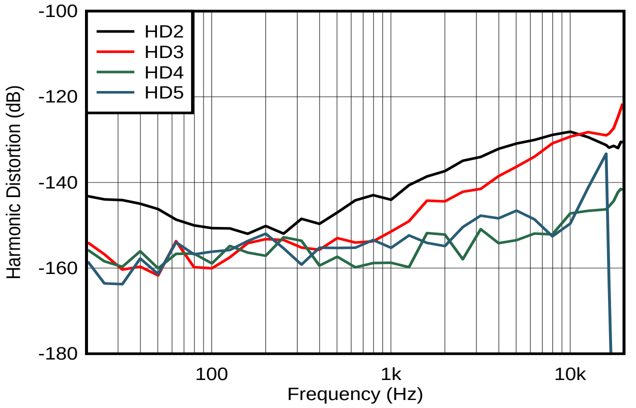
V_{OUT} = 3 V_{RMS} R_L = 600 Ω 80-kHz bandwidth

Figure 19. THD + N Ratio vs Frequency



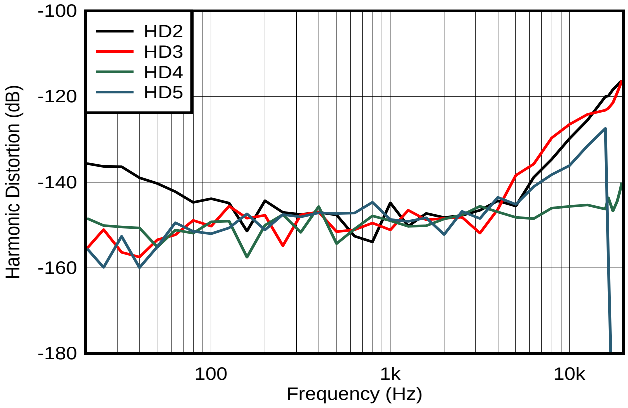
V_{OUT} = 3 V_{RMS} 500-kHz bandwidth

Figure 20. THD + N Ratio vs Frequency



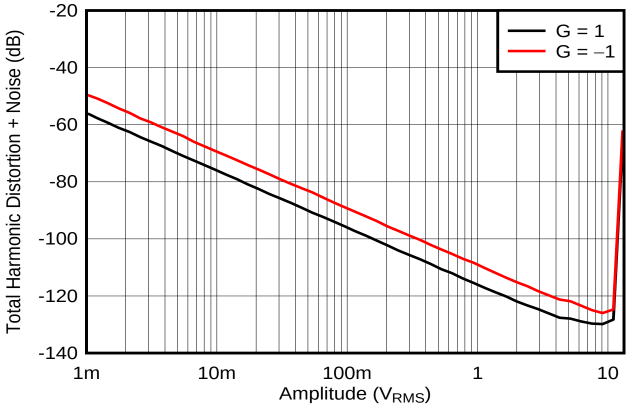
V_{OUT} = 3 V_{RMS} G = 1 80-kHz bandwidth

Figure 21. Distortion Harmonics vs Frequency



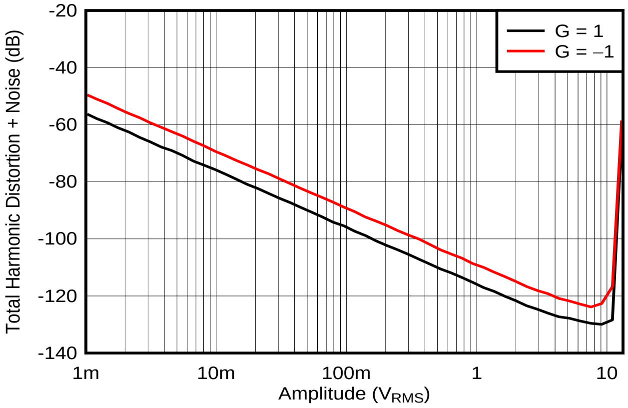
V_{OUT} = 3 V_{RMS} G = –1 80-kHz bandwidth

Figure 22. Distortion Harmonics vs Frequency



f = 1 kHz 80-kHz bandwidth

Figure 23. THD + N Ratio vs Output Amplitude

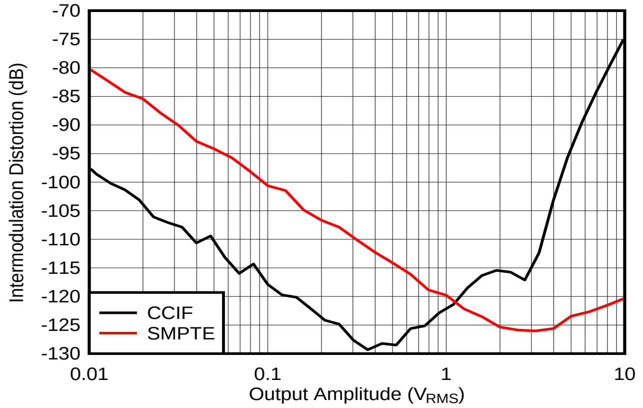


f = 1 kHz R_L = 600 Ω 80-kHz bandwidth

Figure 24. THD + N Ratio vs Output Amplitude

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)



80-kHz bandwidth

Figure 25. Intermodulation Distortion vs Output Amplitude

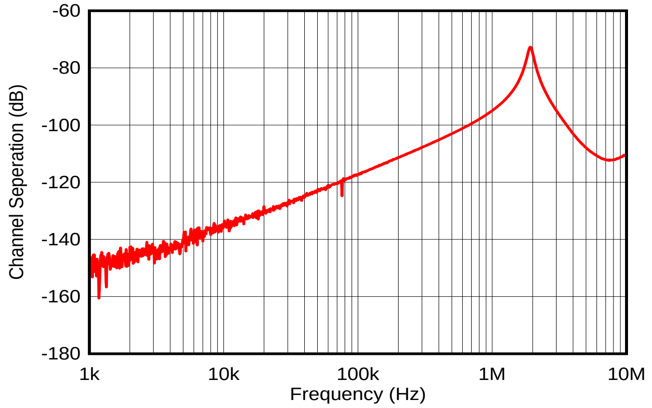
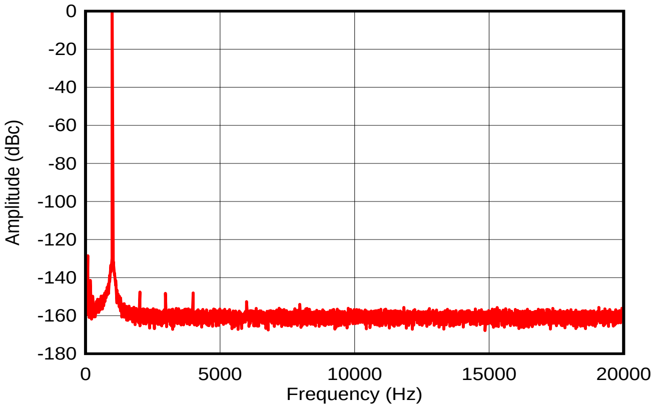
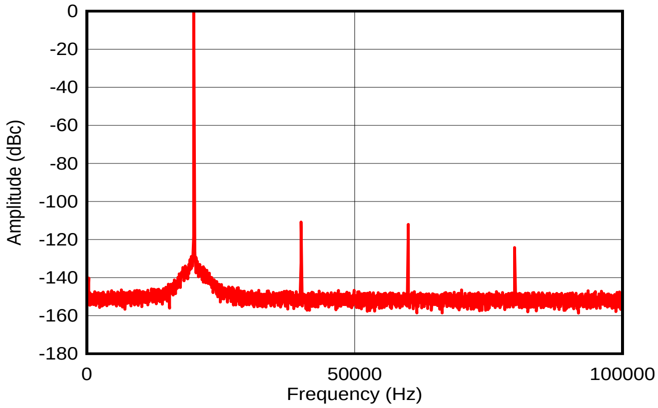


Figure 26. Channel Separation vs Frequency



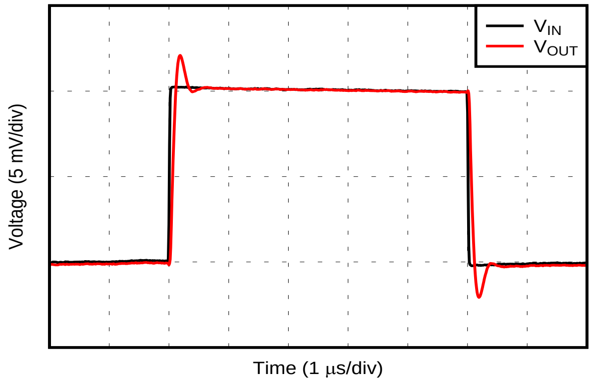
f = 1 kHz V_O = 3 V_{RMS} R_L = 600 Ω

Figure 27. 1-kHz Output Spectrum



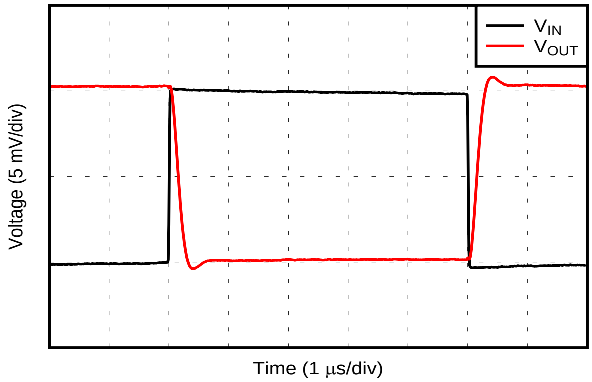
f = 20 kHz V_O = 3 V_{RMS} R_L = 600 Ω

Figure 28. 20-kHz Output Spectrum



100-pF capacitive load 10-mV input step G = 1

Figure 29. Small-Signal Step Response

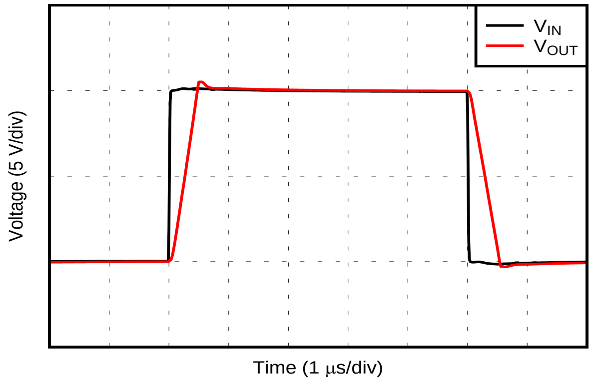


100-pF capacitive load 10-mV input step G = –1

Figure 30. Small-Signal Step Response

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

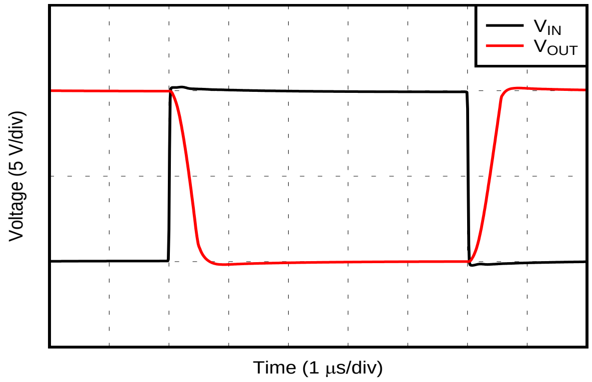


100-pF capacitive load

10-V input step

G = 1

Figure 31. Large-Signal Step Response



100-pF capacitive load

10-V input step

G = –1

Figure 32. Large-Signal Step Response

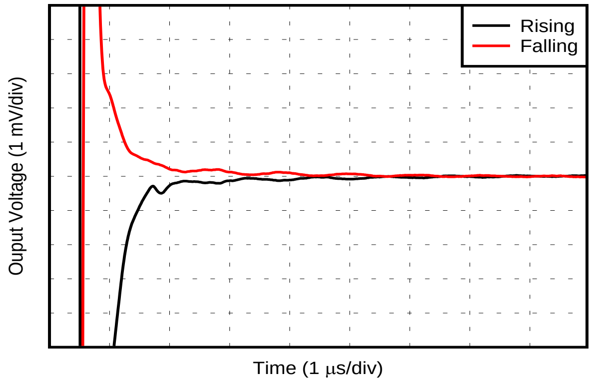
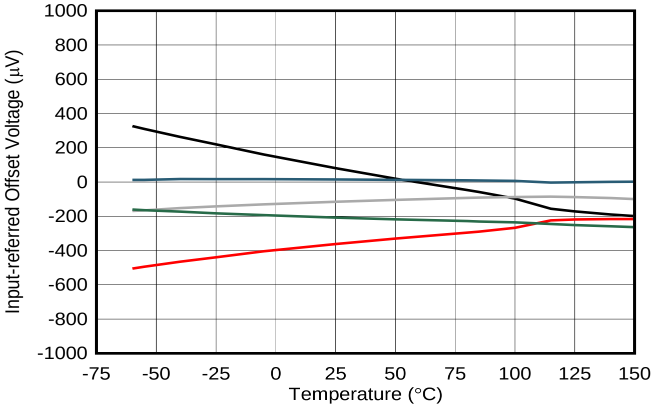
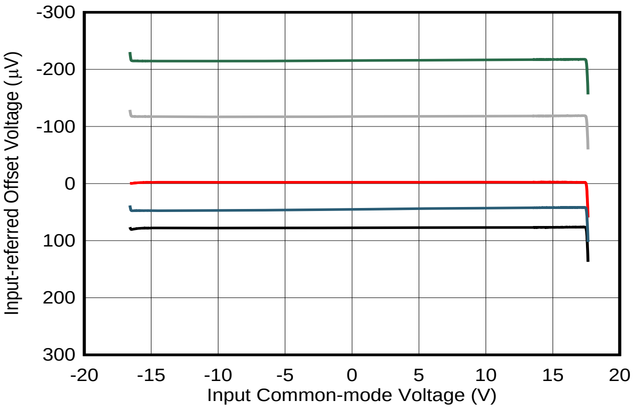


Figure 33. Settling Time



5 typical units

Figure 34. Input Offset Voltage vs Temperature



5 typical units

Figure 35. Input Offset Voltage vs Common-Mode Voltage

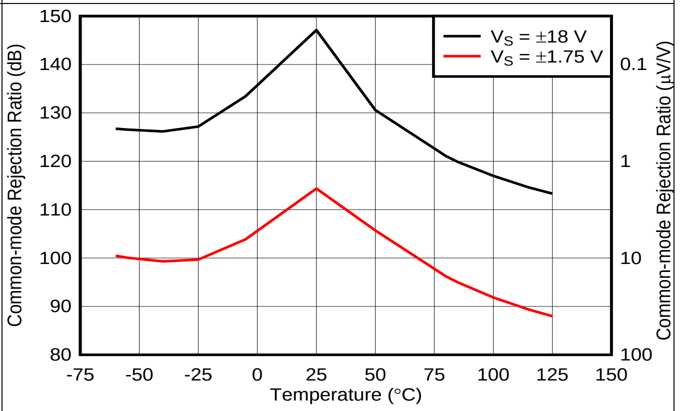


Figure 36. CMRR vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

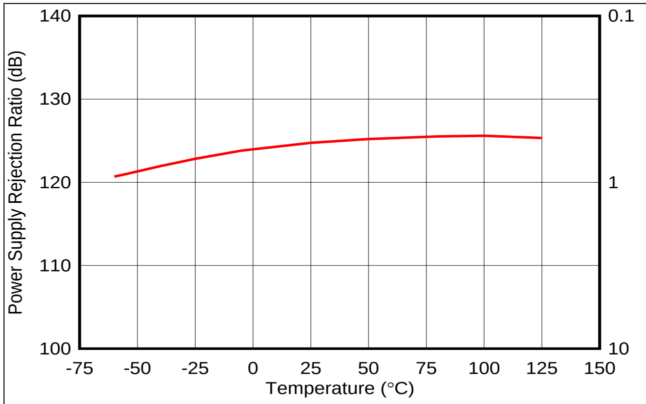


Figure 37. PSRR vs Temperature

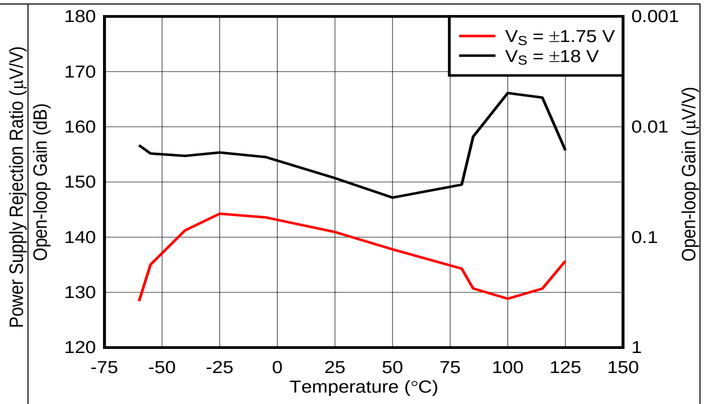


Figure 38. Open-Loop Gain vs Temperature

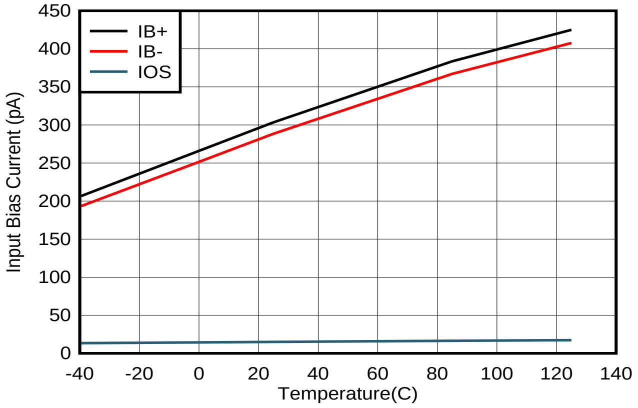


Figure 39. Input Bias and Offset Current vs Temperature

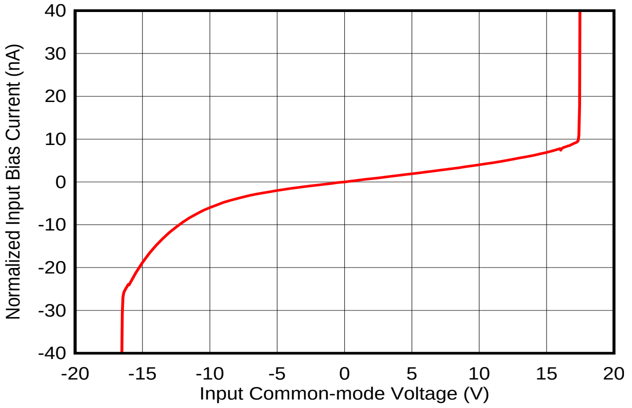
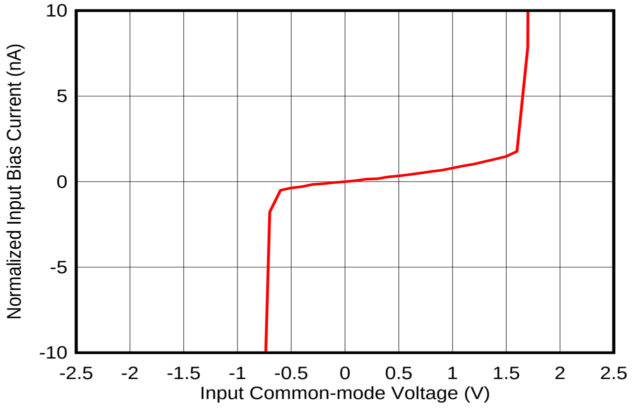


Figure 40. I_B vs Common-Mode Voltage



V_S = ±1.75 V

Figure 41. I_B vs Common-Mode Voltage

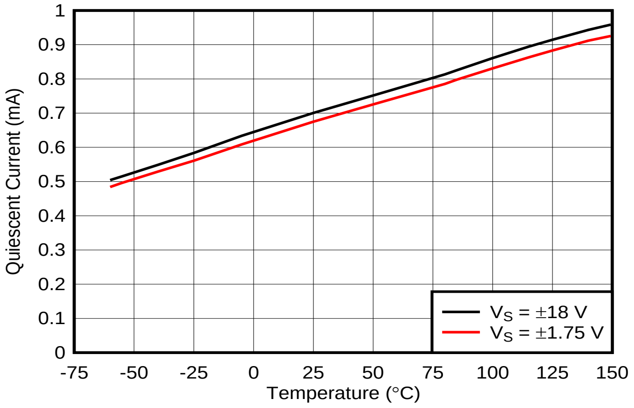


Figure 42. Supply Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

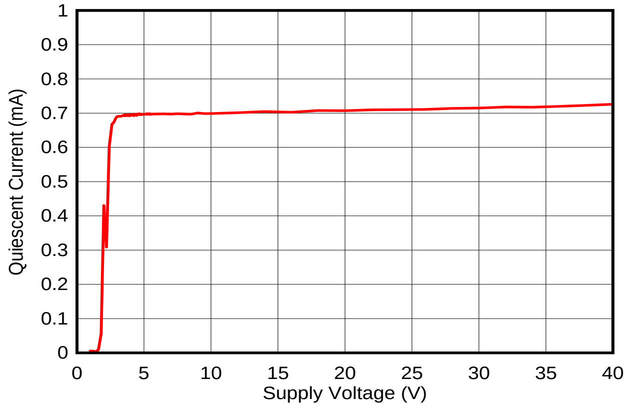


Figure 43. Supply Current vs Supply Voltage

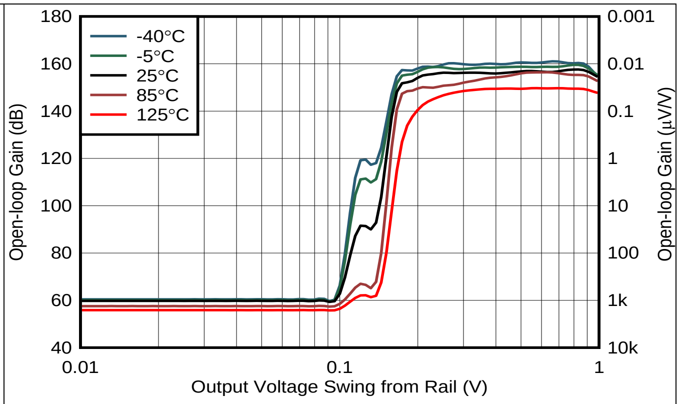
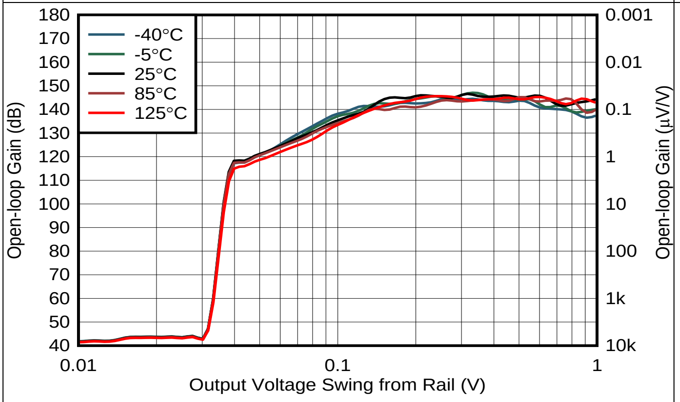
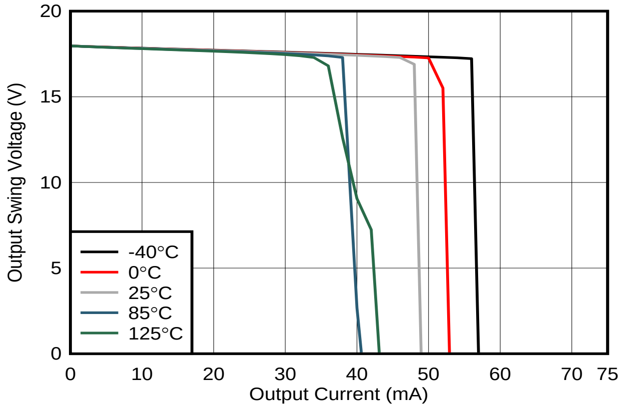


Figure 44. Open-Loop Gain vs Output Voltage



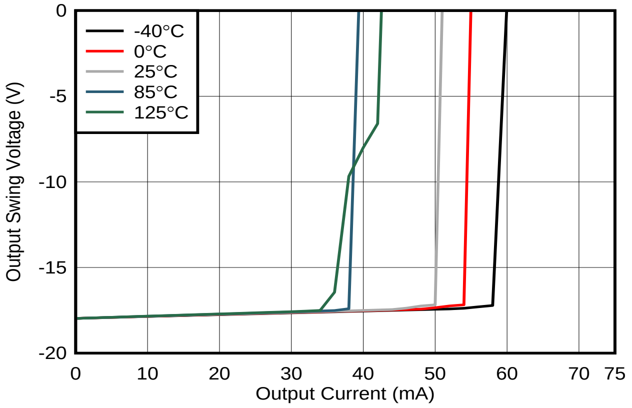
V_S = ±1.75 V

Figure 45. Open-Loop Gain vs Output Voltage



Sourcing

Figure 46. Output Voltage vs Output Current



Sinking

Figure 47. Output Voltage vs Output Current

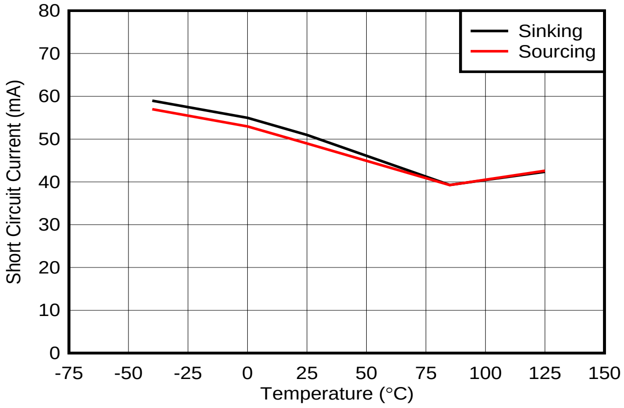


Figure 48. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = ±18 V, and R_L = 2 kΩ (unless otherwise noted)

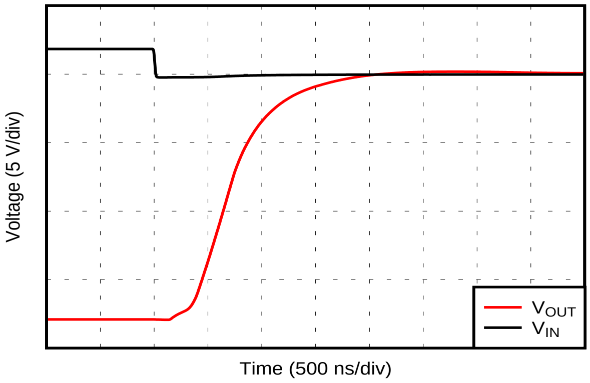


Figure 49. Negative Overload Recovery

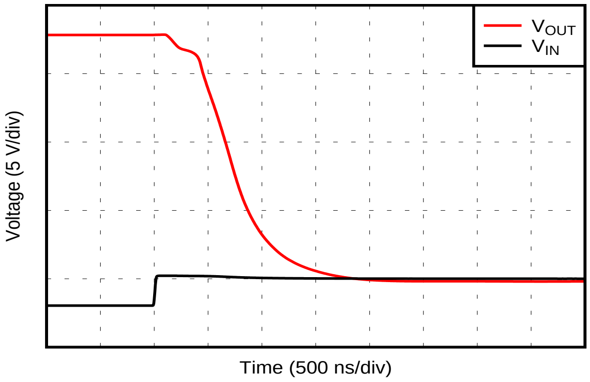


Figure 50. Positive Overload Recovery

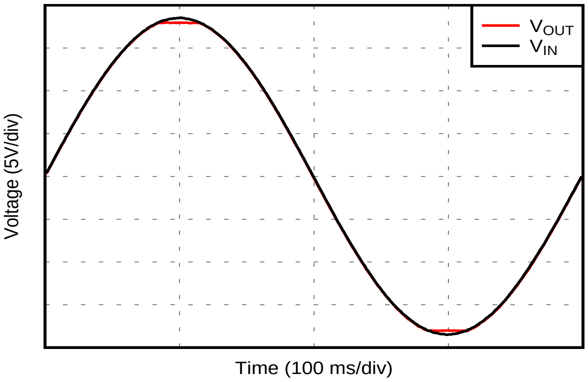


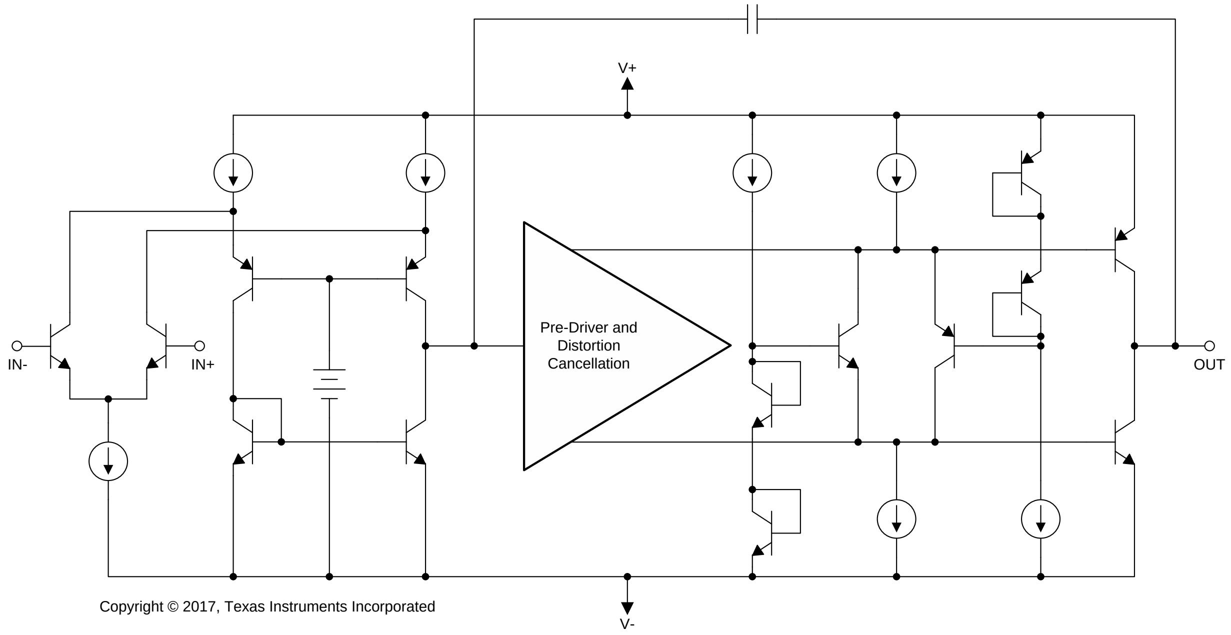
Figure 51. No Phase Reversal

7 Detailed Description

7.1 Overview

The OPA169x amplifiers are unity-gain stable, dual and quad op amps with low noise. The *Functional Block Diagram* shows a simplified schematic of the OPA169x (one channel shown). The device consists of a very low noise input stage with a folded cascode and a rail-to-rail output stage. A proprietary distortion reduction technology allows the OPA169x family of amplifiers to achieve significantly lower distortion than other op amps that consume the equal or greater power supply current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Distortion Reduction

Amplifiers use feedback to reduce the amount of distortion they introduce to the signal path. Increasing the amount of feedback available for distortion reduction typically requires an increase in the power supply current of the amplifier. This is not acceptable in low-power amplifiers targeting applications that require low distortion.

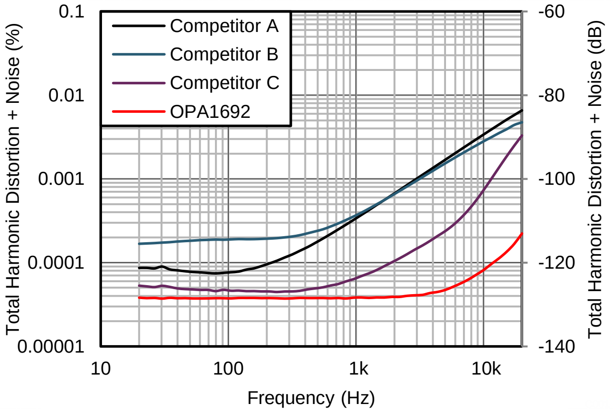


Figure 53. Comparison of THD + N vs Frequency for Multiple Low-Power Amplifiers

Feature Description (continued)

The OPA169x family of amplifiers uses a proprietary technology to reduce signal distortion that does not increase the power supply current. The distortion cancellation technique reduces odd-order harmonic distortion, which is produced by the input transistor pair of the amplifier. As Figure 53 shows, the impact to THD + N is significant, especially at high frequencies where the OPA169x devices exhibit over 30-dB lower distortion than competitor amplifiers at similar power supply current levels.

7.3.2 Phase Reversal Protection

The OPA169x family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, reverses the output into the opposite rail. The input of the OPA169x prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in Figure 54.

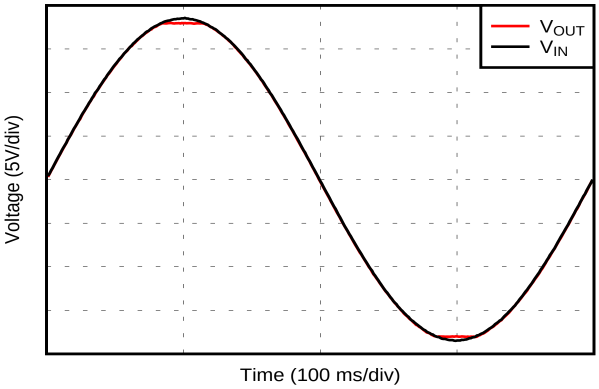


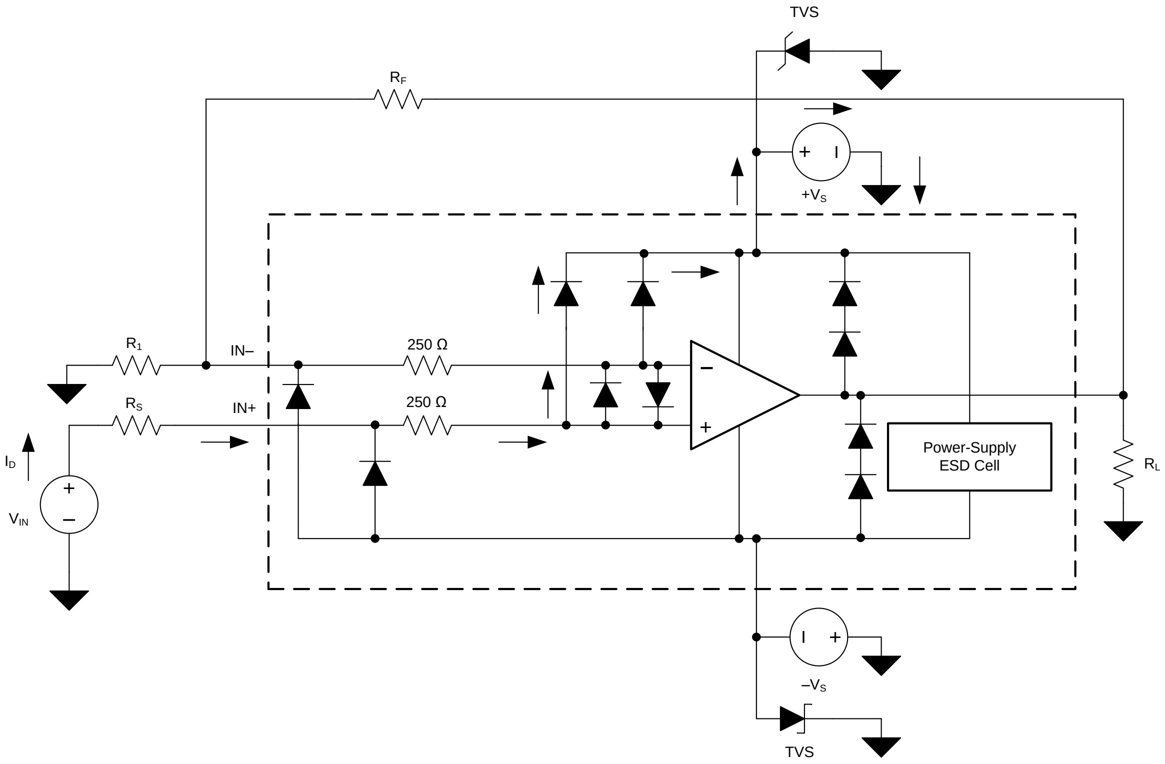
Figure 54. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

7.3.3 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. Figure 55 illustrates the ESD circuits contained in the OPA169x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

Feature Description (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 55. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA169x but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (see Figure 55), the ESD protection components are intended to remain inactive and are not involved in the application-circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

Figure 55 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Feature Description (continued)

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. This question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see Figure 55. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe operating, supply voltage level.

7.4 Device Functional Modes

7.4.1 Operating Voltage

The OPA169x series op amps operate from ±1.75 V to ±18 V supplies while maintaining excellent performance. The OPA169x series operates with as little as 3.5 V between the supplies and with up to 36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA169x series, power-supply voltages are not required to be equal. For example, the positive supply can be set to 25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. Key parameters are assured over the specified temperature range of T_A = –40°C to 125°C. Parameters that vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Capacitive Loads

The dynamic characteristics of the OPA169x amplifiers are optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. Add a small resistor (R_S equal to 50 Ω, for example) in series with the output to isolate heavier capacitive loads.

8.1.2 Noise Performance

Figure 56 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The op amp itself contributes a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA169x has low voltage noise and low current noise. As a result, the current noise contribution of the OPA169x series is negligible for source impedances less than 100 kΩ.

Figure 56 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see *Basic Noise Calculations*.

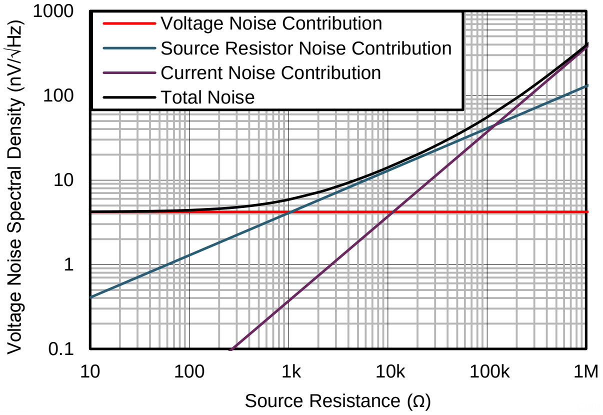


Figure 56. Noise Performance of the OPA169x in a Unity-Gain Buffer Configuration

Application Information (continued)

8.1.3 Basic Noise Calculations

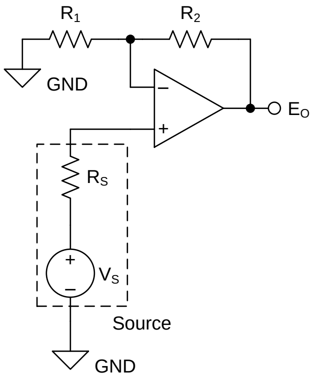
Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 56. The source impedance is typically fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 57 shows noninverting **(A)** and inverting **(B)** op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components.

The selected feedback resistor values make these noise sources negligible. Low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.

(A) Noise in Noninverting Gain Configuration



Noise at the output is given as E_O, where

$$(1)\quad E_O = \left(1+\frac{R_2}{R_1}\right)\cdot\sqrt{(e_S)^2+(e_N)^2+\left(e_{R_1\|R_2}\right)^2+(i_N\cdot R_S)^2+\left(i_N\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]\right)^2}\quad [V_{RMS}]$$

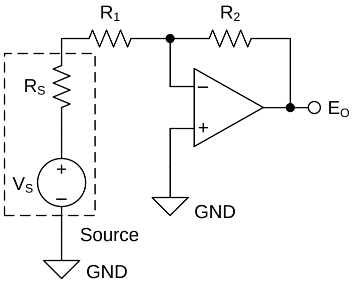
$$(2)\quad e_S=\sqrt{4\cdot k_B\cdot T(K)\cdot R_S}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of R_S

$$(3)\quad e_{R_1\|R_2}=\sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{R_1\cdot R_2}{R_1+R_2}\right]}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $R_1 \| R_2$

$$(4)\quad k_B=1.38065\cdot 10^{-23}\quad\left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(5)\quad T(K)=237.15+T(°C)\quad [K]$$ Temperature in kelvins

(B) Noise in Inverting Gain Configuration



Noise at the output is given as E_O, where

$$(6)\quad E_O=\left(1+\frac{R_2}{R_S+R_1}\right)\cdot\sqrt{(e_N)^2+\left(e_{R_1+R_S\|R_2}\right)^2+\left(i_N\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]\right)^2}\quad [V_{RMS}]$$

$$(7)\quad e_{R_1+R_S\|R_2}=\sqrt{4\cdot k_B\cdot T(K)\cdot\left[\frac{(R_S+R_1)\cdot R_2}{R_S+R_1+R_2}\right]}\quad\left[\frac{V}{\sqrt{Hz}}\right]$$ Thermal noise of $(R_1 + R_S) \| R_2$

$$(8)\quad k_B=1.38065\cdot 10^{-23}\quad\left[\frac{J}{K}\right]$$ Boltzmann Constant

$$(9)\quad T(K)=237.15+T(°C)\quad [K]$$ Temperature in kelvins

(1) e_N is the voltage noise of the amplifier. For the OPAx169x series of operational amplifiers, $e_N = 4.2\ nV/\sqrt{Hz}$ at 1 kHz.

(2) i_N is the current noise of the amplifier. For the OPA169x series of operational amplifiers, $i_N = 370\ fA/\sqrt{Hz}$ at 1 kHz.

(3) For additional resources on noise calculations, see *TI's Precision Labs Series*.

Figure 57. Noise Calculation in Gain Configurations

Application Information (continued)

8.1.4 EMI Rejection

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many op amps is a change in the offset voltage as a result of RF signal rectification. An op amp that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the op amp. In general, only the noninverting input is tested for EMIRR for the following three reasons:

- Op amp input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
- The noninverting and inverting op amp inputs have symmetrical physical layouts and exhibit approximately matching EMIRR performance
- EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input pin can be isolated on a PCB. This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

High-frequency signals conducted or radiated to any pin of the operational amplifier result in adverse effects, as the amplifier does not have sufficient loop gain to correct for signals with spectral content outside its bandwidth. Conducted or radiated EMI on inputs, power supply, or output may result in unexpected DC offsets, transient voltages, or other unknown behavior. Take care to properly shield and isolate sensitive analog nodes from noisy radio signals and digital clocks and interfaces.

The EMIRR IN+ of the OPA169x amplifiers is plotted versus frequency as shown in Figure 58. If available, any dual and quad op amp device versions have nearly similar EMIRR IN+ performance. The OPA169x unity-gain bandwidth is 5.1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the op amp bandwidth.

See *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

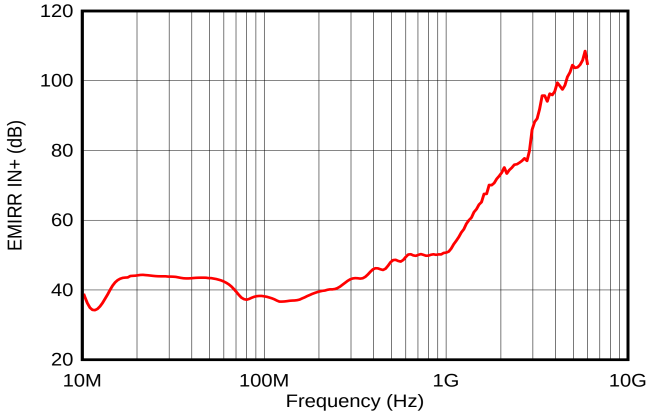


Figure 58. OPA169x EMIRR IN+

Table 1 lists the EMIRR IN+ values for the OPA169x at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPA169x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	45.9 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	50.2 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	70.7 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	76.1 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	94.1 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	104.5 dB

8.1.5 EMIRR +IN Test Configuration

Figure 59 shows the circuit configuration for testing the EMIRR IN+. An RF source connects to the op amp noninverting input pin using a transmission line. The op amp is configured in a unity-gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the op amp input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. A multimeter samples and measures the resulting DC offset voltage. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy.

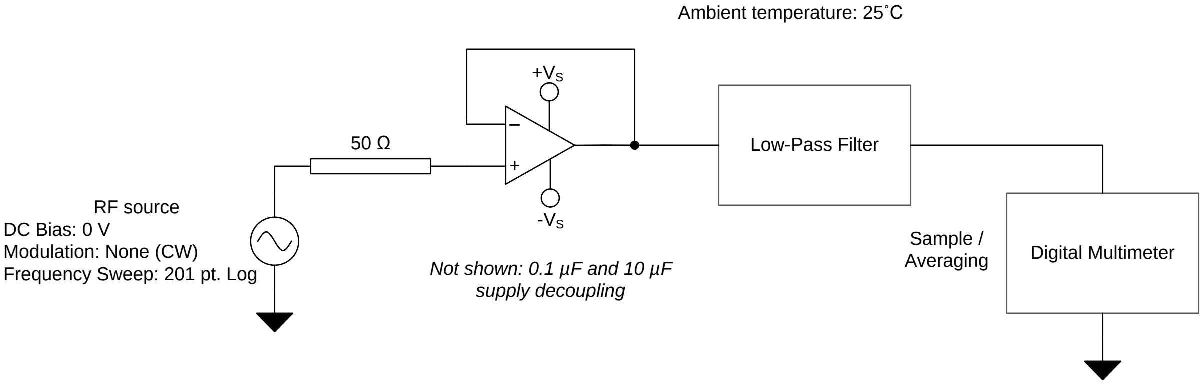


Figure 59. EMIRR +IN Test Configuration

8.2 Typical Application

The low power consumption, noise, and distortion of the OPA169x family of audio operational amplifiers make the family a viable option for a number of analog audio circuits. Figure 60 shows one circuit example, which shows a preamplifier circuit that is designed for high-performance electret microphones that use a 3-wire interface.

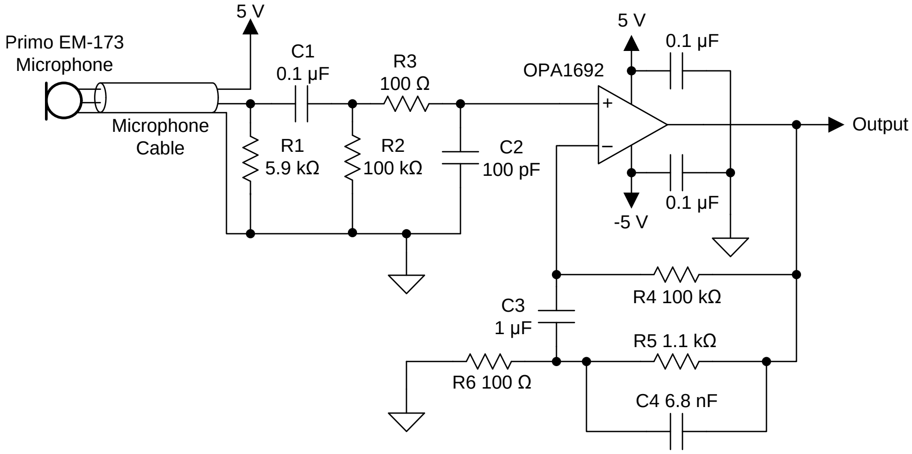


Figure 60. Low-Noise Preamplifier for 3-Wire Electret Microphones

8.2.1 Design Requirements

- Maximum Input Sound Pressure Level (SPL): 120 dB
- –3-dB Bandwidth: 20 Hz to 20 kHz
- Signal-to-Noise Ratio: > 75 dB
- Power Supply Voltage: ± 5 V
- Power Supply Current: < 1.5 mA

8.2.2 Detailed Design Procedure

The selected design requirements represent a high-performance wireless microphone application. Wireless microphones typically use an electret microphone element, an analog pre-amplifier circuit, and transmit circuitry which may use analog or digital methods of transmission. Because these devices are battery-powered, all circuitry must be designed to consume as little power as possible, while still achieving very high audio performance. The performance specifications for the microphone used in this design are shown in Table 2. This microphone element uses a 3-wire connection scheme with separate connections for power, ground, and signal. The microphone data sheet specifies that the signal line is terminated with a recommended 5.6-kΩ resistance and a 5-V supply.

Table 2. Primo EM-173 Microphone Specifications

PARAMETER	VALUE
Sensitivity	–37 dBV
Output impedance	600 Ω
Signal-to-noise ratio (SNR)	80 dB
Maximum input sound pressure level	135 dB
Operating voltage	5 V (3 V – 10 V)
Operating current	600 µA

R1, C1, and R2 provide the correct termination impedance for the microphone and AC-couple the microphone signal to the amplifier input. R2 is selected with a large value (100 kΩ) so that a smaller AC-coupling capacitor can be used (C1). The high-pass corner frequency produced by C1 and R2 must be set to 20 Hz using Equation 1:

$$20\ \text{Hz} = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1} = \frac{1}{2 \cdot \pi \cdot 100\ \text{k}\Omega \cdot C_1} \rightarrow C_1 = 79.6\ \text{nF} \rightarrow 100\ \text{nF} \quad (1)$$

R1 and R2 are in parallel for frequencies above 20 Hz. Therefore, select the value of R1 so that when in parallel with R2, the combination results in a 5.6-kΩ resistance as specified in the microphone data sheet. Equation 2 calculates R1.

$$5.6\ \text{k}\Omega = \frac{R_1 \cdot R_2}{R_1 + R_2} = \frac{R_1 \cdot 100\ \text{k}\Omega}{R_1 + 100\ \text{k}\Omega} \rightarrow R_1 = 5.9\ \text{k}\Omega \quad (2)$$

R3 and C2 form a low-pass filter to prevent the amplification of electromagnetic interference (EMI) signals. Equation 3 shows the corner frequency of this EMI filter.

$$f_{-3\text{dB}} = \frac{1}{2 \cdot \pi \cdot R_3 \cdot C_2} = \frac{1}{2 \cdot \pi \cdot 100\ \Omega \cdot 100\ \text{pF}} = 15.9\ \text{MHz} \quad (3)$$

The input bias current of the OPA1692 through the 100-kΩ input resistor (R2) and can potentially cause a large offset voltage to appear at the output of the amplifier. One solution to this problem is to match the DC resistance of the circuit at each input of the amplifier. R4 and C3 accomplish this goal by providing a DC-feedback path for the amplifier (R4) which has the same resistance as the input resistor (R2). Capacitor C3 serves two functions. First, at low-frequencies this capacitor is effectively an open circuit and therefore the gain of the amplifier is 1, which reduces DC offsets at the output. At high frequencies where the impedance of the capacitor is low, the feedback network of R5, R6, and C4 determine the gain of the amplifier.

The nominal gain of the preamplifier circuit is calculated by considering the output of the microphone at the maximum input SPL. For this design, a maximum input SPL of 120 dB or [20 pascals (Pa)] is specified. The microphone sensitivity is shown as –37 dBV, measured at 1-Pa air pressure. The output signal of the microphone at 20-Pa air pressure can be calculated by converting the –37 dBV sensitivity specification to mV per pascal of air pressure as shown in Equation 4:

$$V_{\text{OUT(MIC)}} = 20\ \text{Pa} \times 10^{\left(\frac{-37\ \text{dBV}}{20}\right)} = 282.5\ \text{mV}_{\text{RMS}} = 399.5\ \text{mVp} \quad (4)$$

The linear output voltage range of the OPA1692 extends to within 200 mV of each power supply. Therefore, on a ±5-V power supply, the linear output voltage range is ±4.8 V. The linear output voltage range of the amplifier and the maximum output signal level of the microphone determine the gain of the amplifier, as shown in Equation 5:

$$G = \frac{V_{\text{OUT(OPA1692)}}}{V_{\text{OUT(MIC)}}} = \frac{4.8\ V_P}{399.5\ \text{mV}_P} = 12.015\ (21.6\ \text{dB}) = 1 + \frac{R_5}{R_6} \quad (5)$$

Selecting values of 1.1 kΩ and 100 Ω for R5 and R6, respectively, produce a nominal gain of 12 for the circuit, allowing the full linear output swing of the amplifier to be used for the maximum input SPL. The feedback capacitor (C4) limits the gain of the circuit at high frequencies beyond the range of human hearing. Equation 6 shows the high-pass corner frequency that capacitor C4 produces:

$$20\ \text{kHz} = \frac{1}{2 \cdot \pi \cdot R_5 \cdot C_4} = \frac{1}{2 \cdot \pi \cdot 1.1\ \text{k}\Omega \cdot C_4} \rightarrow C_4 = 7.23\ \text{nF} \rightarrow 6.8\ \text{nF} \quad (6)$$

Lastly, by the low-frequency bandwidth requirement for the design and the gain determines the value of C3. The high-pass corner frequency produced by this capacitor is affected by resistors R5 and R6 as shown in Equation 7:

$$C_3 = \left(1 + \frac{R_5}{R_6}\right) \frac{1}{2 \cdot \pi \cdot R_4 \cdot f_{-3\text{dB}}} = (12) \frac{1}{2 \cdot \pi \cdot 100\ \text{k}\Omega \cdot 20\ \text{Hz}} \rightarrow C_3 = 955\ \text{nF} \rightarrow 1\ \mu\text{F} \quad (7)$$

8.2.3 Application Curves

Table 3 lists the performance of the preamplifier circuit in Figure 60. The total power supply current of the circuit is a combination of the 600 µA consumed by the microphone element itself and the 650 µA power-supply current of the OPA1692. Figure 61 shows the frequency response of the circuit. Comparing the output signal level of the microphone for a 1-Pa input signal level to the A-weighted noise of the preamplifier circuit and microphone determines the SNR of the circuit. For a 1-Pa input sound level, the microphone produces a 14.13 mV_{RMS} signal. The microphone has an SNR of 80 dB, which results in a RMS noise voltage of 1.41 μV_{RMS}. The input-referred A-weighted noise voltage of the preamplifier circuit is 600.6 nV_{RMS}. The microphone and preamplifier noise must be combined as a root sum of squares, which results in a total RMS noise voltage of 1.53 μV_{RMS} and a total circuit SNR of 79.3 dB. By selecting the OPA1692 for this design, this circuit achieves a high level of performance with low power consumption.

Table 3. Comparison of Design Requirements and Results

SPECIFICATION	DESIGN REQUIREMENT	DESIGN RESULT
Gain	12 V/V or 21.6 dB (120 dB Maximum Input SPL)	11.79 V/V or 21.43 dB
–3-dB bandwidth	20 Hz to 20 kHz	24 Hz to 21 kHz
Signal-to-noise ratio	> 75 dB	79.3 dB
Power supply current (microphone and amplifier circuit)	< 1.5 mA	1.25 mA

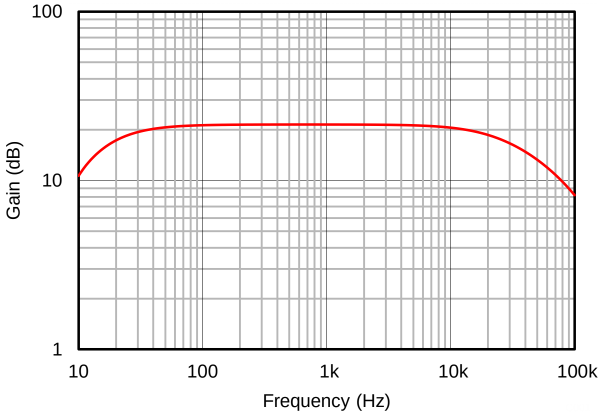


Figure 61. Frequency Response of the Low-Noise Preamplifier for 3-Wire Electret Microphones

8.3 Other Application Examples

8.3.1 Two-Wire Electret Microphone Preamplifier

The circuit in Figure 60 can be modified to accommodate two-wire electret microphones, as shown in Figure 62. In two-wire configurations, there is no resistor in series with the source of the internal JFET of the microphone. The audio signal is output as a varying voltage across the biasing resistor (2.2 kΩ in Figure 62) of the capsule. The preamplifier input is AC-coupled to the biasing resistor through a 0.1-µF capacitor and 47-kΩ input resistor.

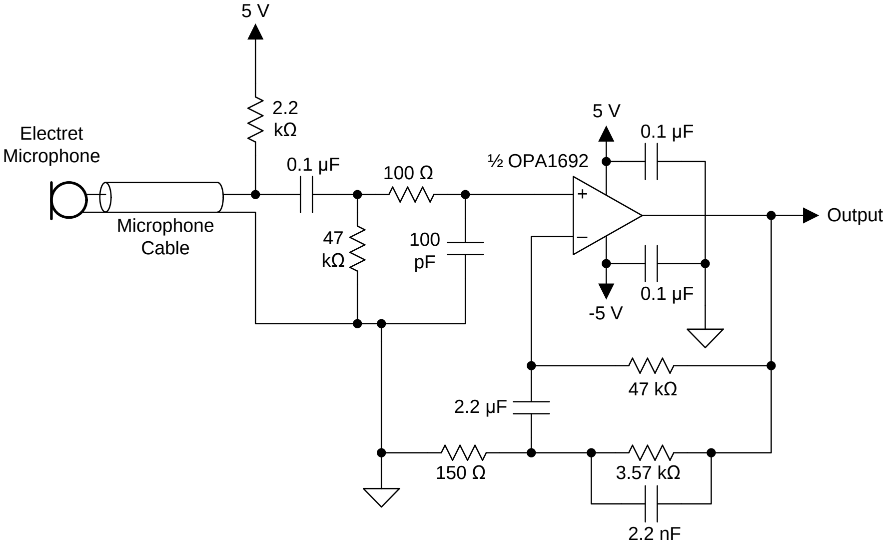
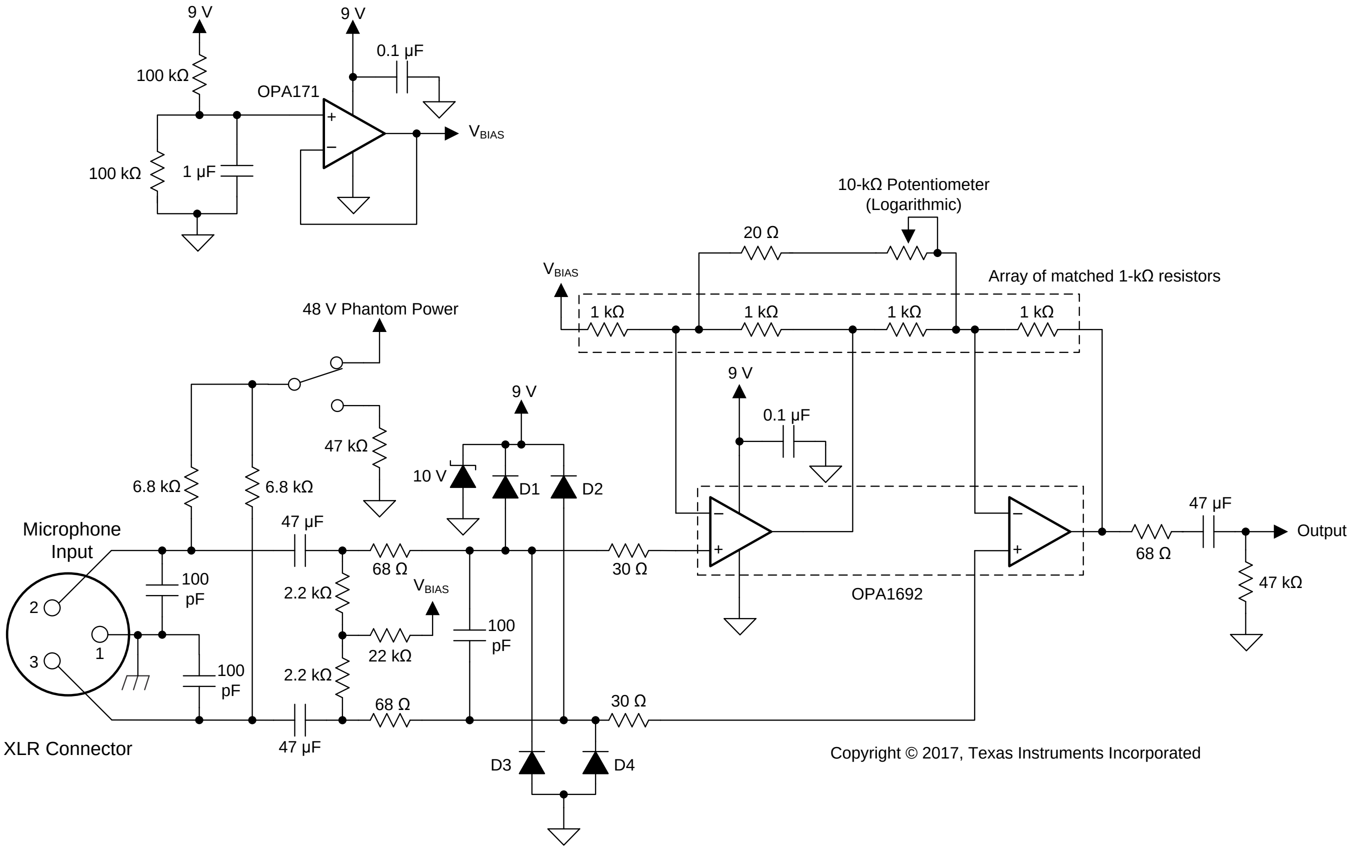


Figure 62. Two-Wire Electret Microphone Preamplifier

Other Application Examples (continued)

8.3.2 Battery-Powered Preamplifier for Professional Microphones

Figure 63 shows a preamplifier designed for portable applications that require low-noise, high common-mode rejection, and long battery life. Both channels of the OPA1692 are configured as a two-op amp instrumentation amplifier with a variable gain from 6 to 40 dB. An array of 1-kΩ resistors is recommended for the feedback network because the excellent matching of these resistors ensure high common-mode rejection in the circuit. An OPA171 is configured as a buffered power supply divider to provide a biasing voltage to the circuit, allowing the system to operate properly on a single 9-V battery. The additional components at the OPA1692 inputs are for phantom power, EMI, and ESD protection. The circuit consumes approximately 2 mA of quiescent power supply current.



Copyright © 2017, Texas Instruments Incorporated

Figure 63. Preamplifier for Professional Microphones Powered from a 9-V Battery

9 Power Supply Recommendations

The OPA169x are specified for operation from 3.5 V to 36 V (±1.75 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

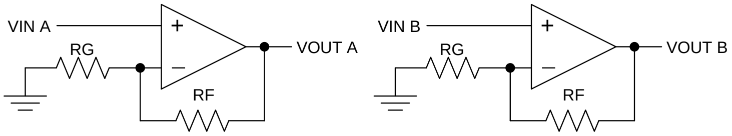
10 Layout

10.1 Layout Guidelines

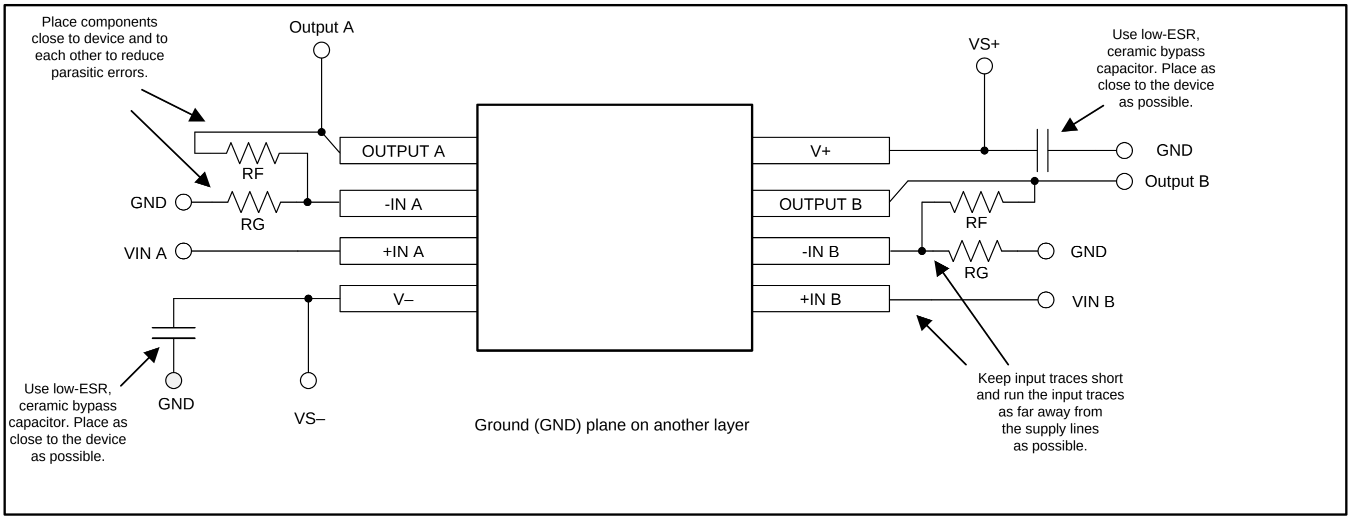
For best operational performance of the device, use good printed-circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Physically separate digital and analog grounds, observing the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close as possible to the device. As shown in Figure 64, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- For best performance, TI recommends cleaning the PCB following assembly.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, TI recommends baking the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



(Schematic Representation)



Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Ground (GND) plane on another layer

Keep input traces short and run the input traces as far away from the supply lines as possible.

Figure 64. Operational Amplifier Board Layout for Noninverting Configuration

10.3 Power Dissipation

The OPA169x series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA169x series op amps improves heat dissipation compared to conventional materials. Circuit board layouts minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise is further minimized by soldering the devices to the circuit board rather than using a socket.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI™ is a free, fully functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 DIP Adapter EVM

The DIP Adapter EVM tool provides an easy, low-cost way to prototype small surface mount ICs. The evaluation tool these TI packages: D or U (SOIC-8), PW (TSSOP-8), DGK (VSSOP-8), DBV (SOT23-6, SOT23-5 and SOT23-3), DCK (SC70-6 and SC70-5), and DRL (SOT563-6). The DIP Adapter EVM may also be used with terminal strips or may be wired directly to existing circuits.

11.1.1.3 Universal Operational Amplifier EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, VSSOP, TSSOP and SOT-23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

11.1.1.4 Smart Amplifier Speaker Characterization Board Evaluation Module

The Smart Amplifier Speaker Characterization Board, when used in conjunction with a supported TI Smart Amplifier and PurePath Console software, provides users the ability to measure speaker excursion, temperature and other parameters for use with a TI Smart Amplifier products.

11.1.1.5 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

11.1.1.6 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents are relevant to using the OPA169x and are recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *Source resistance and noise considerations in amplifiers*
- *Single-Supply Operation of Operational Amplifiers*
- *Op Amp Performance Analysis*
- *Tuning in Amplifiers*
- *Feedback Plots Define Op Amp AC Performance*
- *Active Volume Control for Professional Audio*

11.3 Related Links

Table 4 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA1692	Click here	Click here	Click here	Click here	Click here

11.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.6 Trademarks

SoundPlus, TINA-TI, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1692ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP1692	Samples
OPA1692IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1692	Samples
OPA1692IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1692	Samples
OPA1692IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP1692	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

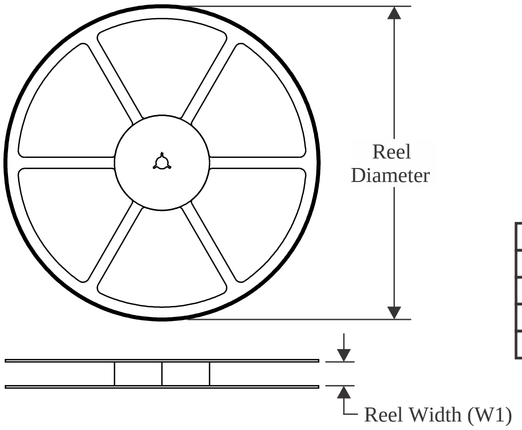
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

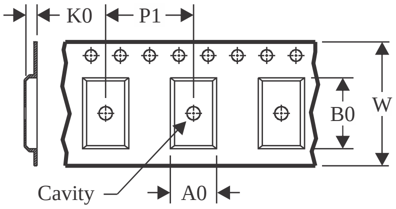
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

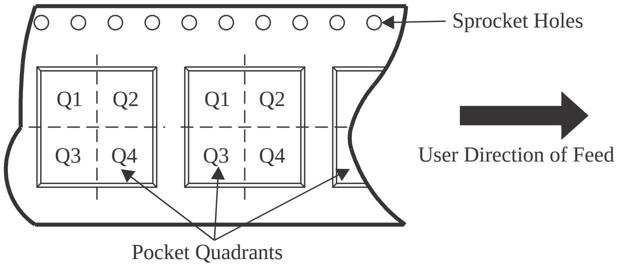


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

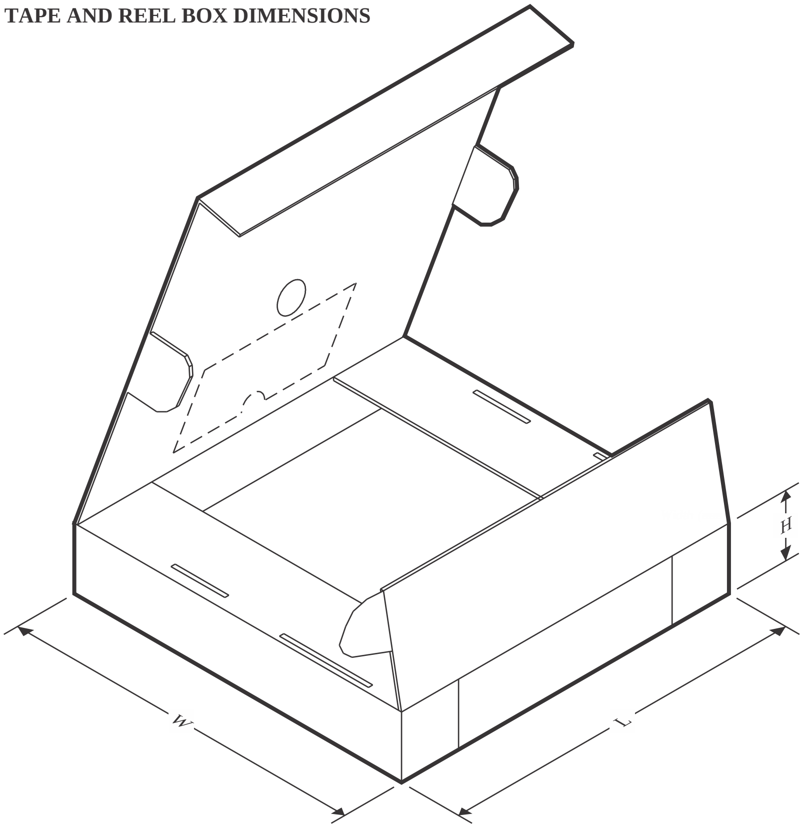
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1692IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA1692IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA1692IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

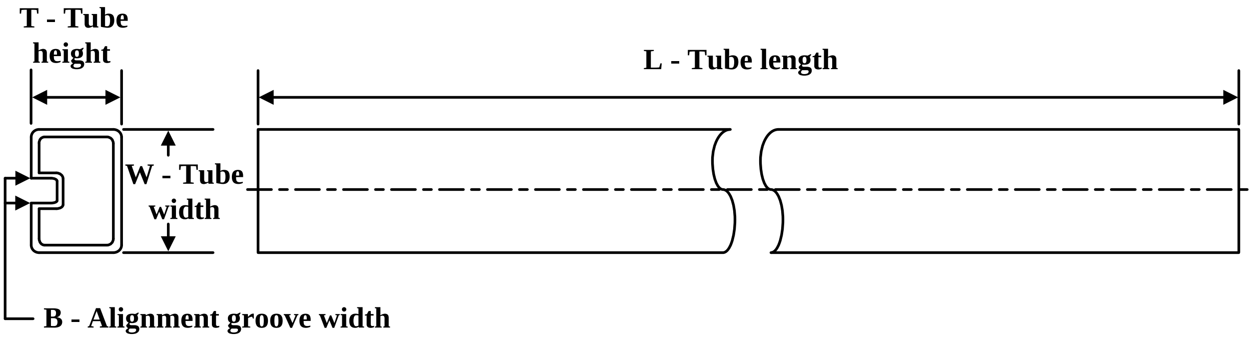
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

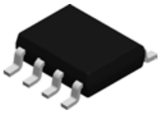
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1692IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA1692IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA1692IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

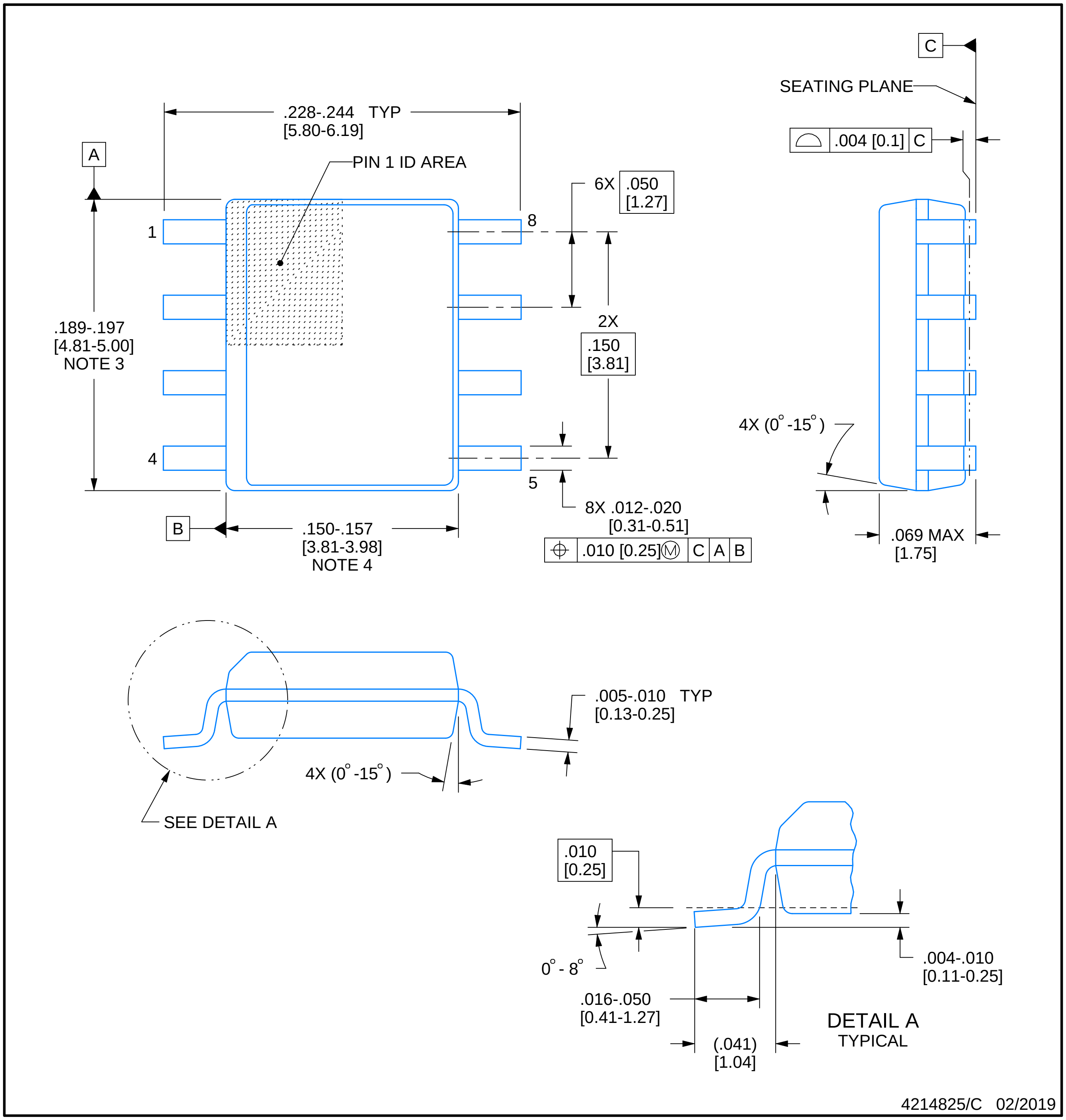
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1692ID	D	SOIC	8	75	506.6	8	3940	4.32



D0008A

SOIC - 1.75 mm max height

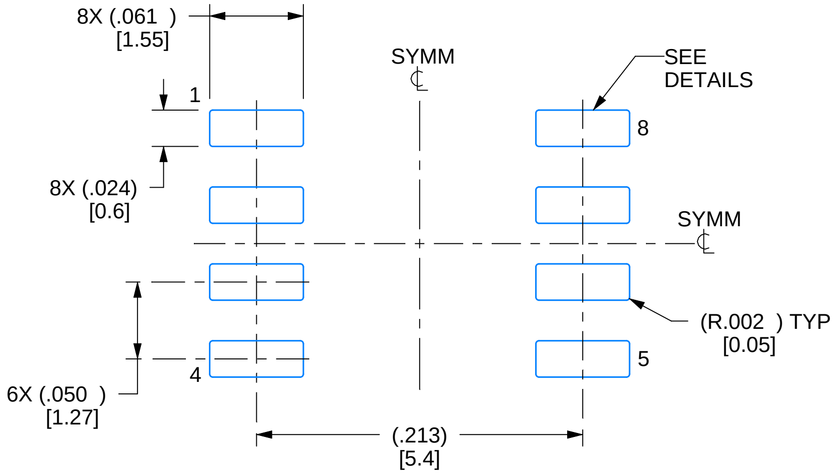
SMALL OUTLINE INTEGRATED CIRCUIT



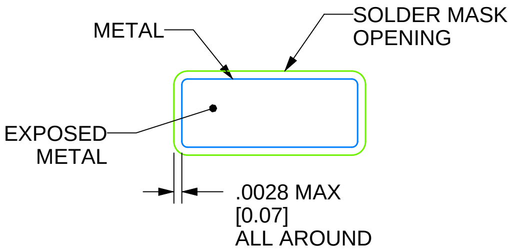
4214825/C 02/2019

NOTES:

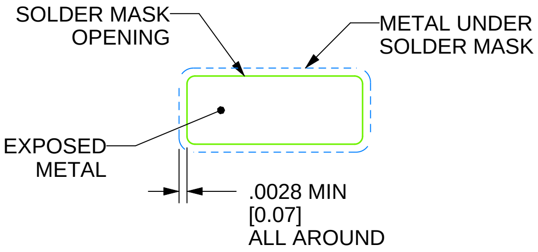
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED



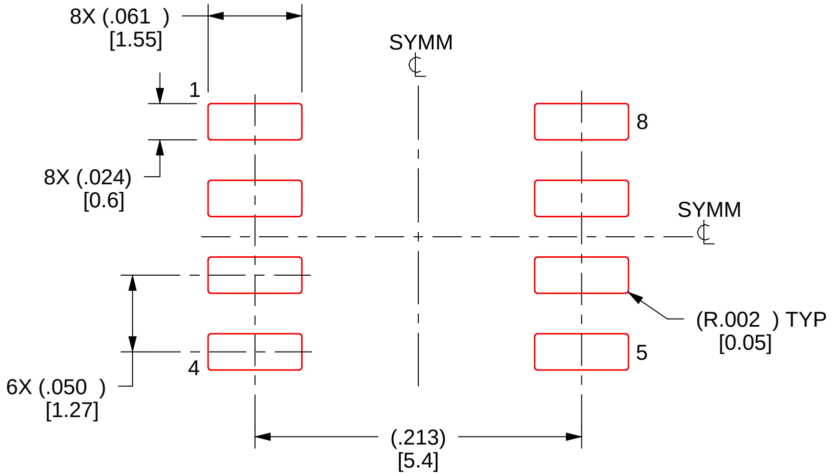
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

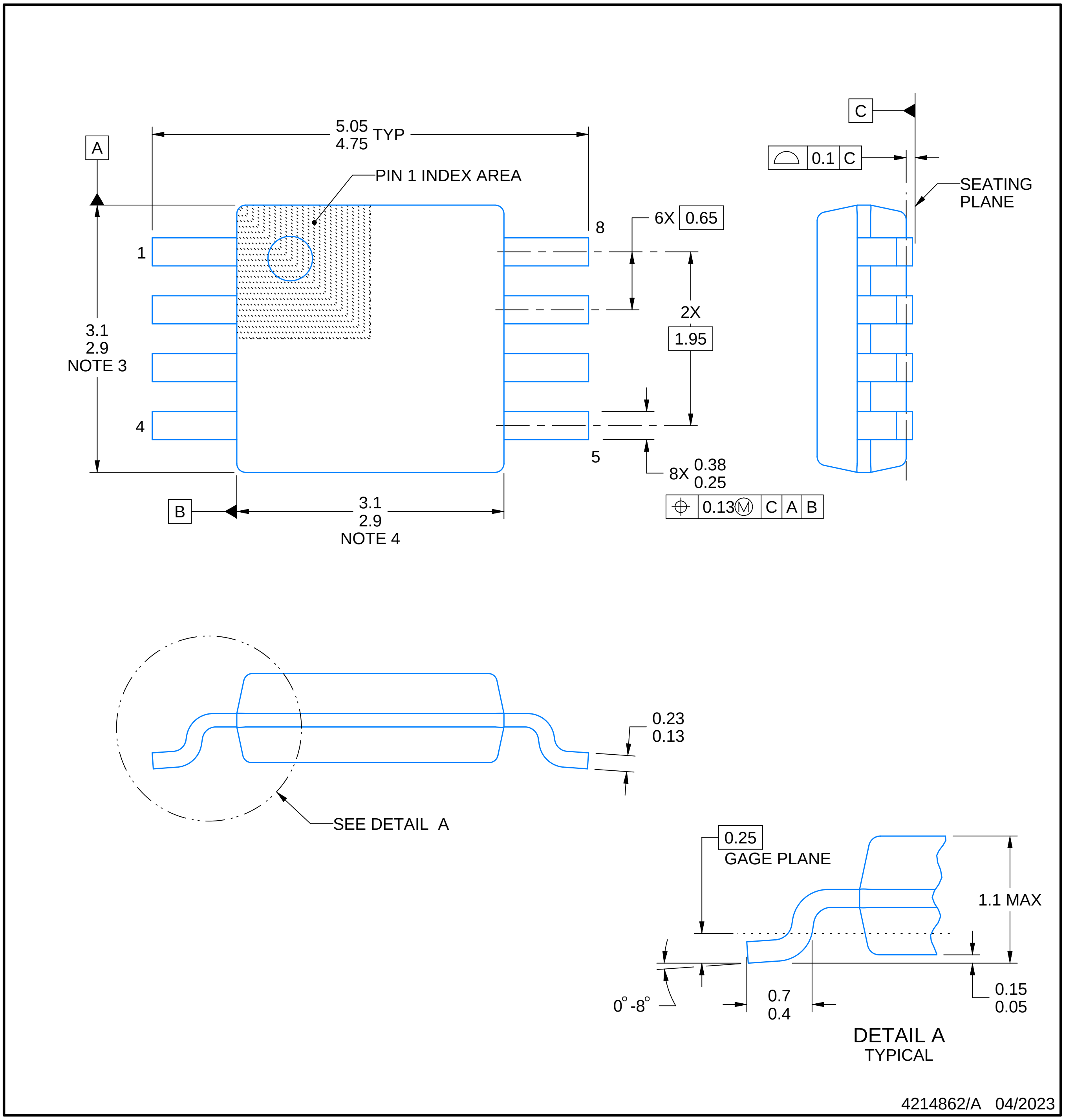


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

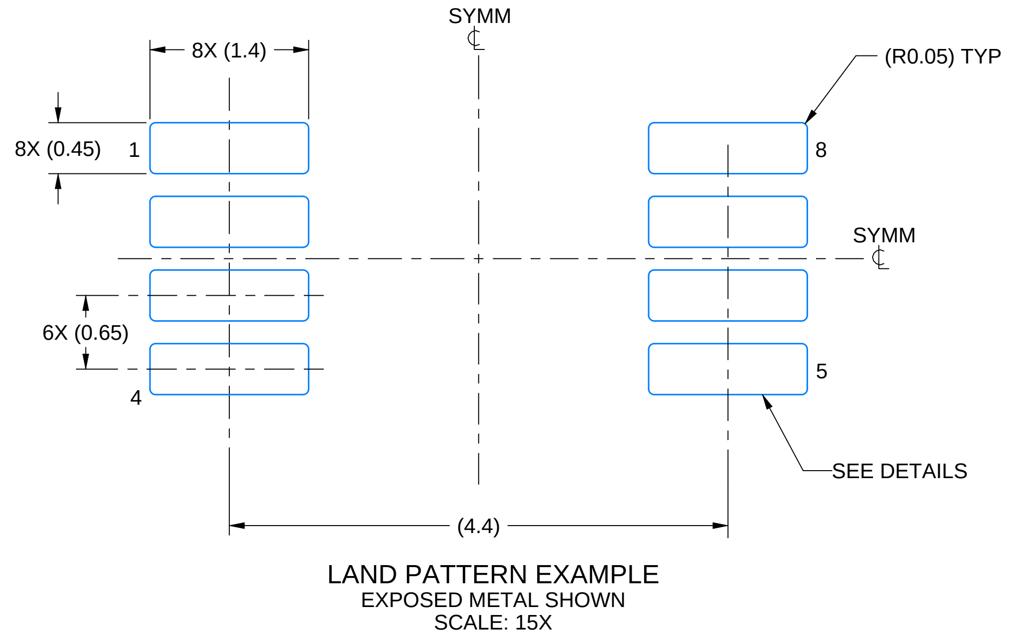


4214862/A 04/2023

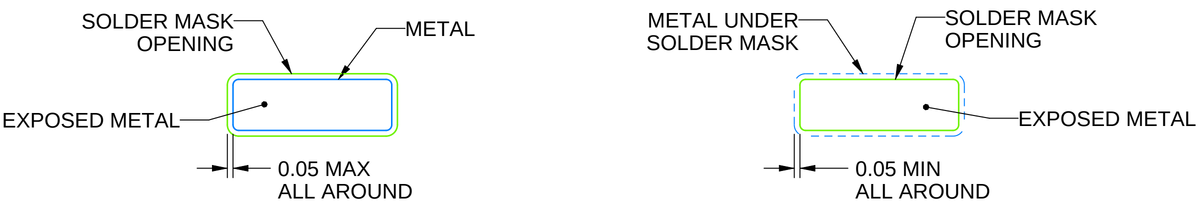
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

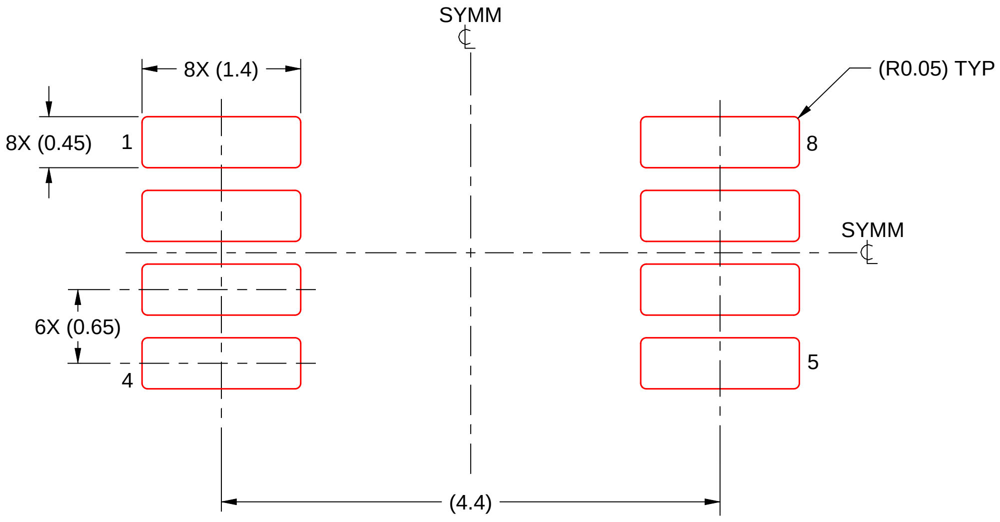
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated