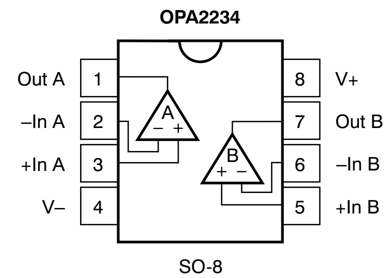
LOW-POWER, PRECISION SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

Check for Samples: OPA2234M

FEATURES

- Wide Supply Range:
  - Single Supply: V_S = 2.7 V to 36 V
  - Dual Supply: V_S = ±1.35 V to ±18 V
- Specified Performance:
  - 2.7 V, 5 V, and ±15 V
- Low Quiescent Current: 250 μA/amp
- Low Input Bias Current: 35 nA Max
- Low Offset Voltage: 100 μV Typ
- High CMRR, PSRR, and A_{OL}
- Dual Versions



DESCRIPTION

The OPA2234 series low-cost op amps are ideal for single-supply, low-voltage, low-power applications. The series provides lower quiescent current than older "1013"-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power-supply rejection, and a wide supply range provides excellent accuracy and versatility. Dual versions have identical specifications for maximum design flexibility. These general-purpose op amps are ideal for portable and battery-powered applications.

The OPA2234 series op amps operate from either single or dual supplies. In single-supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA2234 series ideal for demanding applications, including high load capacitance. Dual design features completely independent circuitry for lowest crosstalk and freedom from interaction.

Single and dual packages are in an SO-8 surface-mount and are specified for –55°C to 125°C operation.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE MARKING
OPA2234MDR	SO-8 Surface-Mount	2234M

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply Voltage, V+ to V–			
Input Voltage		(V–) – 0.7 to (V+) + 0.7	V
Output Short-Circuit(1)		Continuous	
Operating Temperature		–55 to 125	°C
Storage Temperature		–55 to 125	°C
Junction Temperature	T_{JA}	150	°C/W
	T_{JC}	39	
Lead Temperature (soldering, 10 s)		300	°C

(1) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = 5 V

At T_A = –55°C to 125°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	T_A = 25°C, V_{CM} = 2.5 V		±40	±100	µV
		V_{CM} = 2.5 V			±600	µV
vs Temperature (1)	dV_{OS}/dT	Operating Temperature Range		±3		µV/°C
vs Power Supply	PSRR	V_S = 2.7 V to 30 V, V_{CM} = 1.7 V		3	20	µV/V
vs Time				0.2		µV/mo
Channel Separation (Dual)				0.3		µV/V
INPUT BIAS CURRENT						
Input Bias Current (2)	I_B	V_{CM} = 2.5 V		–15	–35	nA
Input Offset Current	I_{OS}	V_{CM} = 2.5 V		±1	±12	nA
NOISE		f = 1 kHz				
Input Voltage Noise Density	V_n			25		nV/√Hz
Current Noise Density	I_n			80		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range			0.5		(V+) – 1	V
Common-Mode Rejection	CMRR	V_{CM} = 0.5 V to 4 V	86	106		dB
INPUT IMPEDANCE						
Differential				10^7 || 5		Ω || pF
Common-Mode		V_{CM} = 2.5 V		10^{10} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 10 kΩ, V_O = 0.25 V to 4 V	78	120		dB
		R_L = 2 kΩ, V_O = 0.5 V to 4 V	75	96		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	C_L = 100 pF		0.35		MHz
Slew Rate	SR			0.2		V/µs
Settling Time:						
0.1%		G = 1, 3 V Step, C_L = 100 pF		15		µs
0.01%		G = 1, 3 V Step, C_L = 100 pF		25		µs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		16		µs
OUTPUT						
Voltage Output:						
Positive		R_L = 10 kΩ to V_S/2	(V+) – 1	(V+) – 0.65		V
Negative		R_L = 10 kΩ to V_S/2	0.25	0.05		V
Positive		R_L = 10 kΩ to Ground	(V+) – 1	(V+) – 0.65		V
Negative		R_L = 10 kΩ to Ground	0.1	0.05		V
Short-Circuit Current	I_{SC}			±11		mA
Capacitive Load Drive (Stable Operation) (3)		G = 1		1000		pF
POWER SUPPLY						
Specified Operating Voltage				5		V
Operating Voltage Range			2.7		36	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		250	550	µA

(1) Wafer-level tested to 95% confidence level.
(2) Positive conventional current flows into the input terminals.
(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: V_S = 5 V (continued)

At T_A = –55°C to 125°C, V_S = 5 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
Specified Range			–55		125	°C
Operating Range			–55		125	°C
Storage			–55		125	°C
Thermal Resistance	θ_{JA}			150		°C/W

ELECTRICAL CHARACTERISTICS: V_S = 2.7 V

At T_A = –55°C to 125°C, V_S = 2.7 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	T_A = 25°C, V_{CM} = 1.35 V		±40	±100	µV
		V_{CM} = 1.35 V			±600	µV
vs Temperature[1]	dV_{OS}/dT	Operating Temperature Range		±3		µV/°C
vs Power Supply	PSRR	V_S = 2.7 V to 30 V, V_{CM} = 1.7 V		3	20	µV/V
vs Time				0.2		µV/mo
Channel Separation (Dual)				0.3		µV/V
INPUT BIAS CURRENT						
Input Bias Current[2]	I_B	V_{CM} = 1.35 V		–15	–35	nA
Input Offset Current	I_{OS}	V_{CM} = 1.35 V		±1	±12	nA
NOISE		f = 1 kHz				
Input Voltage Noise Density	V_n			25		nV/√Hz
Current Noise Density	I_n			80		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range			0.5		(V+) – 1.1	V
Common-Mode Rejection	CMRR	V_{CM} = 0.5 V to 1.6 V	86	106		dB
INPUT IMPEDANCE						
Differential				10^7 || 5		Ω || pF
Common-Mode		V_{CM} = 1.35 V		10^{10} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	R_L = 10 kΩ, V_O = 0.25 V to 1.7 V	78	125		dB
		R_L = 2 kΩ, V_O = 0.5 V to 1.7 V	69	96		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	C_L = 100 pF		0.35		MHz
Slew Rate	SR			0.2		V/µs
Settling Time:						
0.1%		G = 1, 1 V Step, C_L = 100 pF		6		µs
0.01%		G = 1, 1 V Step, C_L = 100 pF		16		µs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		8		µs
OUTPUT						
Voltage Output:						
Positive		R_L = 10 kΩ to V_S/2	(V+) – 1	(V+) – 0.6		V
Negative		R_L = 10 kΩ to V_S/2	0.25	0.05		V
Positive		R_L = 10 kΩ to Ground	(V+) – 1	(V+) – 0.65		V
Negative		R_L = 10 kΩ to Ground	0.1	0.05		V
Short-Circuit Current	I_{SC}			±8		mA
Capacitive Load Drive (Stable Operation)[3]		G = 1		1000		pF
POWER SUPPLY						
Specified Operating Voltage				2.7		V
Operating Voltage Range			2.7		36	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		250	550	µA

(1) Wafer-level tested to 95% confidence level.
(2) Positive conventional current flows into the input terminals.
(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: V_S = 2.7 V (continued)

At T_A = –55°C to 125°C, V_S = 2.7 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
Specified Range			–55		125	°C
Operating Range			–55		125	°C
Storage			–55		125	°C
Thermal Resistance	θ_{JA}			150		°C/W

ELECTRICAL CHARACTERISTICS: V_S = ±15 V

At T_A = –55°C to 125°C, V_S = ±15 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	T_A = 25°C, V_{CM} = 0 V		±70	±250	µV
		V_{CM} = 0 V			±750	µV
vs Temperature (1)	dV_{OS}/dT	Operating Temperature Range		±3		µV/°C
vs Power Supply	PSRR	V_S = ±1.35 V to ±18 V, V_{CM} = 0 V		3	20	µV/V
vs Time				0.2		µV/mo
Channel Separation (Dual)				0.3		µV/V
INPUT BIAS CURRENT						
Input Bias Current (2)	I_B	V_{CM} = 0 V		–12	–30	nA
Input Offset Current	I_{OS}	V_{CM} = 0 V		±1	±12	nA
NOISE		f = 1 kHz				
Input Voltage Noise Density	V_n			25		nV/√Hz
Current Noise Density	I_n			80		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range			(V–) + 1		(V+) – 1	V
Common-Mode Rejection	CMRR	V_{CM} = –14 V to 14 V	86	106		dB
INPUT IMPEDANCE						
Differential				10^7 || 5		Ω || pF
Common-Mode		V_{CM} = 0 V		10^{10} || 6		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = –13.5 V to 13 V	87	120		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	C_L = 100 pF		0.35		MHz
Slew Rate	SR			0.2		V/µs
Settling Time:						
0.1%		G = 1, 10 V Step, C_L = 100 pF		41		µs
0.01%		G = 1, 10 V Step, C_L = 100 pF		47		µs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		22		µs
OUTPUT						
Voltage Output:						
Positive			(V+) – 2	(V+) – 0.7		V
Negative			(V–) + 1.5	(V–) + 0.15		V
Short-Circuit Current	I_{SC}			±22		mA
Capacitive Load Drive (Stable Operation) (3)		G = 1		1000		pF
POWER SUPPLY						
Specified Operating Voltage				±15		V
Operating Voltage Range			±1.35		±18	V
Quiescent Current (per amplifier)	I_Q	I_O = 0		±275	±550	µA

(1) Wafer-level tested to 95% confidence level.
(2) Positive conventional current flows into the input terminals.
(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

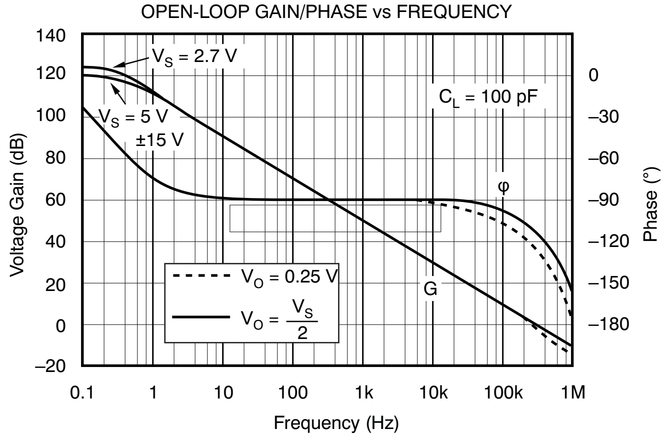
ELECTRICAL CHARACTERISTICS: V_S = ±15 V (continued)

At T_A = –55°C to 125°C, V_S = ±15 V, R_L = 10 kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

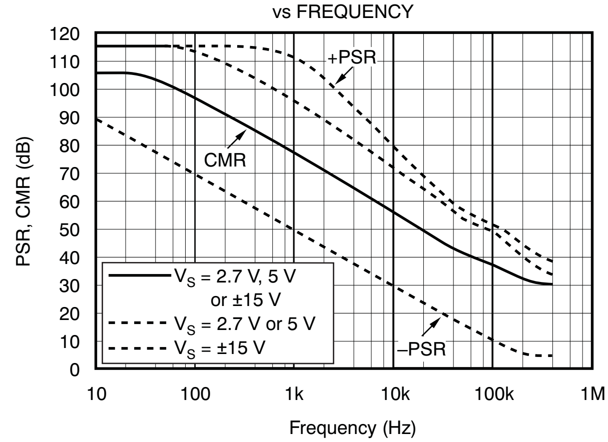
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE						
Specified Range			–55		125	°C
Operating Range			–55		125	°C
Storage			–55		125	°C
Thermal Resistance	θ_{JA}			150		°C/W

TYPICAL CHARACTERISTICS

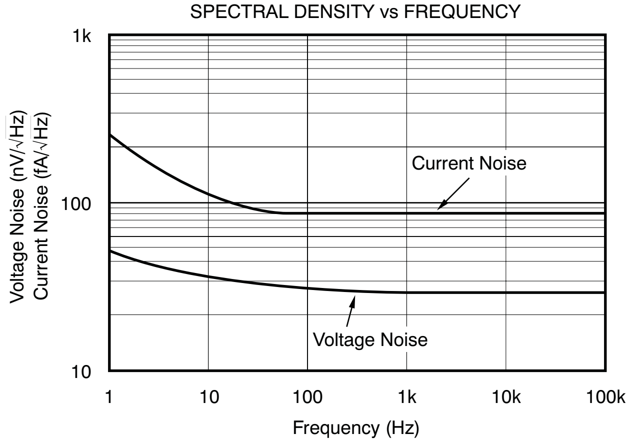
OPEN-LOOP GAIN/PHASE vs FREQUENCY



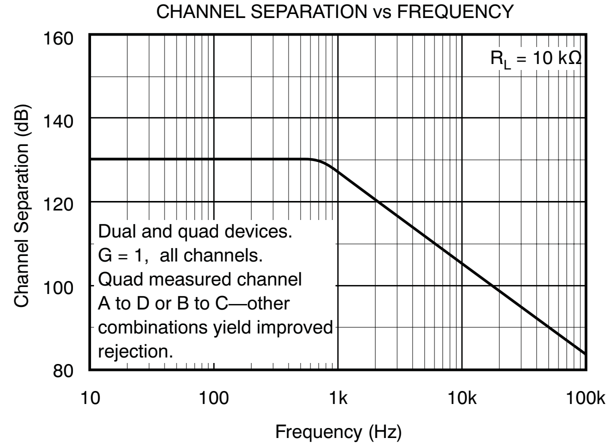
POWER-SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY



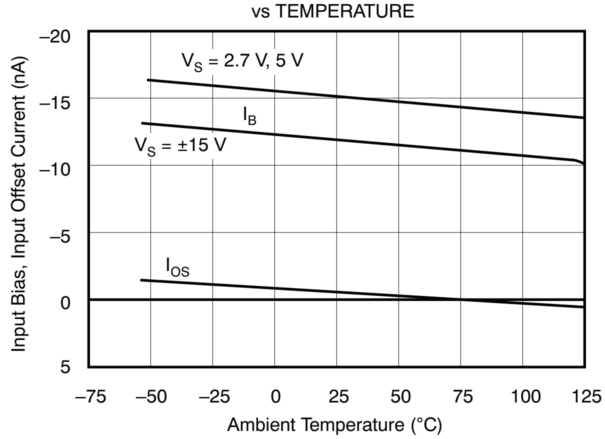
INPUT NOISE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY



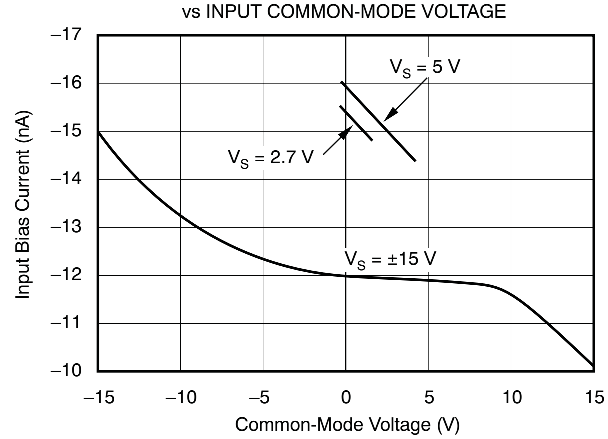
CHANNEL SEPARATION vs FREQUENCY



INPUT BIAS AND INPUT OFFSET CURRENT vs TEMPERATURE

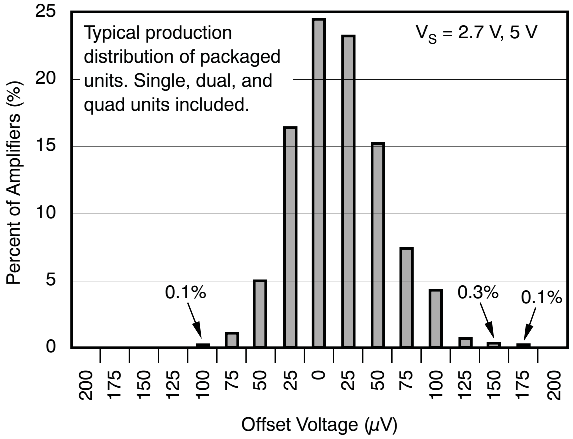


INPUT BIAS CURRENT vs INPUT COMMON-MODE VOLTAGE

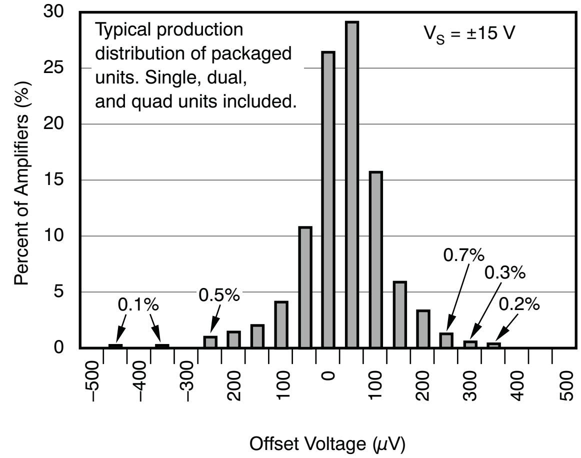


TYPICAL CHARACTERISTICS (continued)

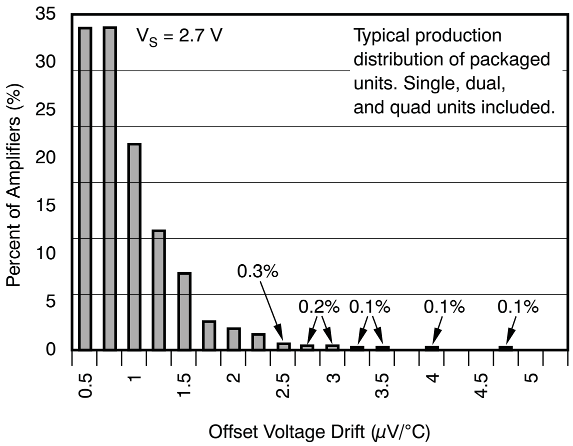
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



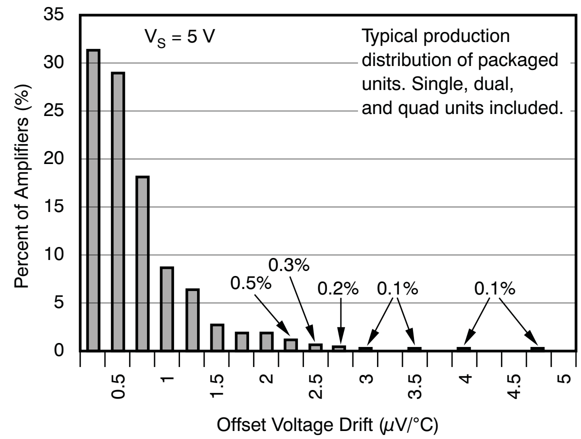
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



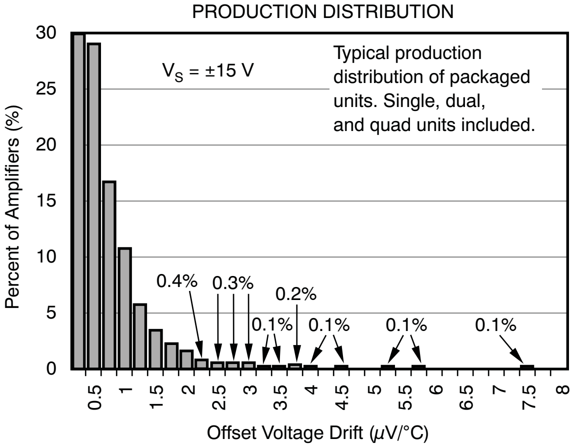
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



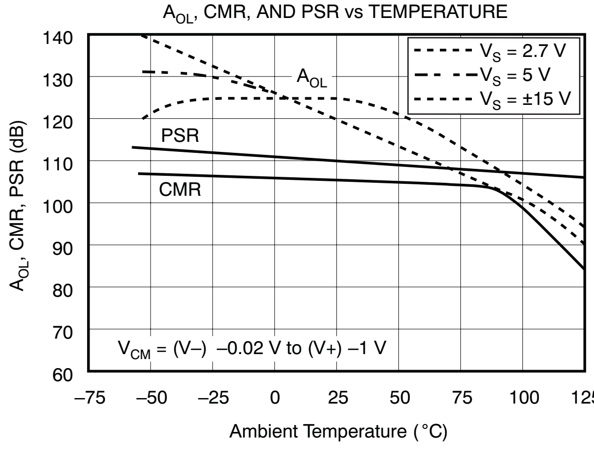
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION

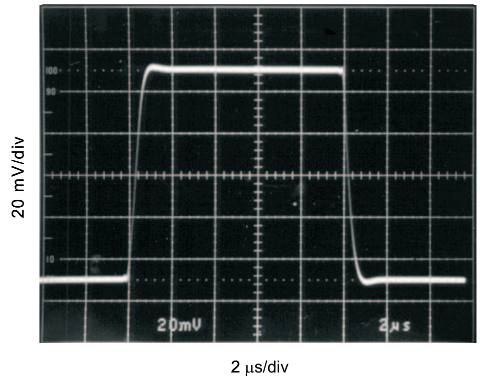


A_{OL}, CMR, AND PSR vs TEMPERATURE

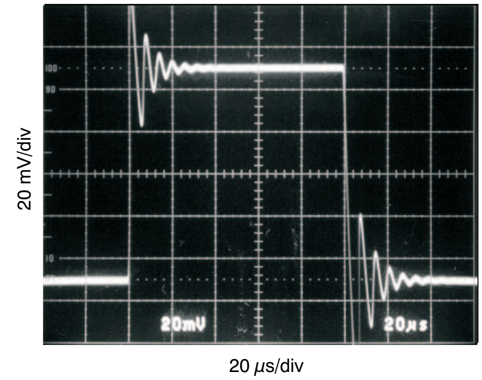


TYPICAL CHARACTERISTICS (continued)

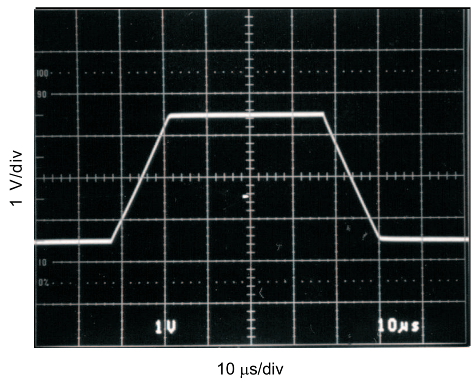
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 100 pF, V_S = 5 V



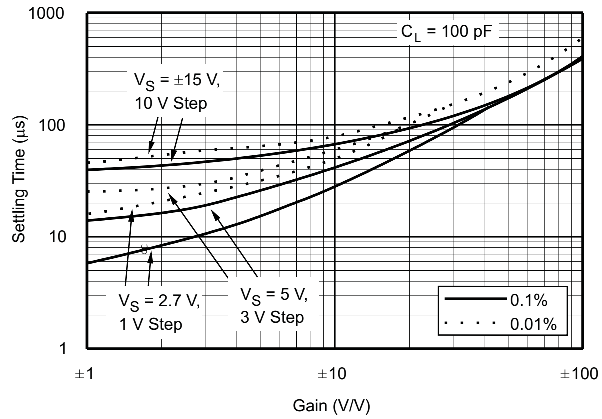
SMALL-SIGNAL STEP RESPONSE
G = 1, C_L = 10,000 pF, V_S = 5 V



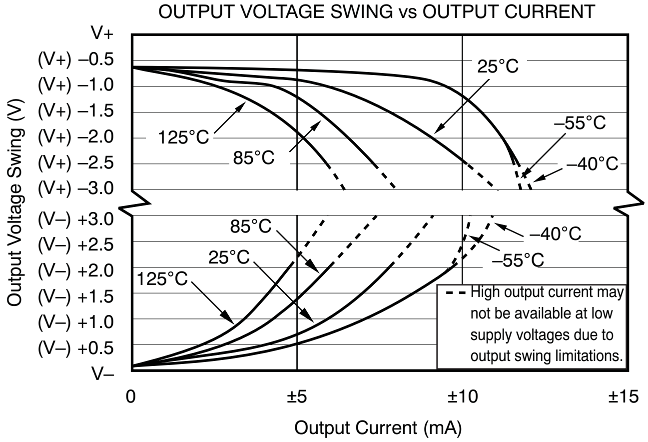
LARGE-SIGNAL STEP RESPONSE
G = 1, C_L = 100 pF, V_S = 5 V



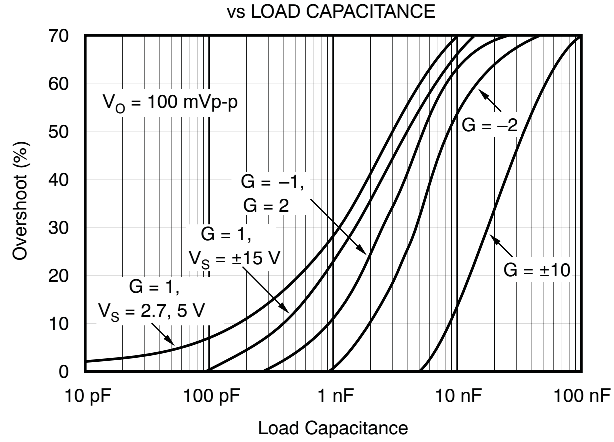
SETTLING TIME vs CLOSED-LOOP GAIN



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

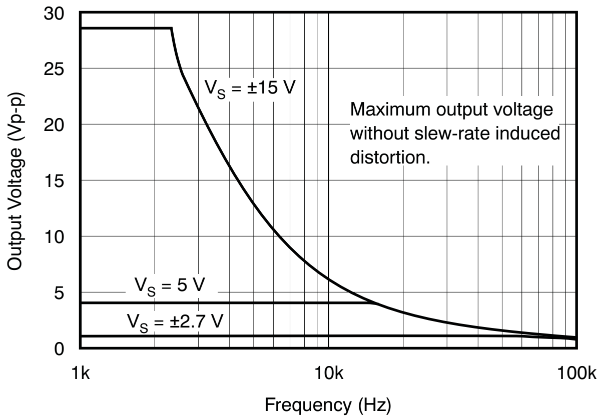


SMALL-SIGNAL OVERSHOOT
vs LOAD CAPACITANCE

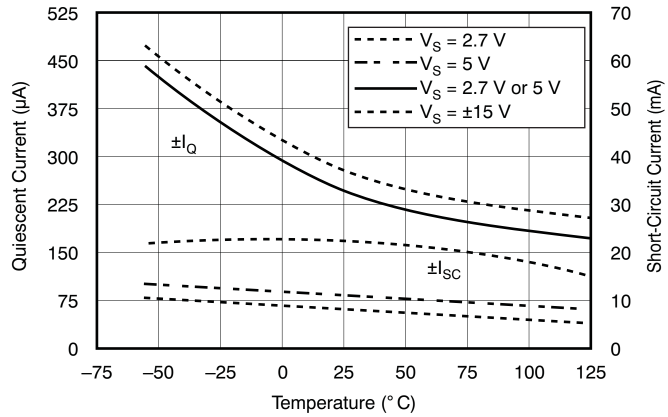


TYPICAL CHARACTERISTICS (continued)

MAXIMUM OUTPUT VOLTAGE
vs FREQUENCY



QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT
vs TEMPERATURE



APPLICATION INFORMATION

The OPA2234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10 nF ceramic capacitors.

OPERATING VOLTAGE

The OPA2234 series op amps operate from single (2.7 V to 36 V) or dual (±1.35 V to ±18 V) supplies with excellent performance. Specifications are production tested with 2.7 V, 5 V, and ±15 V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristic curves.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2234MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF OPA2234M :

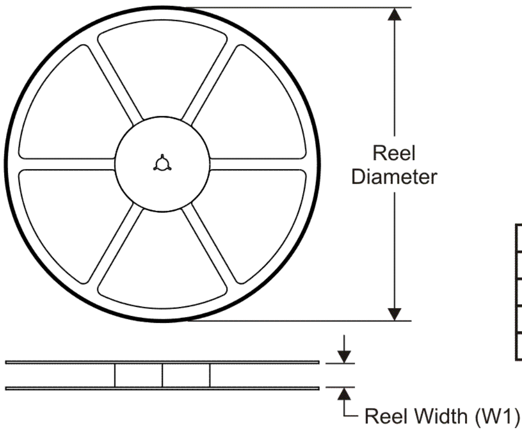
- Catalog: OPA2234

NOTE: Qualified Version Definitions:

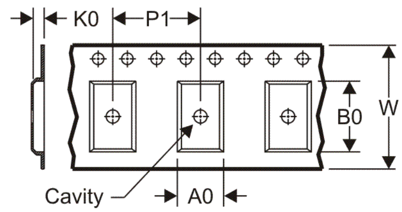
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

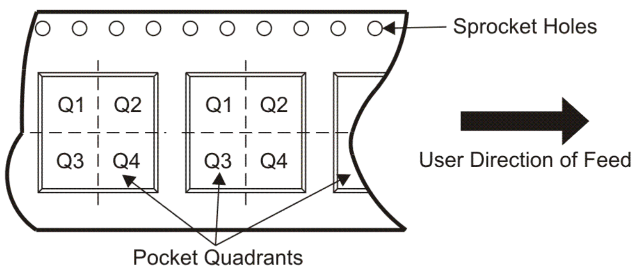


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

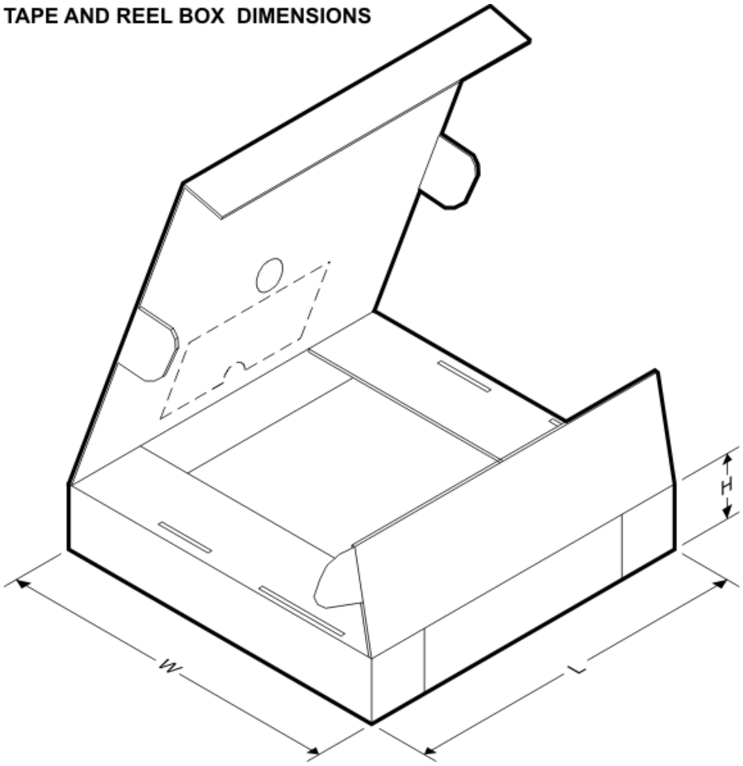
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2234MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

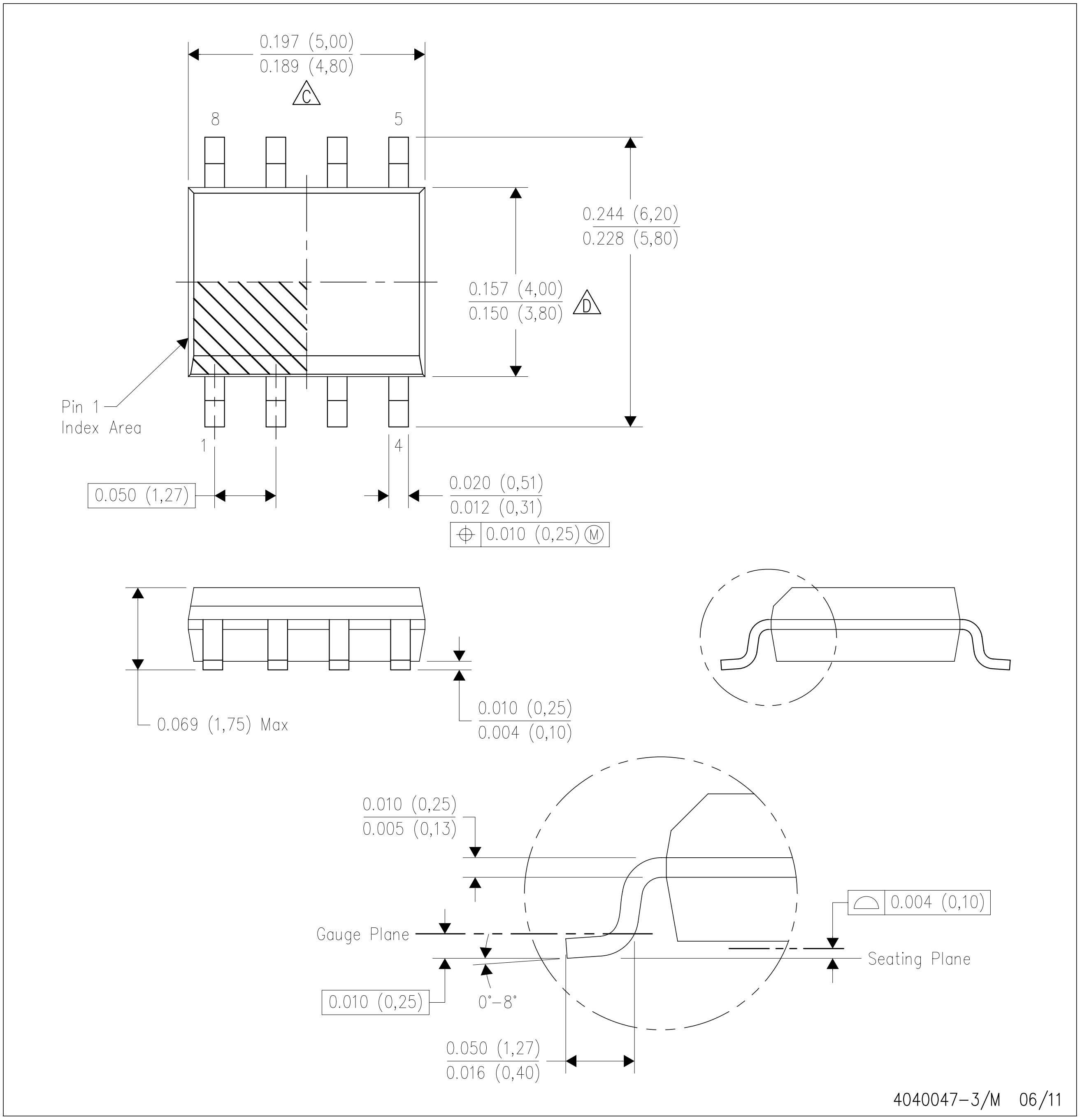
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

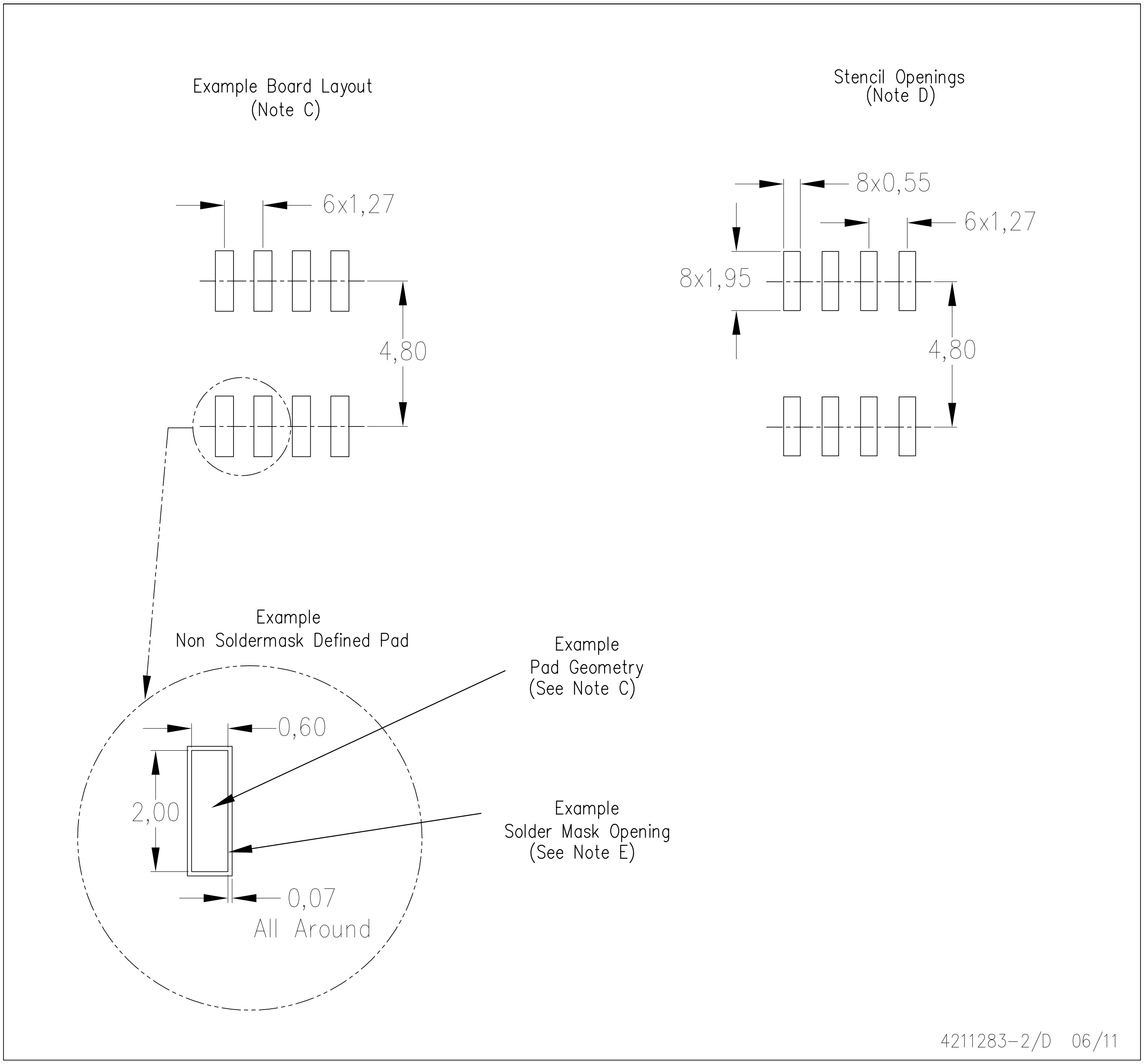
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2234MDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.