SBOS256 – AUGUST 2002

Ultra-Wideband, Current-Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- GAIN = +2 BANDWIDTH (900MHz)
- GAIN = +8 BANDWIDTH (420MHz)
- OUTPUT VOLTAGE SWING: ±3.8V
- ULTRA-HIGH SLEW RATE: 4200V/µs
- 3RD-ORDER INTERCEPT: > 40dBm (f < 50MHz)
- LOW POWER: 130mW
- LOW DISABLED POWER: 3mW

APPLICATIONS

- VERY WIDEBAND ADC DRIVER
- LOW-COST PRECISION IF AMPLIFIER
- BROADBAND VIDEO LINE DRIVER
- PORTABLE INSTRUMENTS
- ACTIVE FILTERS
- ARB WAVEFORM OUTPUT DRIVER
- OPA685 PERFORMANCE UPGRADE

DESCRIPTION

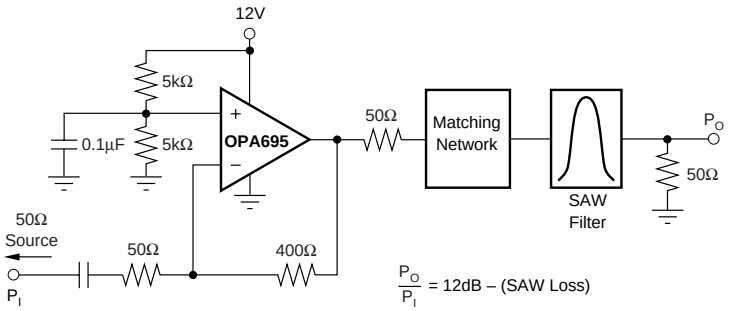
The OPA695 is a very high bandwidth, current-feedback op amp that combines exceptional 4200V/µs slew rate and low input voltage noise to deliver a precision low cost, high dynamic range Intermediate Frequency (IF) amplifier. Optimized for high gain operation, the OPA695 is ideally suited to buffering Surface Acoustic Wave (SAW) filters in an IF strip or delivering high output power at low distortion for cable modem upstream line drivers. Even higher bandwidth at lower gains gives a 900MHz video line driver for high resolution workstation graphics.

The OPA695's low 13mA supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives low system power over temperature. System power may be further reduced using the optional disable control pin. Leaving this pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA695 supply current drops to less than 150µA. This power-savings feature, along with exceptional single +5V operation, and ultra-small SOT23-6 packaging, make the OPA695 ideal for portable communications requirements.

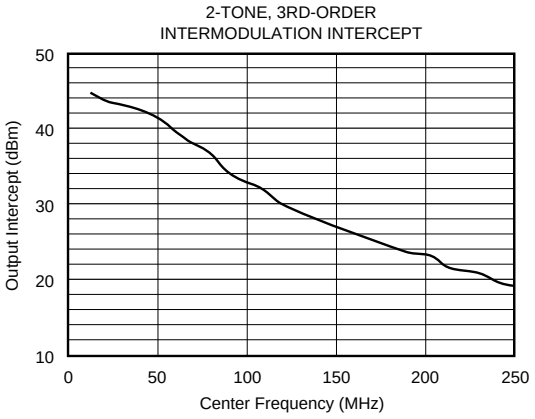
PRODUCT PREVIEW

OPA695 RELATED PRODUCTS

SINGLES	DUALS
OPA658	OPA2658
OPA691	OPA2691
OPA692	—



Low Distortion, 12dB Gain SAW Driver



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: U, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

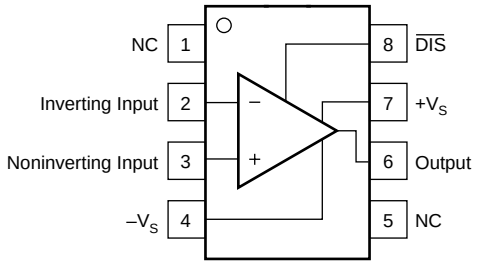
PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA695	SO-8	D	–40°C to +85°C	OPA695ID	OPA695ID	Rails, 100
"	"	"	"	"	OPA695IDR	Tape and Reel, 2500
OPA695	SOT23-6	DBV	–40°C to +85°C		OPA695IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA695IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PRODUCT PREVIEW

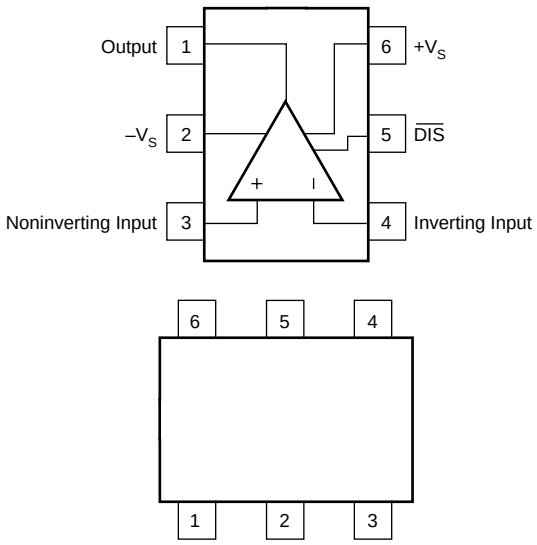
PIN CONFIGURATIONS

Top View **SO**



NC = No Connection

Top View **SOT23-6**



Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 402\Omega$, $R_L = 100\Omega$, and G = +8, (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA695ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	TEST LEVEL(3)
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, $R_F = 523\Omega$	1200				MHz	typ	C
	G = +2, $R_F = 511\Omega$	900				MHz	typ	C
	G = +8, $R_F = 402\Omega$	420				MHz	min	B
	G = +16, $R_F = 249\Omega$	340				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O = 0.5Vp-p, $R_F = 523\Omega$	350				MHz	min	B
Peaking at a Gain of +1	$R_F = 523\Omega$, V_O = 0.5Vp-p	3				dB	max	B
Large-Signal Bandwidth	G = +8, V_O = 4Vp-p	350				MHz	typ	C
Slew Rate	G = –8, V_O = 4V Step	4200				V/µs	min	B
	G = +8, V_O = 4V Step	2900				V/µs	min	B
Rise-and-Fall Time	G = +8, V_O = 0.5V Step	0.7				ns	typ	C
	G = +8, V_O = 4V Step	1.0				ns	typ	C
Settling Time to 0.02%	G = +8, V_O = 2V Step	4				ns	typ	C
0.1%	G = +8, V_O = 2V Step	3				ns	typ	C
Harmonic Distortion	G = +8, f = 10MHz, V_O = 2Vp-p							
2nd-Harmonic	$R_L = 100\Omega$	–66				dBc	max	B
	$R_L \geq 500\Omega$	–75				dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–90				dBc	max	B
	$R_L \geq 500\Omega$	–84				dBc	max	B
Input Voltage Noise	f > 1MHz	1.5				nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	11				pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	14				pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.02				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4Vp, $R_L = 150\Omega$	0.01				deg	typ	C
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 100\Omega$	42	**26**			kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	±1.2	**±2.5**	±3.2	±4	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V					µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+56	**+90**			µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V					nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	±10	**±30**			µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V					nA°/C	max	B
INPUT								
Common-Mode Input Range(5) (CMIR)		±3.4	**±3.2**			V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	54	**49**			dB	min	A
Noninverting Input Impedance		87 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	19				Ω	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.1	**±3.9**			V	min	A
	100Ω Load	±3.6	**±3.3**			V	min	A
Current Output, Sourcing	V_O = 0	+130	**+100**	+85	+80	mA	min	A
Current Output, Sinking	V_O = 0	–120	**–100**	–85	–80	mA	min	A
Closed-Loop Output Impedance	G = +8, f = 100kHz	0.2				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–150				µA	typ	C
Disable Time		100				ns	typ	C
Enable Time		100				ns	typ	C
Off Isolation	G = +8, 10MHz	70				dB	typ	C
Output Capacitance in Disable		3				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±100				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	80				µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6**	±6	±6	V	max	A
Max Quiescent Current	V_S = ±5V	13.0	**13.5**	13.5	13.5	mA	max	A
Min Quiescent Current	V_S = ±5V	13.0	**12.5**	11.9	11.2	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	55	**49**	47	46	dB	typ	A
TEMPERATURE RANGE								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for 25°C specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature specifications. (3) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ± CMIR limits.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 348Ω, R_L = 100Ω to V_S/2, and G = +8, (see Figure 3 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA695ID, IDBV						TEST LEVEL(3)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(1)	0°C to 70°C(2)	–40°C to +85°C(2)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 3)								
Small-Signal Bandwidth (V_O = 0.5Vp-p)	G = +1, R_F = 511Ω	600				MHz	typ	C
	G = +2, R_F = 487Ω	450				MHz	min	B
	G = +8, R_F = 348Ω	350				MHz	typ	C
	G = +16, R_F = 162Ω	250				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5Vp-p, R_F = 487Ω	140				MHz	min	B
Peaking at a Gain of +1	R_F = 511Ω, V_O < 0.5Vp-p	0.4				dB	max	B
Large-Signal Bandwidth	G = +8, V_O = 2Vp-p	350				MHz	typ	C
Slew Rate	G = +8, 2V Step	1900				V/µs	min	B
Rise-and-Fall Time	G = +8, V_O = 0.5V Step	0.8				ns	typ	C
	G = +8, V_O = 2V Step	1.0				ns	typ	C
Settling Time to 0.02%	G = +8, V_O = 2V Step	9				ns	typ	C
0.1%	G = +8, V_O = 2V Step	7				ns	typ	C
Harmonic Distortion	G = +8, f = 10MHz, V_O = 2Vp-p							
2nd-Harmonic	R_L = 100Ω to V_S/2	–60				dBc	max	B
	R_L ≥ 500Ω to V_S/2	–68				dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–58				dBc	max	B
	R_L ≥ 500Ω to V_S/2	–60				dBc	max	B
Input Voltage Noise	f > 1MHz	1.5				nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	11				pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	15				pA/√Hz	max	B
DC PERFORMANCE(4)								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 100Ω to V_S/2	40	**25**			kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	±1	**±3**	±3.5	±4.0	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2					µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	+40	**+110**			µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2					nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	±50	**±100**			µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2					nA/°C	max	B
INPUT								
Least Positive Input Voltage(5)		1.7	**1.8**			V	max	A
Most Positive Input Voltage(5)		3.3	**3.2**			V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = V_S/2	54	**48**			dB	min	A
Noninverting Input Impedance		87 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	23				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.1	**3.9**			V	min	A
	R_L = 100Ω to V_S/2	4.0	**3.8**			V	min	A
Least Positive Output Voltage	No Load	0.9	**1.1**			V	max	A
	R_L = 100Ω to V_S/2	1.0	**1.2**			V	max	A
Current Output, Sourcing	V_O = V_S/2	90	**62**			mA	min	A
Current Output, Sinking	V_O = V_S/2	–70	**–45**			mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.3				Ω	typ	C
DISABLE (Disabled LOW)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–150				µA	typ	C
Disable Time		150				ns	typ	C
Enable Time		150				ns	typ	C
Off Isolation	G = +8, 10MHz	70				dB	typ	C
Output Capacitance in Disable		3				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±100				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0	75				µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Max Single-Supply Operating Voltage			**12**	12	12	V	max	A
Max Quiescent Current	V_S = +5V	10.7	**11.3**	11.3	11.3	mA	max	A
Min Quiescent Current	V_S = +5V	10.7	**9.0**	8.3	8.1	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	54	**51**	49	48	dB	min	A
TEMPERATURE RANGE								
Specification: ID, IDBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT23-6		150				°C/W	typ	C

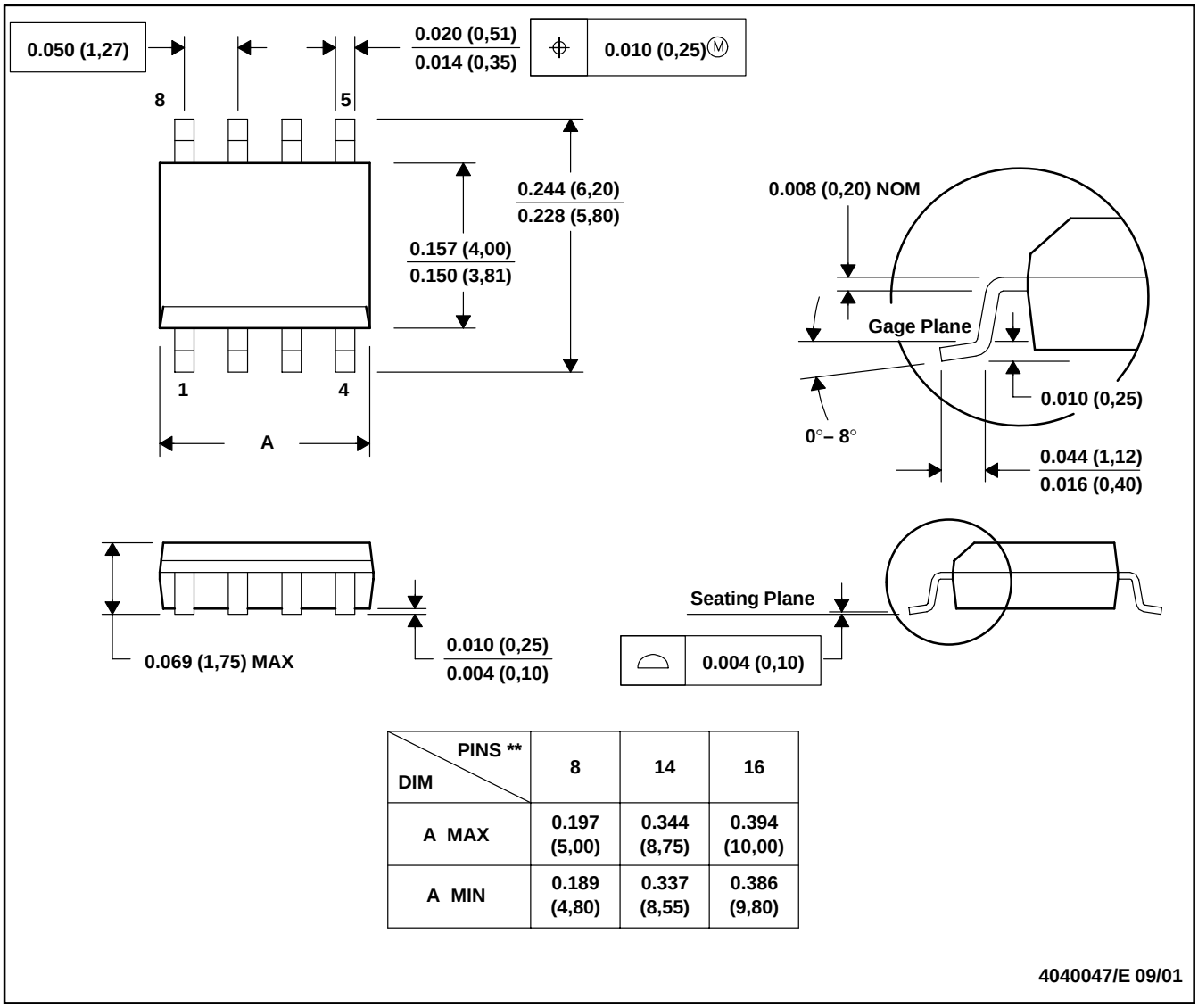
NOTES: (1) Junction temperature = ambient for 25°C specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature specifications. (3) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMRR at ±CMIR limits.

PRODUCT PREVIEW

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



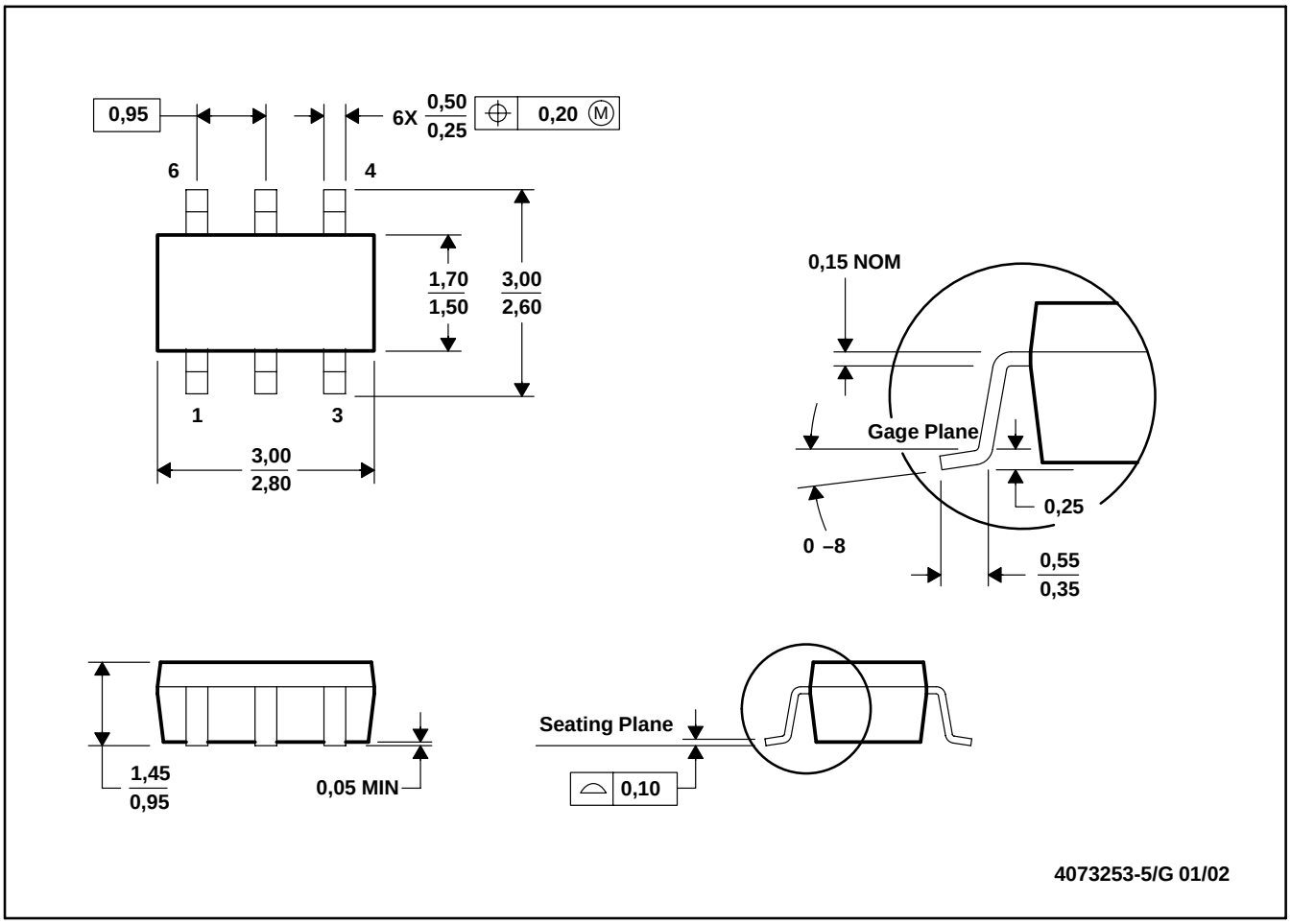
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PRODUCT PREVIEW

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 may be wider than leads 4, 5, 6 for package orientation.

PRODUCT PREVIEW

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