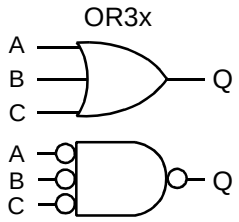
Description

OR3x is a family of 3-input gates which perform the logical OR function.

Logic Symbol



Truth Table

A	B	C	Q
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

HDL Syntax

Verilog ..... OR3x *inst_name* (Q, A, B);

VHDL..... *inst_name*: OR3x port map (Q, A, B);

Pin Loading

Pin Name	Equivalent Loads			
	OR31	OR32	OR34	OR36
A	1.0	1.0	2.1	3.1
B	1.0	1.0	2.1	3.1
C	1.0	1.0	2.1	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR31	2.0	TBD	3.6
OR32	3.0	TBD	5.0
OR34	6.0	TBD	10.4
OR36	8.0	TBD	13.4

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR31	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.23 0.37	0.33 0.51	0.44 0.67	0.59 0.85	0.71 0.98
OR32	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.25 0.45	0.37 0.63	0.45 0.75	0.54 0.87	0.65 1.02
OR34	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.40	0.31 0.57	0.42 0.69	0.52 0.81	0.63 0.93
OR36	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.21 0.42	0.31 0.57	0.41 0.69	0.50 0.81	0.59 0.93

Delay will vary with input conditions. See page 2-17 for interconnect estimates.