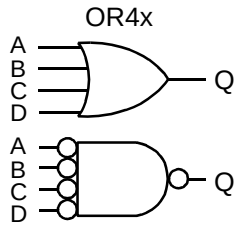
Description

OR4x is a family of 4-input gate which performs the logical OR function.

Logic Symbol



Truth Table

A	B	C	D	Q
L	L	L	L	L
H	X	X	X	H
X	H	X	X	H
X	X	H	X	H
X	X	X	H	H

HDL Syntax

Verilog ..... OR4x *inst_name* (Q, A, B, C, D);

VHDL..... *inst_name*: OR4x port map (Q, A, B, C, D);

Pin Loading

Pin Name	Equivalent Loads			
	OR41	OR42	OR44	OR46
A	1.0	1.0	3.2	3.1
B	1.0	1.0	3.2	3.1
C	1.0	1.0	3.2	3.1
D	1.0	1.0	3.2	3.1

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
OR41	3.0	TBD	4.8
OR42	4.0	TBD	7.8
OR44	8.0	TBD	12.3
OR46	9.0	TBD	16.8

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

OR41	**Number of Equivalent Loads**		**1**	**4**	**8**	**13**	**17 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.31	0.31 0.46	0.43 0.66	0.58 0.91	0.69 1.10
OR42	**Number of Equivalent Loads**		**1**	**8**	**15**	**22**	**30 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.25 0.35	0.36 0.55	0.45 0.72	0.55 0.88	0.66 1.05
OR44	**Number of Equivalent Loads**		**1**	**14**	**28**	**42**	**56 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.19 0.38	0.30 0.59	0.41 0.74	0.50 0.86	0.59 0.97
OR46	**Number of Equivalent Loads**		**1**	**21**	**42**	**62**	**83 (max)**
	From: Any Input To: Q	t_{PLH} t_{PHL}	0.22 0.50	0.33 0.69	0.44 0.83	0.55 0.94	0.67 1.05

Delay will vary with input conditions. See page 2-17 for interconnect estimates.