



## LCD MODULE SPECIFICATION



**MODEL NO.**

**OSD2002BYPNJB**

FOR MESSRS:

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ON DATE OF:

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APPROVED BY:

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## **C O N T E N T S**

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3. Absolute Maximum Rating
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## 1. Precaution in use of PLED Module

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of PLED module.
- (3) Don't disassemble the module
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist module.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please storage in anti-static electricity container and clean environment.

## 2. General Specification

### (1) Mechanical Dimension

Item	Dimension	Unit
Number of Characters	20characters x 2 Lines	—
Module dimension ( L x W x H )	116.0 x 37.0 x 9.5(Max)	mm
View area	79.0 x 17.0	mm
Active area	73.45 x 11.4	mm
Dot size	0.55 x 0.65	mm
Dot pitch	0.65 x 0.70	mm
Character size ( L x W )	3.15 x 5.55	mm
Character pitch ( L x W )	3.7 x 5.95	mm

### (2) Controller IC: **PT6880(Command software same as HD44780 or KS0066)**

### (3) Temperature Range

	Wide
Operating	-20 ~+50°C
Storage	-30 ~+70°C



### 3. Absolute Maximum Ratings

#### 3.1 Electrical Absolute Maximum Ratings

(V<sub>ss</sub>=0V, Ta=25°C)

Item	Symbol	Min	Max	Unit
Supply Voltage (Logic)	V <sub>dd</sub> -V <sub>ss</sub>	4.5	5.5	V
Input Voltage	V <sub>I</sub>	V <sub>ss</sub>	V <sub>dd</sub>	V
Wide Temperature Type	Top	-20	+50	°C
	T <sub>stg</sub>	-30	+70	°C

#### 3.2 Environmental Absolute Maximum Ratings

Item	Operating		Storage		Comment
	(Min.)	(Max.)	(Min.)	(Max.)	
Humidity	Note(2)		Note(2)		Without condensation
Vibration	--	4.9M/S <sup>2</sup>	--	19.6M/S <sup>2</sup>	XYZ Direction
Shock	--	29.4M/S <sup>2</sup>	--	490M/S <sup>2</sup>	XYZ Direction

Note (1) Ta = 0°C : 50Hr Max.

Note (2) Ta ≤ 40°C : 90% RH MAX

Ta > 40°C : Absolute humidity must be lower than the humidity of 90% at 40°C.



#### 4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	Vdd-Vss	—	4.5	—	5.5	V
Input High Volt.	V <sub>IH</sub>	—	0.8Vdd	—	Vdd	V
Input Low Volt.	V <sub>IL</sub>	—	—	—	0.6	V
Output High Volt.	V <sub>OH</sub>	—	0.8Vdd	—	—	V
Output Low Volt.	V <sub>OL</sub>	—	—	—	0.4	V
Brightness control voltage			2.5	3.0	5.0	
Supply Current	I <sub>dd</sub>	Vdd=5V	—		100	mA



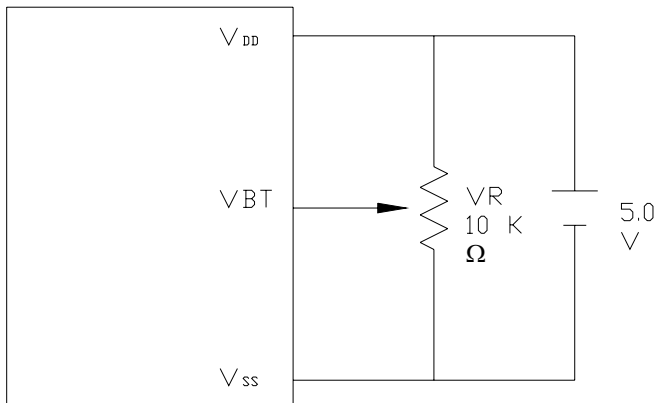
## 5. Optical Characteristics

### 5.1 Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
View Angle	(V) $\theta$	$CR \geq 20$	-80		80	deg
	(H) $\varphi$	$CR \geq 20$	-80		80	deg
Contrast Ratio	CR	—		100		—
Response Time 25°C	T rise	—		40		us
	T fall	—		40		us

### 5.2 Brightness control

LCD Module block diagram





## 6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	Vss	0V	Supply Voltage for logic <b>GND</b>
2	Vdd	5V	Supply Voltage for logic <b>5V</b>
3	VBT	3.0	Brightness control voltage
4	RS	H/L	H:DATA, L:Instruction code
5	R/W	H/L	H:Read(MPU→Module)L:Write(MPU→Module)
6	E	H,H→L	Chip enable signal
7	DB0	H/L	Data bit 0
8	DB1	H/L	Data bit 1
9	DB2	H/L	Data bit 2
10	DB3	H/L	Data bit 3
11	DB4	H/L	Data bit 4
12	DB5	H/L	Data bit 5
13	DB6	H/L	Data bit 6
14	DB7	H/L	Data bit 7
15	NC		
16	NC		

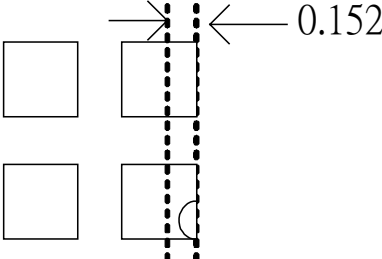
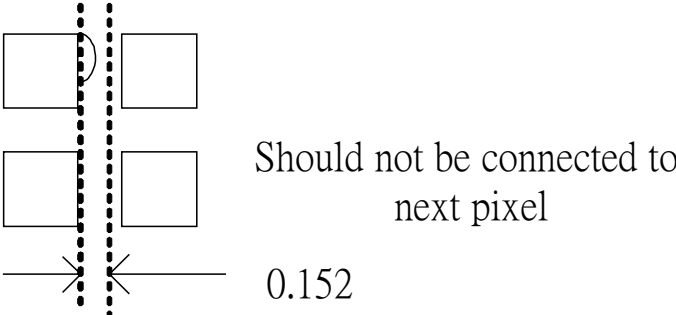
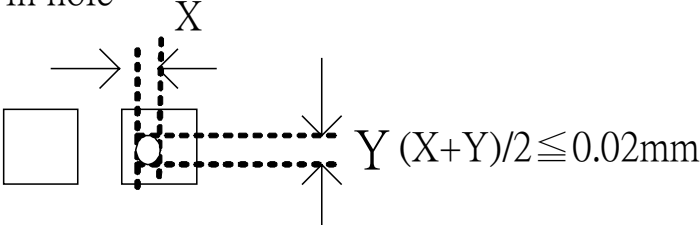
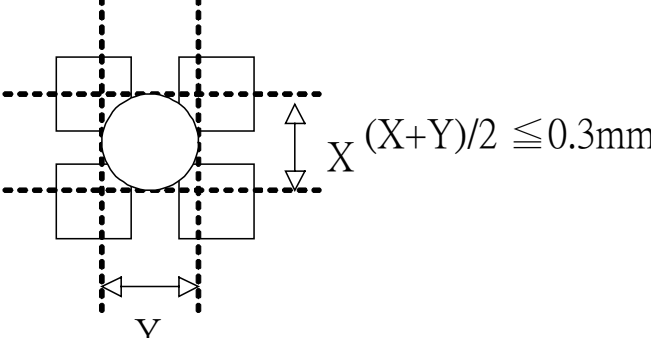


## 7.Quality Assurance

NO.	Parameter	Criteria																										
1	Black or White spots	<table border="1"> <thead> <tr> <th rowspan="2">Zone Dimension</th> <th colspan="2">Acceptable Number</th> <th rowspan="2">Class Of Defects</th> <th rowspan="2">Acceptable Level</th> </tr> <tr> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td><math>D &lt; 0.15</math></td> <td>*</td> <td>*</td> <td rowspan="4">Minor</td> <td rowspan="4">2.5</td> </tr> <tr> <td><math>0.15 \leq D \leq 0.2</math></td> <td>4</td> <td>4</td> </tr> <tr> <td><math>0.2 \leq D \leq 0.25</math></td> <td>2</td> <td>2</td> </tr> <tr> <td><math>D \leq 0.3</math></td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p><math>D = (\text{Long} + \text{Short})/2</math>      *: Disregard</p>	Zone Dimension	Acceptable Number		Class Of Defects	Acceptable Level	A	B	$D < 0.15$	*	*	Minor	2.5	$0.15 \leq D \leq 0.2$	4	4	$0.2 \leq D \leq 0.25$	2	2	$D \leq 0.3$	0	1					
Zone Dimension	Acceptable Number			Class Of Defects	Acceptable Level																							
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2	Scratch, Substances	<table border="1"> <thead> <tr> <th colspan="2">Zone X(mm) Y(mm)</th> <th colspan="2">Acceptable Number</th> <th rowspan="2">Class Of Defects</th> <th rowspan="2">Acceptable Level</th> </tr> <tr> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td>*</td> <td><math>0.04 \geq W</math></td> <td>*</td> <td>*</td> <td rowspan="4">Minor</td> <td rowspan="4">2.5</td> </tr> <tr> <td><math>3.0 \geq L</math></td> <td><math>0.06 \geq W</math></td> <td>4</td> <td>4</td> </tr> <tr> <td><math>2.0 \geq L</math></td> <td><math>0.08 \geq W</math></td> <td>2</td> <td>3</td> </tr> <tr> <td>—</td> <td><math>0.1 &lt; W</math></td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>X: Length    Y: Width    *: Disregard Total defects should not exceed 4/module</p>	Zone X(mm) Y(mm)		Acceptable Number		Class Of Defects	Acceptable Level	A	B	*	$0.04 \geq W$	*	*	Minor	2.5	$3.0 \geq L$	$0.06 \geq W$	4	4	$2.0 \geq L$	$0.08 \geq W$	2	3	—	$0.1 < W$	0	1
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—	$0.1 < W$	0	1																									
3	Air Bubbles ( between glass & polarizer)	<table border="1"> <thead> <tr> <th rowspan="2">Zone Dimension</th> <th colspan="2">Acceptable Number</th> <th rowspan="2">Class Of Defects</th> <th rowspan="2">Acceptable Level</th> </tr> <tr> <th>A</th> <th>B</th> </tr> </thead> <tbody> <tr> <td><math>D \leq 0.15</math></td> <td>*</td> <td>*</td> <td rowspan="3">Minor</td> <td rowspan="3">2.5</td> </tr> <tr> <td><math>0.15 &lt; D \leq 0.25</math></td> <td>2</td> <td>*</td> </tr> <tr> <td><math>0.25 &lt; D</math></td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>*: Disregard Total defects shall not excess 3/module.</p>	Zone Dimension	Acceptable Number		Class Of Defects	Acceptable Level	A	B	$D \leq 0.15$	*	*	Minor	2.5	$0.15 < D \leq 0.25$	2	*	$0.25 < D$	0	1								
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4	Uniformity	<p>(1) Pixel shape (with Dent)</p>  <p>(2) Pixel shape (With Projection)</p>  <p>Should not be connected to next pixel</p> <p>(3) Pin hole</p>  <p><math>(X+Y)/2 \leq 0.02\text{mm}</math></p> <p>(Less than 0.1mm is no counted)</p> <p>(4) Deformation</p>  <p><math>(X+Y)/2 \leq 0.3\text{mm}</math></p> <p>Total acceptable number : 1/pixel,5/cell</p>
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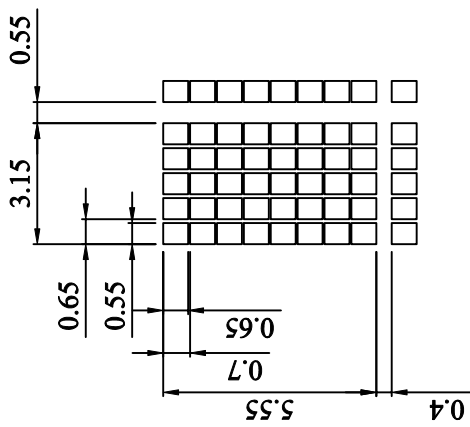
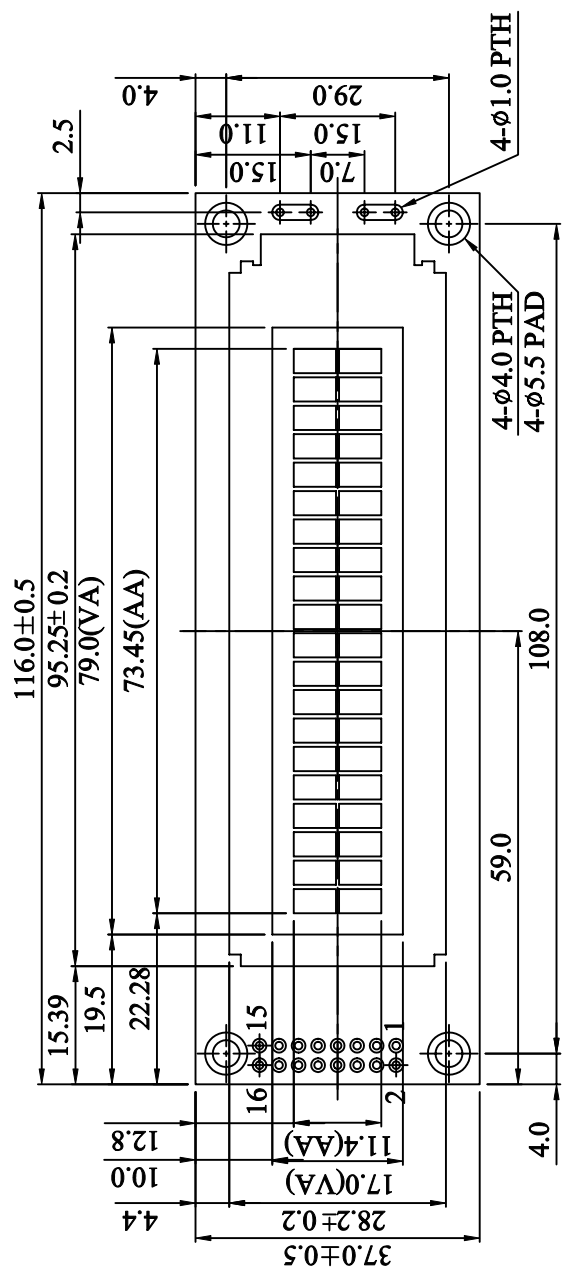
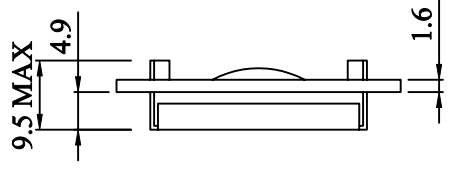
## 8. Reliability

### Content of Reliability Test

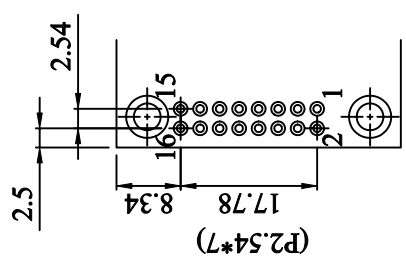
Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High Temperature storage	Endurance test applying the high storage temperature for a long time.	60°C 200hrs	—
2	Low Temperature storage	Endurance test applying the high storage temperature for a long time.	-20°C 200hrs	—
3	High Temperature Operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	50°C 200hrs	—
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time.	0°C 200hrs	—
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time.	60°C,90%RH 96hrs	—
6	High Temperature/ Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	40°C,90%RH 96hrs	—
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. 	-20°C/60°C 10 cycles	—
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10~22Hz→1.5mmp-p 22~500Hz→1.5G Total 0.5hrs	—
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G Half sign wave 11 msdc 3 times of each direction	—
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115mbar 40hrs	—
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V,RS=1.5kΩ CS=100pF 1 time	—

\*\*\*Supply voltage for logic system=5V.

PIN NO.	SYMBOL
1	V <sub>ss</sub>
2	V <sub>dd</sub>
3	V <sub>o</sub>
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7
15	NC
16	NC



DOT SIZE  
SCALE 5/1



PIN DETAIL

The non-specified tolerance of dimension is ±0.3 mm .

SCALE: 1/1	REV: 0	One Stop Displays
UNIT: mm	PAGE: 1/1	MODEL
APPROVE CHEN	CHECK TOM	TITLE
DRAW Davidy	DWGNO. 05/20/04	LCM DRAWING
		PLM04052001



### 12-2.1 Function description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

#### Busy Flag (BF)

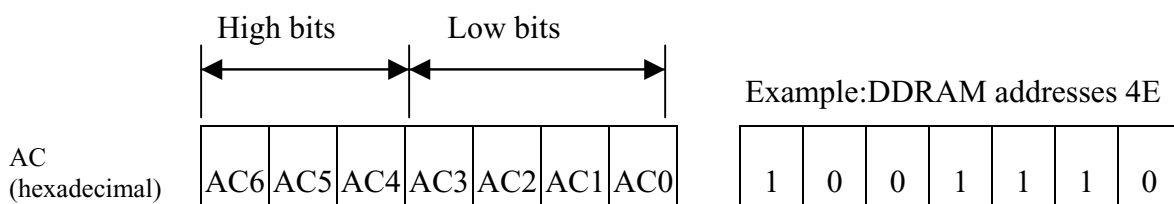
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

#### Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

#### Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationship between DDRAM addresses and positions on the liquid crystal display.



#### DDRAM Address



Display position DDRAM address

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16

00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Example: 2-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.



## Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character Patterns (CGRAM Data)

For 5 \* 8 dot character patterns

Character Codes ( DDRAM data )								CGRAM Address						Character Patterns ( CGRAM data )															
7	6	5	4	3	2	1	0	5			4			3			2			1			0						
High				Low				High			Low			High				Low											
0 0 0 0 * 0 0 0								0 0 0						0	0	0	*	0	0	0	0	* * *	0				0	Character pattern( 1 )	
														0	0	1	*	0	0	0	0	* * *	0 0 0				0		
														0	1	0	*	0	0	0	0	* * *	0 0 0				0		
														0	1	1	*	0	0	0	0	* * *	0				0 0 0		0
														1	0	0	*	0	0	0	0	* * *	0 0				0 0 0		0
														1	0	1	*	0	0	0	0	* * *	0 0 0				0		0
														1	1	0	*	0	0	0	0	* * *	0 0 0 0				0		0
														1	1	1	*	0	0	0	0	* * *	0 0 0 0 0				0		0
														0	0	0	*	0	0	0	0	* * *	0				0 0 0 0		0
														0	0	1	*	0	0	0	0	* * *	0				0 0 0 0		0
0 0 0 0 * 0 0 1								0 0 1						0	1	1	*	0	0	0	1	* * *	0 0				0 0 0	Character pattern( 2 )	
														1	0	0	*	0	0	0	1	* * *	0 0 0				0 0 0		
														1	0	1	*	0	0	0	1	* * *	0 0 0				0 0 0		
														1	1	0	*	0	0	0	1	* * *	0 0 0				0 0 0		
0 0 0 0 * 1 1 1								1 1 1						1	0	0	*	1	1	1	1	* * *	0 0 0 0 0				Cursor pattern		
														1	0	1	*	1	1	1	1	* * *	0 0 0 0 0						
														1	1	0	*	1	1	1	1	* * *	0 0 0 0 0						
														1	1	1	*	1	1	1	1	* * *	0 0 0 0 0						

For 5 \* 10 dot character patterns

Character Codes ( DDRAM data )										CGRAM Address										Character Patterns ( CGRAM data )																						
7	6	5	4	3	2	1	0	5					4					3					2					1					0									
High					Low					High					Low					High					Low																	
0 0 0 0 * 0 0 0										0 0										0	0	0	0	0	0	0	0	0	0	* * *	0 0 0 0 0 0					0					Character pattern	
																				0	0	0	0	1	0	0	0	0	0	* * *	0 0 0 0 0 0					0						
																				0	0	1	0	0	0	0	0	0	0	* * *	0					0 0 0 0 0	0					
																				0	0	1	1	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				0	1	0	0	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				0	1	0	1	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				0	1	1	0	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				0	1	1	1	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				1	0	0	0	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
																				1	0	0	1	0	0	0	0	0	0	* * *	0 0 0 0 0					0						
1 1 1 1										1 1 1 1										1	0	1	0	*	1	1	1	1	1	* * *	* * * * *					* * * * *					Cursor pattern	
																				1	0	1	0	*	1	1	1	1	1	* * *	* * * * *					* * * * *						

■ : " High "



9-2.2 C.G ROM table. table 2

Code J: English – Japanese Font

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)			0	1	2	3	4				5	6	7	8	9
LLLH	(2)	!	0	1	2	3	4	5			6	7	8	9	0	1
LLHL	(3)	"	0	1	2	3	4	5			6	7	8	9	0	1
LLHH	(4)	#	0	1	2	3	4	5			6	7	8	9	0	1
LHLL	(5)	\$	0	1	2	3	4	5			6	7	8	9	0	1
LHLH	(6)	%	0	1	2	3	4	5			6	7	8	9	0	1
LHHL	(7)	&	0	1	2	3	4	5			6	7	8	9	0	1
LHHH	(8)	'	0	1	2	3	4	5			6	7	8	9	0	1
HLLL	(1)	(	0	1	2	3	4	5			6	7	8	9	0	1
HLLH	(2)	)	0	1	2	3	4	5			6	7	8	9	0	1
HLHL	(3)	*	0	1	2	3	4	5			6	7	8	9	0	1
HLHH	(4)	+	0	1	2	3	4	5			6	7	8	9	0	1
HHLL	(5)	,	0	1	2	3	4	5			6	7	8	9	0	1
HHLH	(6)	-	0	1	2	3	4	5			6	7	8	9	0	1
HHHL	(7)	.	0	1	2	3	4	5			6	7	8	9	0	1
HHHH	(8)	/	0	1	2	3	4	5			6	7	8	9	0	1







# Code C: English - Cyrillic Font

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)			0	1	2	3	4			5	6	7	8	9	0
LLLH	CG RAM (2)		!	1	2	3	4				5	6	7	8	9	0
LLHL	CG RAM (3)		!"	2	3	4	5	6			7	8	9	0	1	2
LLHH	CG RAM (4)		!"#	3	4	5	6	7			8	9	0	1	2	3
LHLL	CG RAM (5)		!"#\$	4	5	6	7	8			9	0	1	2	3	4
LHLH	CG RAM (6)		!"#\$%	5	6	7	8	9			0	1	2	3	4	5
LHHL	CG RAM (7)		!"#\$%&	6	7	8	9	0			1	2	3	4	5	6
LHHH	CG RAM (8)		!"#\$%&'	7	8	9	0	1			2	3	4	5	6	7
HLLL	CG RAM (1)		!"#\$%	6	7	8	9	0			1	2	3	4	5	6
HLLH	CG RAM (2)		!"#\$%&	7	8	9	0	1			2	3	4	5	6	7
HLHL	CG RAM (3)		!"#\$%&'	8	9	0	1	2			3	4	5	6	7	8
HLHH	CG RAM (4)		!"#\$%&'&	9	0	1	2	3			4	5	6	7	8	9
HHLL	CG RAM (5)		!"#\$%	7	8	9	0	1			2	3	4	5	6	7
HHLH	CG RAM (6)		!"#\$%&	8	9	0	1	2			3	4	5	6	7	8
HHHL	CG RAM (7)		!"#\$%&'	9	0	1	2	3			4	5	6	7	8	9
HHHH	CG RAM (8)		!"#\$%&'&	0	1	2	3	4			5	6	7	8	9	0



### 9-2.3. Instruction table

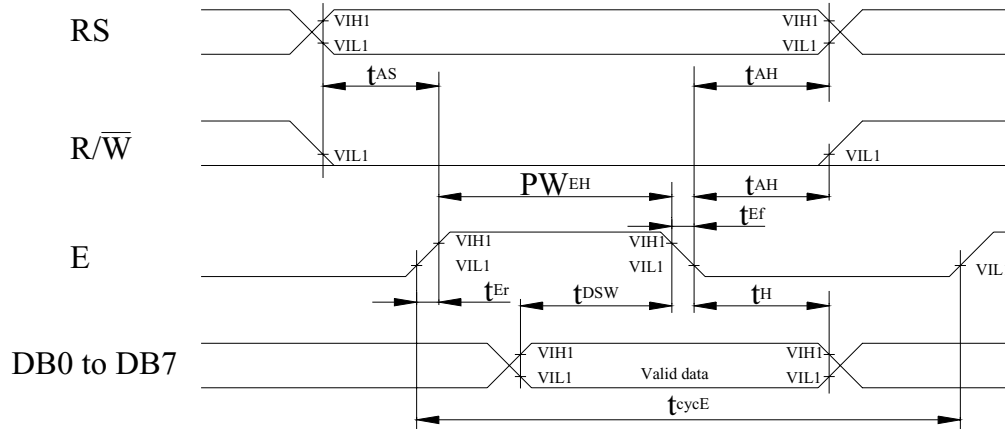
Instruction	Instruction Code										Description	Execution time	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms	
Return Home	0	0	0	0	0	0	0	0	0	1	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms	
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 $\mu$ s
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 $\mu$ s
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	—	—	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39 $\mu$ s
Function Set	0	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5 $\times$ 11 dots/5 $\times$ 8 dots)	39 $\mu$ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address counter.	39 $\mu$ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address counter.	39 $\mu$ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0 $\mu$ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM).	43 $\mu$ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM).	43 $\mu$ s

— : don't care



## 9-2.4 Timing characteristics

### Write Operation

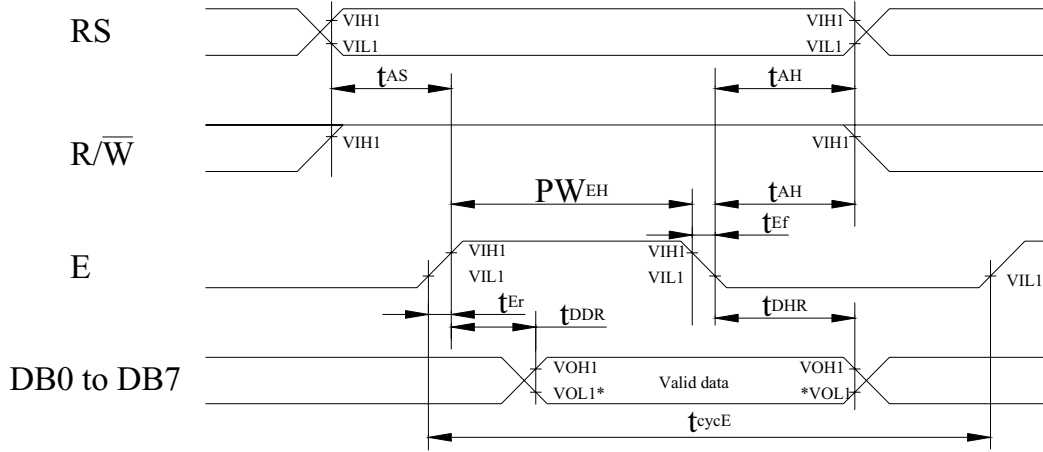


$T_a=25^{\circ}\text{C}, V_{dd}=5.0\pm 0.5\text{V}$

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	$t_{\text{cycE}}$	500	—	—	ns
Enable pulse width (high level)	$PW_{\text{EH}}$	230	—	—	ns
Enable rise/fall time	$t_{\text{Er}}, t_{\text{Ef}}$	—	—	20	ns
Address set-up time (RS, R/W to E)	$t_{\text{AS}}$	40	—	—	ns
Address hold time	$t_{\text{AH}}$	10	—	—	ns
Data set-up time	$t_{\text{DSW}}$	80	—	—	ns
Data hold time	$t_{\text{H}}$	10	—	—	ns



## Read Operation



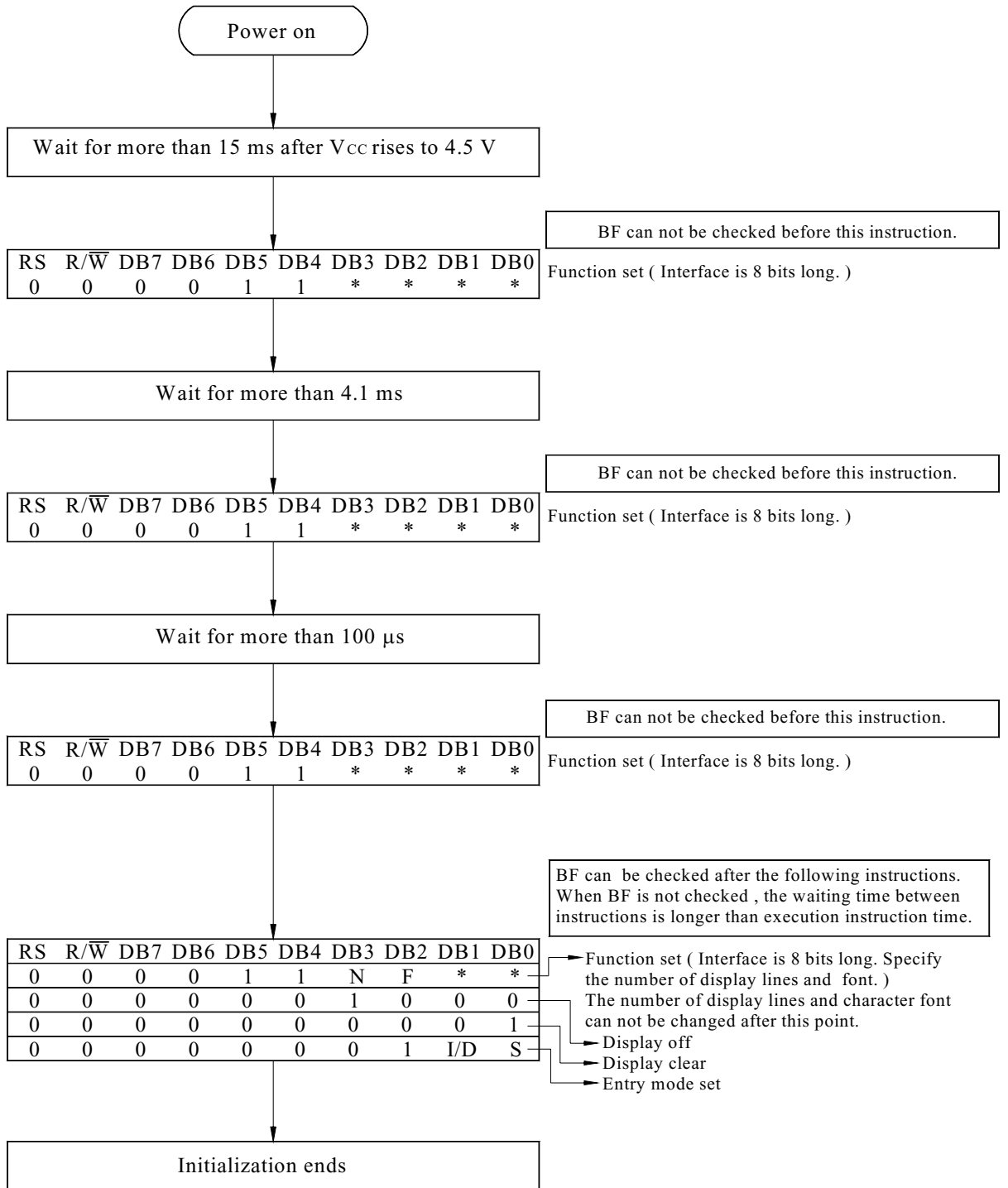
NOTE: \*VOL1 is assumed to be 0.8V at 2 MHz operation.

$T_a=25^{\circ}\text{C}, V_{dd}=5.0\pm 0.5\text{V}$

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	$t_{cycE}$	500	—	—	ns
Enable pulse width (high level)	$PW_{EH}$	230	—	—	ns
Enable rise/fall time	$t_{Er}, t_{Ef}$	—	—	20	ns
Address set-up time (RS, R/W to E)	$t_{AS}$	40	—	—	ns
Address hold time	$t_{AH}$	10	—	—	ns
Data delay time	$t_{DDR}$	—	—	160	ns
Data hold time	$t_{DHR}$	5	—	—	ns



## 9-2.5 Initializing software of LCM 8-bit interface



8-Bit Ineterface

## 4-bit interface

