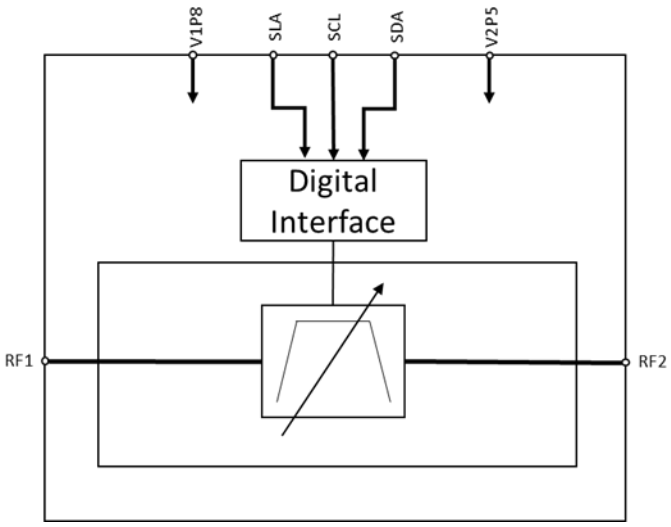
OTFL101 Datasheet

Features

- 2.5 GHz to 7.5 GHz Frequency Range
- Digitally Tunable
- Up to 1.5 GHz of Instantaneous Bandwidth (IBW)
- In Band IIP3: 47 dBm
- Power Supplies: +1.8 V, +2.5 V
- Single Chip Replacement for Discrete Filter Banks
- Flip Chip C4 Bump
- Die Dimension: 2.34 mm x 1.634 mm
- MatLab Explorer App Available

Block Diagram



Description

The OTFL101 is a digitally tunable bandpass filter. This wide range of control (many different combinations) provides flexibility of passband tuning from 2.5 GHz to 7.5 GHz. The typical insertion loss is 7 dB.

This device delivers spur/interference removal techniques over multiple center frequencies to RF systems while providing 10x PCB area reduction in comparison to a switched filter bank or cavity tuned filter solution. These application areas include but not limited, radio, communication, military radar, and instrumentation.

MatLab Explorer App was developed to assist customers to use in system chain analysis and optimization. These data driven models predict amplitude and phase very accurately in response to the user defined input controls. This advanced capability enables intimate exploration of the device's degrees of freedom.

Applications

- Software Defined Radio
- EW, Radar & ECM
- Satcom & Space
- Instrumentation
- Industrial & Medical Equipment

Related Items

- Evaluation Board: OTFL101-EVAL
- MatLab Explorer App

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Revision History

September 2021, Rev A (Initial Release)

February 2022, Rev B (General Updates)

Specifications

For all supplied data in the table below, the nominal conditions are defined as the following:

- Ambient Temperature: 25°C
- Voltages: V1P8 = 1.8V, V2P5 = 2.5V
- Measured on the OTFL101-EVAL evaluation board and de-embedded using Automatic Fixture Removal (AFR)

Table 1 – Specifications

Parameter	Test Configuration	Units	Min.	Typ.	Max.
Operating Temperature		°C	-40		85
RF Design					
Operating RF Frequency		GHz	2.5		7.5
Center Frequency		GHz	3		7
Insertion Loss		dB		7	
Instantaneous Bandwidth (3dB)		GHz		1	
Input Return Loss		dB		15	
Output Return Loss		dB		15	
IP0.1dB Compression		dBm		28	
IIP3 (In Band)		dBm		47	
Group Delay Flatness		ns			0.5
Amplitude Settling Time		ns		tbd	
Phase Settling Time		ns		tbd	
20dB Rejection (LS)		GHz		0.8 x fcenter	
20dB Rejection (HS)		GHz		1.3 x fcenter	
Re-Entry Rejection	≤30 dB	GHz		5.4 x fcenter	
Serial Interface Design, Tuning Digital Control					
Operating Frequency		MHz		10	tbd
Logic Inputs	I/O: SLA,SCL,SDA				
Logic Low		V		0	
Logic High		V		1.8	
Power Supplies					
1.8V					
Voltage		V	1.7	1.8	1.9
Current		uA			10
2.5V					
Voltage		V	2.4	2.5	2.6
Current		uA			10

Table 2 – Examples of Tuning Settings

C1	C2	C3	C4	C5	Fc, GHz	-3dB BW, MHz
31	31	31	31	31	3	757
28	28	28	28	28	3.11	710
19	19	19	19	19	3.5	845
13	13	13	13	13	3.9	919
12	12	12	12	12	4	844
8	8	8	8	8	4.5	949
6	6	6	6	6	5	1148
4	4	4	4	4	5.5	1222
3	3	3	3	3	6	1384
1	1	1	1	1	6.5	1689
0	0	0	0	0	7	1657

Absolute Maximum Ratings

Table 3 – Absolute Maximum Ratings & ESD Ratings

Parameter	Rating
Maximum RF Input Power	tbd
Storage Temperature Range	-65C to +150C
c4 Reflow	260C
Junction Temperature	+125C
Electrostatic Discharge	
Digital Pins (HBM)	2000 V
RF Pins (HBM)	2000 V

Typical Performance Plots

For the measured plots below, each of the five stage's capacitor banks (C1-5) are set to the same decimal value. Tuning of the center frequency and fine-tuning passband flatness are possible with the topology. Many combinations are possible with 32 states (2^5) filter banks, but for simplicity, these values are tied together.

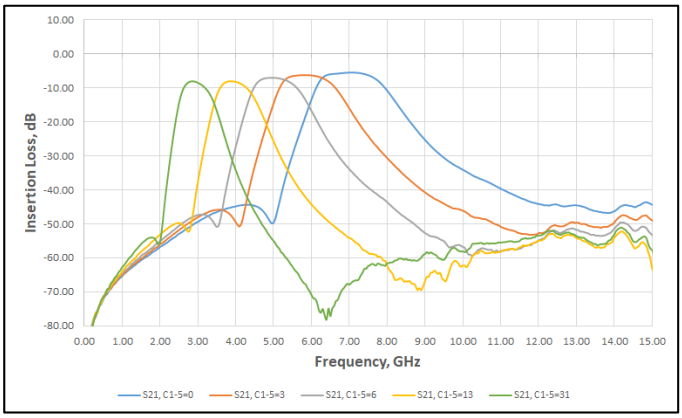

Figure 1 – Insertion Loss vs Grouped Tuning Settings

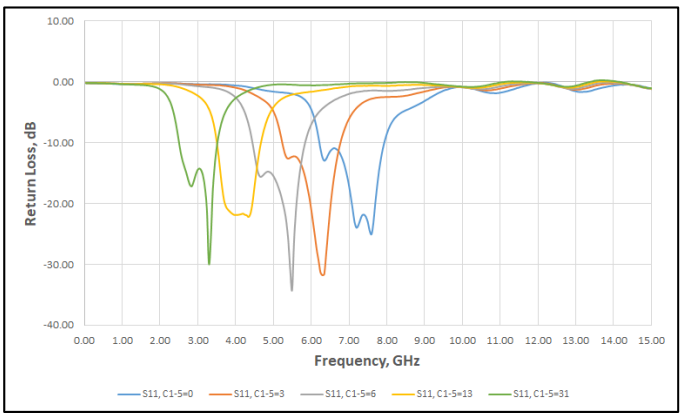

Figure 2 – Input Return Loss vs Grouped Tuning Settings

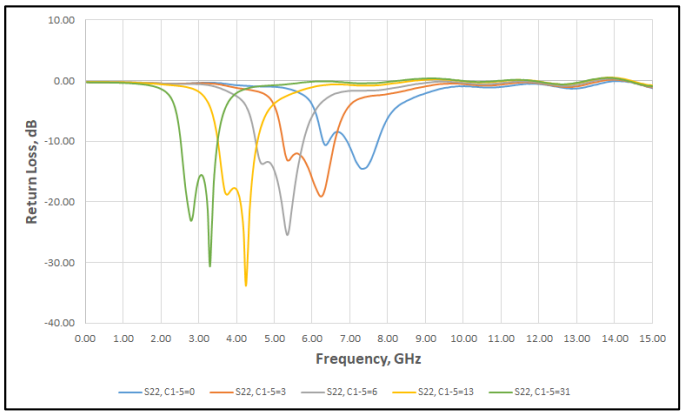

Figure 3 – Output Return Loss vs Grouped Tuning Settings

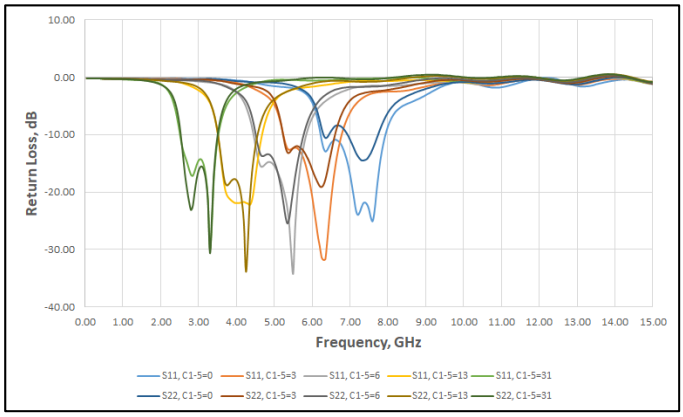

Figure 4 – Overlaid S11 and S22 Return Loss

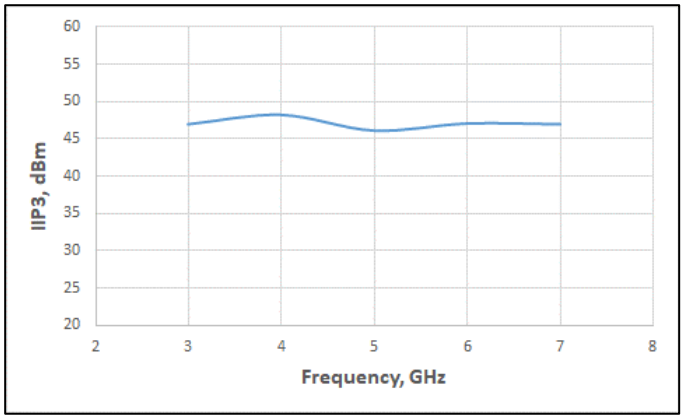

Figure 7 – In-Band IIP3 vs Frequency

Functional Information

Filter Design

The OTFL101 is a digitally tunable frequency of operation bandpass filter. The IC features 5 bits (32 states) of digital control at every stage, with a total of 5 stages. This wide range of control (many different combinations) provides flexibility of frequency tuning from 2.5 GHz to 7.5 GHz, with 20dB filter rejection of 0.8 x center frequency on the low side and 1.3 x center frequency on the high side.

Serial Interface Design

A simple 3-wire serial interface is utilized to control the filter. The interface utilizes the following signals for communication:

- SCL: Single ended clock input to chip
- SDA: Single ended data input to chip
- SLA: Single ended latch input to chip (active low)

A diagram of the digital interface is provided below:

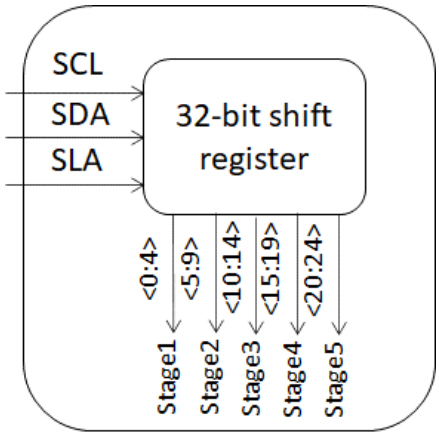

Figure 5 – Digital Interface Overview

A timing diagram is provided below for these signals:

Figure 6 - Interface Timing Diagram

The data message is 32 bits long. The OTFL101 filter utilizes the first 25 bits in the data stream (5 bits x 5 stages), so bits 25-31 are not used in this chip design. The serial data is latched into the filter when the SLA pin goes low. The full list of the used functions is shown below:

Table 4 – Control Bit Description

Bit	Name	Description
31	n/a	not used
30	n/a	not used
29	n/a	not used
28	n/a	not used
27	n/a	not used
26	n/a	not used
25	n/a	not used
24	Stage5_b4	Stage 5, Bit 4 (MSB)
23	Stage5_b3	Stage 5, Bit 3
22	Stage5_b2	Stage 5, Bit 2
21	Stage5_b1	Stage 5, Bit 1
20	Stage5_b0	Stage 5, Bit 0 (LSB)
19	Stage4_b4	Stage 4, Bit 4 (MSB)
18	Stage4_b3	Stage 4, Bit 3
17	Stage4_b2	Stage 4, Bit 2
16	Stage4_b1	Stage 4, Bit 1
15	Stage4_b0	Stage 4, Bit 0 (LSB)
14	Stage3_b4	Stage 3, Bit 4 (MSB)
13	Stage3_b3	Stage 3, Bit 3
12	Stage3_b2	Stage 3, Bit 2
11	Stage3_b1	Stage 3, Bit 1
10	Stage3_b0	Stage 3, Bit 0 (LSB)
9	Stage2_b4	Stage 3, Bit 4 (MSB)
8	Stage2_b3	Stage 2, Bit 3
7	Stage2_b2	Stage 2, Bit 2
6	Stage2_b1	Stage 2, Bit 1
5	Stage2_b0	Stage 2, Bit 0 (LSB)
4	Stage1_b4	Stage 1, Bit 4 (MSB)
3	Stage1_b3	Stage 1, Bit 3
2	Stage1_b2	Stage 1, Bit 2
1	Stage1_b1	Stage 1, Bit 1
0	Stage1_b0	Stage 1, Bit 0 (LSB)

I/O Functional Description

Table 5 – Filter Pin Description

Pin	Name	Description
1	RF2	RF Port 2 (50Ω). External DC block is not required, except for when voltages are present.
2	RF1	RF Port 1 (50Ω). External DC block is not required, except for when voltages are present.
3	SLA	Serial latch input signal.
4	SCL	Serial clock input signal.
5	SDA	Serial data input signal.
6	V1P8	1.8V power supply. Place 0.1uF and 100pF decoupling capacitors close to pin.
7	V2P5	2.5V power supply. Place 0.1uF and 100pF decoupling capacitors close to pin.
8-19	GND	Common GND. Connect to PCB ground.

Pin Configuration

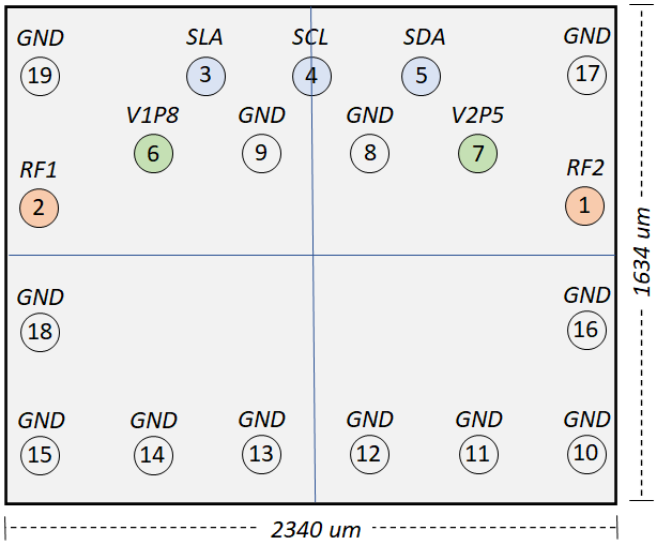

Figure 7 – Pin Configuration (Bumps Up)

Note: Drawing not drawn to scale.

Table 6 – Pin Coordinates (Bumps Up)

Pin	Name	Pin Center (um)	
		X	Y
1	RF2	1000	200
2	RF1	-1000	200
3	SLA	-400	600
4	SCL	0	600
5	SDA	400	600
6	V1P8	-600	380.36
7	V2P5	600	380.36
8	GND	200	380.36
9	GND	-200	380.36
10	GND	1000	-600
11	RFC	600	-600
12	GND	200	-600
13	GND	-200	-600
14	GND	-600	-600
15	GND	-1000	-600
16	GND	1000	-200
17	GND	1000	600
18	GND	-1000	-200
19	GND	-1000	600

Note: All coordinates are referenced to the die center and refer to the center of the pin.

Die Mechanical Specifications

Table 7 - Die Mechanical Specifications

Parameter	Unit	Min	Typ	Max	Notes
Die size (x,y)	mm		2.34 x 1.634		+/- 10um
Die thickness	um		300		
Bump Material	-		SnAg		
Bump Pitch	um	280			
Bump Height	um		75		
Bump Diameter	um		90		

Soldermask defined pads are utilized for the bump landing areas. Please refer to the supplied Altium footprint file and the OTFL101-EVAL evaluation board artwork files for the exact landing pattern dimensions and implementation.