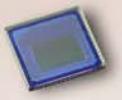
OmniVision



datasheet

1/4" CMOS QXGA (3.2 Megapixel) CameraChip™ sensor
with OmniPixel3™ technology

OV3640

color CMOS QXGA (3.2 Megapixel) CameraChip™ sensor with OmniPixel3™ technology

datasheet (COB)

Version 1.0
May 2007

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- cellular phones
- toys
- PC multimedia
- digital still camera

ordering information

- **OV03640-G00A** (color, no chip probing, no backgrinding)

features

- ultra low power and low cost
- automatic image control functions: automatic exposure control (AEC), automatic white balance (AWB), automatic band filter (ABF), automatic 50/60 Hz luminance detection, and automatic black level calibration (ABLC)
- programmable controls for frame rate, AEC/AGC 16-zone size/position/weight control, mirror and flip, scaling, cropping, windowing, and panning
- image quality controls: color saturation, hue, gamma, sharpness (edge enhancement), lens correction, defective pixel canceling, and noise canceling
- support for output formats: RAW RGB, RGB565/555/444, CCIR656, YUV422/420, YCbCr422 and compression
- support for images sizes: QXGA, and any arbitrary size scaling down from QXGA
- support for video or snapshot operations
- support for horizontal and vertical sub-sampling
- support for data compression output
- support for auto focus control (AFC)
- support for anti-shake
- support for internal and external frame synchronization
- support for LED and flash strobe mode
- standard serial SCCB interface
- digital video port (DVP) parallel output interface
- MIPI serial output interface
- support for second camera chip-sharing ISP and MIPI interface
- embedded microcontroller
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- programmable I/O drive capability

key specifications

- **active array size:** 2048 x 1536
- **power supply:**
  core: 1.5VDC ± 5%
  analog: 2.5 ~ 3.0V
  I/O: 1.7 ~ 3.0V
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -20°C to 70°C
  stable image: 0°C to 50°C
- **output formats (8-bit):** YUV(422/420) / YCbCr422, RGB565/555/444, CCIR656, 8-bit compression data, 8-/10-bit raw RGB data
- **lens size:** 1/4"
- **lens chief ray angle:** 25° non-linear (see Table 10-1)
- **input clock frequency:** 6 ~ 27 MHz
- **maximum image transfer rate:**
  QXGA (2048x1536): 15fps for QVGA and any size scaling down from QVGA
  XGA (1024x768): 30fps for XGA and any size scaling down from XGA
- **sensitivity:** TBD
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **shutter:** rolling shutter
- **scan mode:** progressive
- **maximum exposure interval:** 1560 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 1.75 µm x 1.75 µm
- **well capacity:** TBD
- **dark current:** TBD
- **fixed pattern noise (FPN):** TBD
- **image area:** 3626 µm x 2709 µm
- **die dimensions:** 6300 µm x 6140 µm

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV3640 image sensor. The die information is shown in section 9.

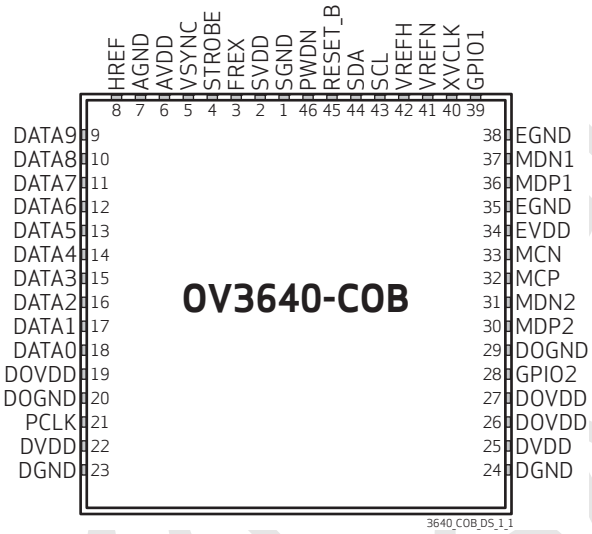
table 1-1 signal descriptions (sheet 1 of 2)

pad number	signal name	pad type	description	default I/O status
01	SGND	ground	ground for sensor circuit	
02	SVDD	power	power for sensor circuit	
03	FREX	I/O	frame exposure input, anti-shake status output, or OTP memory output	input
04	STROBE	I/O	strobe output or scan chain test mode input	input
05	VSYNC	I/O	vertical sync output	input
06	AVDD	power	analog power	
07	AGND	ground	analog power	
08	HREF	I/O	horizontal reference output	input
09	DATA9	I/O	digital video port (DVP) bit[9]	input
10	DATA8	I/O	digital video port (DVP) bit[8]	input
11	DATA7	I/O	digital video port (DVP) bit[7]	input
12	DATA6	I/O	digital video port (DVP) bit[6]	input
13	DATA5	I/O	digital video port (DVP) bit[5]	input
14	DATA4	I/O	digital video port (DVP) bit[4]	input
15	DATA3	I/O	digital video port (DVP) bit[3]	input
16	DATA2	I/O	digital video port (DVP) bit[2]	input
17	DATA1	I/O	digital video port (DVP) bit[1]	input
18	DATA0	I/O	digital video port (DVP) bit[0]	input
19	DOVDD	power	power for I/O circuit	
20	DOGND	ground	ground for I/O circuit	
21	PCLK	I/O	pixel clock output	input
22	DVDD	reference	power for digital core	
23	DGND	ground	ground for digital core	
24	DGND	ground	ground for digital core	

table 1-1 signal descriptions (sheet 2 of 2)

pad number	signal name	pad type	description	default I/O status
25	DVDD	reference	power for digital core	–
26	DOVDD	power	power for I/O circuit	
27	DOVDD	power	power for I/O circuit	
28	GPIO2	I/O	general purpose I/O (GPIO) 2	input
29	DOGND	ground	ground for I/O circuit	
30	MDP2	output	MIPI second data lane positive output	
31	MDN2	output	MIPI second data lane negative output	
32	MCP	output	MIPI clock lane positive output	
33	MCN	output	MIPI clock lane negative output	
34	EVDD	reference	power for MIPI core	
35	EGND	ground	ground for MIPI core	
36	MDP1	output	MIPI first data lane positive output	
37	MDN1	output	MIPI first data lane negative output	
38	EGND	ground	ground for MIPI core	
39	GPIO1	I/O	general purpose I/O (GPIO) 1	input
40	XVCLK	input	system input clock	
41	VREFN	reference	internal analog reference	
42	VREFH	reference	internal analog reference	
43	SCL	input	SCCB input clock	
44	SDA	I/O	SCCB data	
45	RESET_B	input	reset (active low with internal pull-up resistor)	
46	PWDN	input	power down active high with internal pull-down resistor	

figure 1-1 pad diagram



2 system level description

2.1 overview

The OV3640 (color) CAMERACHIP™ sensor is a low voltage, high performance 1/4-inch 3.2 megapixel CMOS image sensor that provides the full functionality of a single chip QXGA (2048x1536) camera using OmniPixel3™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or arbitrarily scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface or MIPI interface.

The OV3640 has an image array capable of operating at up to 15 frames per second (fps) in QXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface, MIPI interface or embedded microcontroller. The OV3640 also includes a compression engine for increased processing power. In addition, Omnivision CAMERACHIP sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

The OV3640 has an embedded a microcontroller, which can be combined with an internal auto focus engine and programmable general purpose I/O modules (GPIO), for external auto focus control. It also provides an anti-shake function with an internal anti-shake engine. For storage purposes, the OV3640 also includes a one-time programmable (OTP) memory.

The OV3640 supports both a digital video parallel port and a serial MIPI port. The MIPI and ISP interface can be used for a second camera sensor without requiring a dual serial port camera system.

2.2 architecture

The OV3640 sensor core generates stream pixel data at a constant frame rate, indicated by HREF and VSYNC. **figure 2-1** shows the functional block diagram of the OV3640 image sensor. **figure 2-2** shows an example application using an OV3640 sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV3640 block diagram

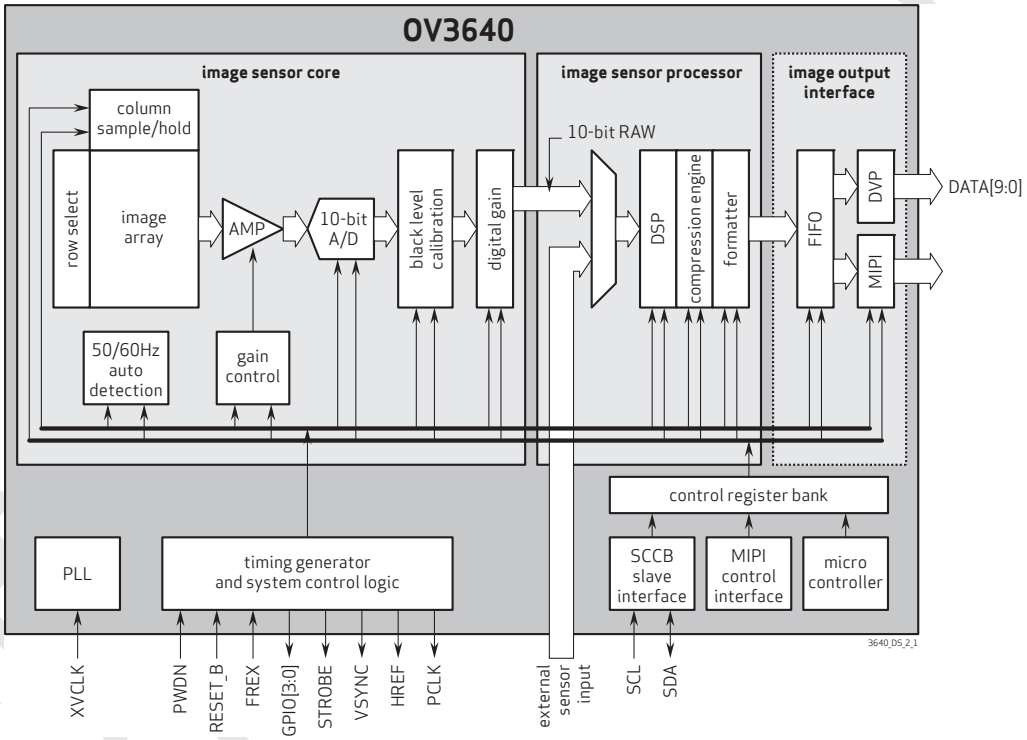
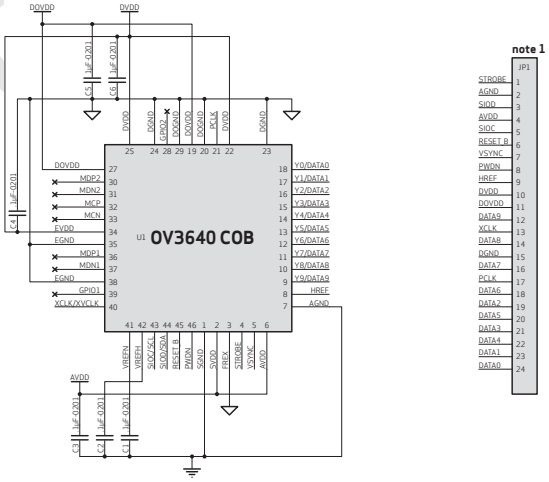


figure 2-2 reference design schematic



note 1 flex cable to Molex 52437-2491

note 2 PWDN should be connected to ground outside of module if unused.
RESET_B should be connected to DOVDD outside of module if unused.
AVDD is 2.45V - 3.0V of sensor analog power (clean).
DVDD is 1.5V +/- 10% of sensor digital power (clean).
DOVDD is 1.7V - 3.0V of sensor digital I/O power (clean).
sensor AGND and DGND should be separated and connected to a single point outside the PCB (do not connect inside the module).
capacitors should be close to the related sensor pins.
DATA[9:0] is the sensor's 10-bit RGB output (DATA[9]: MSB; DATA[0]: LSB).

3640_CSP_DS_2_2

2.3 I/O control

The OV3640 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output driving capability control	0x30B2[1:0]	R_PAD[1:0]: Output driving capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] I/O control	{0x30B1[1:0], 0x30B0[7:0]}	Input/Output selection for the DATA[9:0] pads : 0: Input 1: Output
GPIO2 I/O control	0x30B1[7]	Input/Output selection for the GPIO2 pad : 0: Input 1: Output
GPIO1 I/O control	0x30B1[6]	Input/Output selection for the GPIO1 pad : 0: Input 1: Output
VSYNC I/O control	0x30B1[5]	Input/Output selection for the VSYNC pad : 0: Input 1: Output
HREF I/O control	0x30B1[2]	Input/Output selection for the HREF pad : 0: Input 1: Output
PCLK I/O control	0x30B1[3]	Input/Output selection for the PCLK pad : 0: Input 1: Output
STROBE I/O control	0x30B1[4]	Input/Output selection for the STROBE pad : 0: Input 1: Output

2.4 system clock control

The OV3640 PLL allows for an input clock frequency ranging from 6~27 Mhz and has a maximum VCO frequency of 1.3 Ghz. SysClk is the input clock for the sensor core, SerClk is for the MIPI and DvpClk is for the internal clock of the Image Signal Processing (ISP) block. The PLL can be bypassed by setting register 0x300F[3] to 1.

2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6 power up sequence

Powering up the OV3640 sensor does not require a special power supply sequence. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up. Manually applying a hard reset upon power up is recommended even though the on-chip power-up reset is included.

2.7 reset

The OV3640 sensor includes a RESET_B pin that forces a complete hardware reset when it is pulled low (GND). The OV3640 clears all registers and resets them to their default values when a hardware reset occurs. A reset can also be initiated through the SCCB interface by setting register 0x3012[7] to high.

2.8 standby and sleep

Two suspend modes are available for the OV3640:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV3640 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

The OV3640 also supports MIPI ultra low power state (ULPS). After receiving ULPS command from host, the OV3640 will enter into ULPS mode. Except for the low speed part of the MIPI PHY and SCCB, all other blocks are enter into power down mode in ULPS mode.

3 block level description

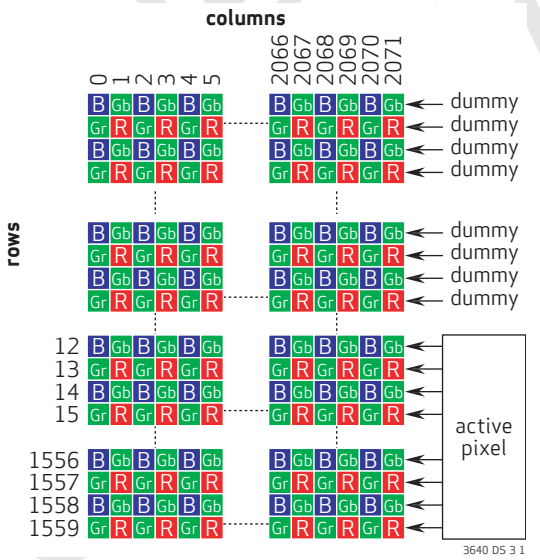
3.1 pixel array structure

The OV3640 sensor has an image array of 2072 columns by 1568 rows (3,248,896 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 3,248,896 pixels, 3,145,728 (2048x1536) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV3640 provides Mirror and Flip readout modes, which respectively reverse the sensor data readout order horizontally and veritically (see **figure 4-1**). In mirror, since the Bayer order changes from BGBG... to GBGB..., the OV3640 usually delays the readout sequence by one pixel by setting register 0x397C[1] to 1. In flip, the OV3640 does not need additional settings because the ISP block will auto-detect whether the pixel is in the red line or blue line and make necessary adjustment.

figure 4-1 mirror and flip samples

table 4-1 mirror and flip function control

function	register	description
mirror	0x307C[1]	Mirror ON/OFF select 0: Mirror OFF 1: Mirror ON
	0x3090[3]	Array mirror ON/OFF select 0: Array mirror OFF 1: Array mirror ON
flip	0x307C[0]	Flip ON/OFF select 0: Flip OFF 1: Flip ON
	0x3023	B/R row adjustment

4.2 image cropping

An image cropping area is defined by four parameters, HS(horizontal start), HW(horizontal width), VS(vertical start), VH(vertical height). By properly setting the parameters, any portion within the sense array size can be cropped as a visable area. This cropping is achieved by simply masking the pixels outside the cropping window; thus, it will not affect original timings. It will also not conflict with the flip and mirror functions.

figure 4-2 image cropping

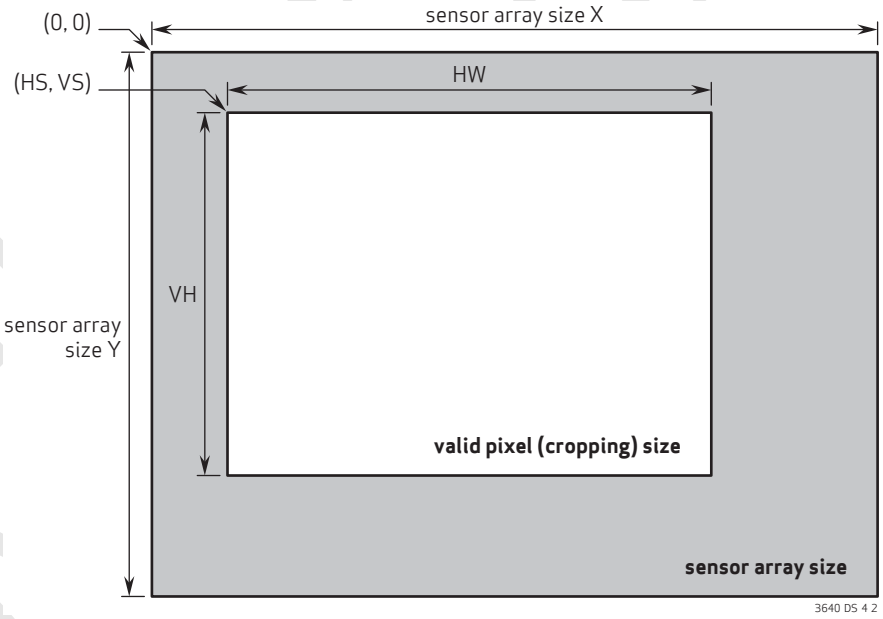


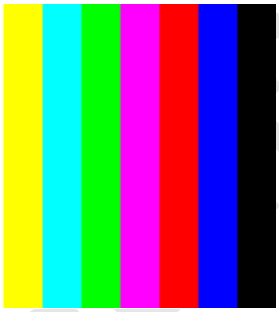
table 4-2 image cropping control functions

function	register	description
horizontal start	{0x3020, 0x3021}	HS[15:8] = 0x3020 HS[7:0] = 0x3021
vertical start	{0x3022, 0x3023}	VS[15:8] = 0x3022 VS[7:0] = 0x3023
horizontal width	{0x3024, 0x3025}	HW[15:8] = 0x3024 HW[7:0] = 0x3025
vertical height	{0x3026, 0x3027}	VH[15:8] = 0x3026 VH[7:0] = 0x3027

4.3 test pattern

For testing purposes, the OV3640 offers one type of test pattern, CBAR.

figure 4-3 test pattern



color bar

table 4-3 test pattern selection control

function	register	description
test pattern ON/OFF	0x3080[7]	Test pattern ON/OFF select 0: OFF 1: ON
color bar	0x307B[1:0]	color bar pattern select 10: Color bar pattern
	0x307D[7]	color bar enable 0: Color bar OFF 1: Color bar enable
	0x306C[4]	0: Color bar 1: Normal image

4.4 50/60hz detection

When the integration time is not an integer multiple of the period of light intensity, the image will flicker. The function of the detector is to detect whether the sensor is under a 50hz or 60hz light source so that the basic step of integration time can be determined.

4.5 AEC/AGC algorithms

4.5.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the CAMERACHIP sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-4**.

table 4-4 AEC/AGC control functions

function	register	description
AEC enable	0x3013[0]	Auto/manual exposure control select 0: Manual 1: Auto
AEC exposure time	{0x3002, 0x3003}	AEC[15:8] = 0x3000[15:8] AEC[7:0] = 0x3001[7:0]
AGC gain	{0x3000, 0x3001}	AGC[15:8] = 0x3002[9:8] AGC[7:0] = 0x3003[7:0]
AGC enable	0x3013[2]	Auto/manual gain control select 0: Manual 1: Auto
histogram / average-based selection	0x3047[7]	AEC/AGC method select 0: Average-based AEC/AGC 1: Histogram-based AEC/AGC

4.5.2 average-based algorithm

The Average-based AEC controls image luminance using registers 0x3018 (WPT/HisH) and 0x3019 (BPT/HisL). In average-based mode, the value of register 0x3018 (WPT/HisH) indicates the high threshold value and the value of register 0x3019 (BPT/HisL) indicates the low threshold value. When the target image luminance average value 0x301B (YAVG) is within the range specified by registers 0x3018 (WPT/HisH) and 0x3019 (BPT/HisL), the AEC keeps the image exposure. When register 0x301B (YAVG) is greater than the value in register 0x3018 (WPT/HisH), the AEC will decrease the image exposure. When register 0x301B (YAVG) is less than the value in register 0x3019 (BPT/HisL), the AEC will increase the image exposure. Accordingly, the value in register 0x3018 (WPT/HisH) should be greater than the value in register 0x3019 (BPT/HisL). The gap between the values of registers 0x3018 (WPT/HisH) and 0x3019 (BPT/HisL) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers 0x3018 (WPT/HisH) and 0x3019 (BPT/HisL). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. AEC set to fast mode will provide for an approximate ten-step increment or decrement in the image exposure to maintain the specified range. A value of "0" in register 0x3013[7] (Auto_1[7]) will result in normal speed operation and a "1" will result in fast speed operation.

Register 0x301A (VPT) controls the fast AEC range. If the target image 0x301B (YAVG) is greater than 0x301A[7:4] × 16, AEC will decrease by 2. If register 0x301B (YAVG) is less than 0x301A[3:0] × 16, AEC will increase by 2.

As shown in **figure 4-4**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

4.5.2.1 Outside Control Zone
Step Size: 2 × (AEC[15:0])

t_{STEP}: t_{ROW} × (2 × AEC[15:0])

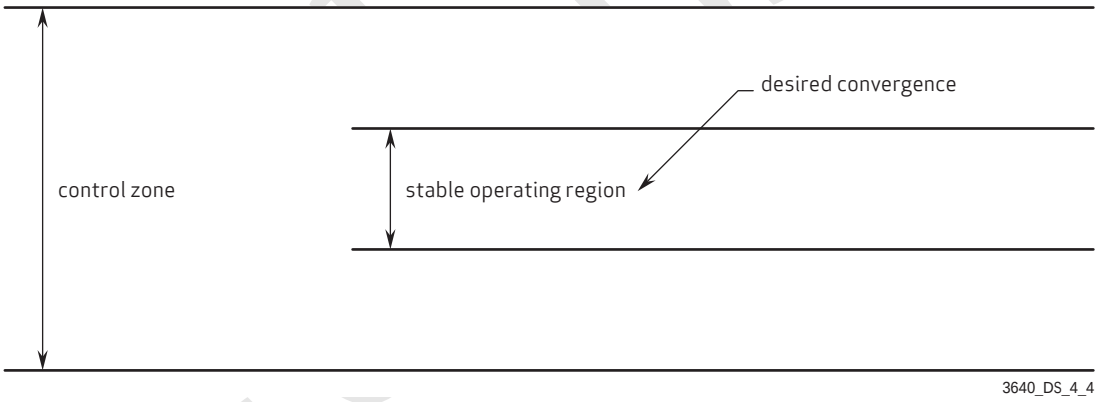
4.5.2.2 Inside Control Zone
Step Size: 2 × (AEC[15:0]) ÷ 16)

t_{STEP}: t_{ROW} × (2 × AEC[15:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

The Step Limit register acts to create a "middle ground" by limiting the maximum step size to 32 rows (delay time = t_{ROW} × 32).

figure 4-4 desired convergence



Control Zone Upper Limit: {VPT[7:4] (0x301A[7:4]), 4'b0000}

Control Zone Lower Limit: {VPT[3:0] (0x301A[3:0]), 4'b0000}

Stable Operating Region Upper Limit: WPT[7:0] (0x3018)

Stable Operating Region Lower Limit: BPT[7:0] (0x3019)

table 4-5 AEC control functions

function	register	description
WPT/HisH	0x3018	Luminance signal / histogram high range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance histogram is greater than WPT/HisH[7:0].
BPT/HisL	0x3019	Luminance signal / histogram low range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance histogram is less than BPT/HisL[7:0].
VPT	0x301A	Fast mode large step range thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0].
YAVG	0x301B	Luminance average - this register will auto update. Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) x 0.25
fast AEC enble	0x3013[7]	AEC speed select 0: Average-based AEC/AGC 1: Histogram-based AEC/AGC

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided by sixteen (4x4) zones (see **figure 4-5**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.5.2.3,** average luminance (YAVG).

4.5.2.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting AHS,AVS, AHW, and AVH as shown in **figure 4-5**, a 4x4 grid average window is defined. The average value is the weighted average of the 16 sections. **table 4-6** lists the corresponding registers.

figure 4-5 average-based window defininition

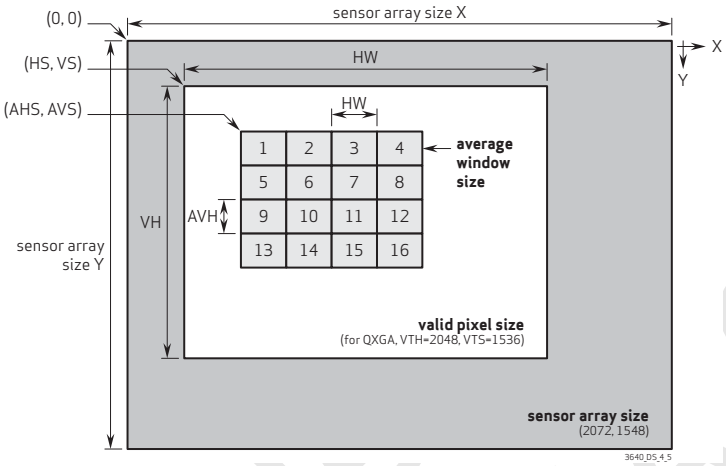


table 4-6 average-based algorithm functions

function	register	description
horizontal starting pixel (AHS)	{0x3038, 0x3039}	AHS[11:8] = 0x3038[3:0] AHS[7:0] = 0x3039[7:0]
vertical starting pixel (AVS)	{0x303A, 0x303B}	AVS[10:8] = 0x303A[2:0] AVS[7:0] = 0x303B[7:0]
average section width (AHW)	{0x303C, 0x303D}	AHW[11:8] = 0x303C[3:0] AHW[7:0] = 0x303D[7:0]
average section height (AVH)	{0x303E, 0x303F}	AVH[11:8] = 0x303E[3:0] AVH[7:0] = 0x303F[7:0]
average section weighting	0x3030~0x3037	Section 1 weight = 0x3030[3:0] Section 2 weight = 0x3030[7:4] Section 3 weight = 0x3031[3:0] Section 4 weight = 0x3031[7:4] Section 5 weight = 0x3032[3:0] Section 6 weight = 0x3032[7:4] Section 7 weight = 0x3033[3:0] Section 8 weight = 0x3033[7:4] Section 9 weight = 0x3034[3:0] Section 10 weight = 0x3034[7:4] Section 11 weight = 0x3035[3:0] Section 12 weight = 0x3035[7:4] Section 13 weight = 0x3036[3:0] Section 14 weight = 0x3036[7:4] Section 15 weight = 0x3037[3:0] Section 16 weight = 0x3037[7:4]

4.5.3 histogram-based algorithm

The OV3640 histogram-based AEC controls exposure levels based on image histogram distribution and probability.

table 4-7 histogram-based AEC registers

function	register	description
WPT/HisH[7:0] - HRL	0x3018	Luminance signal / histogram high range for AEC/AGC operation AEC/AGC value decreases in auto mode when average luminance histogram is greater than WPT/HisH[7:0].
BPT/HisL[7:0] - LRL	0x3019	Luminance signal / histogram low range for AEC/AGC operation AEC/AGC value increases in auto mode when average luminance histogram is less than BPT/HisL[7:0].
HISTO0 - LPH	0x3040	Lower limit of probability for HRL after exposure/gain stabilizes
HISTO1 - UPL	0x3041	Upper limit of probability for LRL after exposure/gain stabilizes
HISTO2 = TPL	0x3042	Probability threshold for LRL to control AEC/AGC speed
HISTO3 - TPH	0x3043	Probability threshold for HRL to control AEC/AGC speed
HISTO4[7:4] - TLH	0x3044[7:4]	High nibble of luminance threshold for AEC/AGC speed control
HISTO4[3:0] - TLL	0x3044[3:0]	Low nibble of luminance threshold for AEC/AGC speed control

figure 4-6 average-based window definition

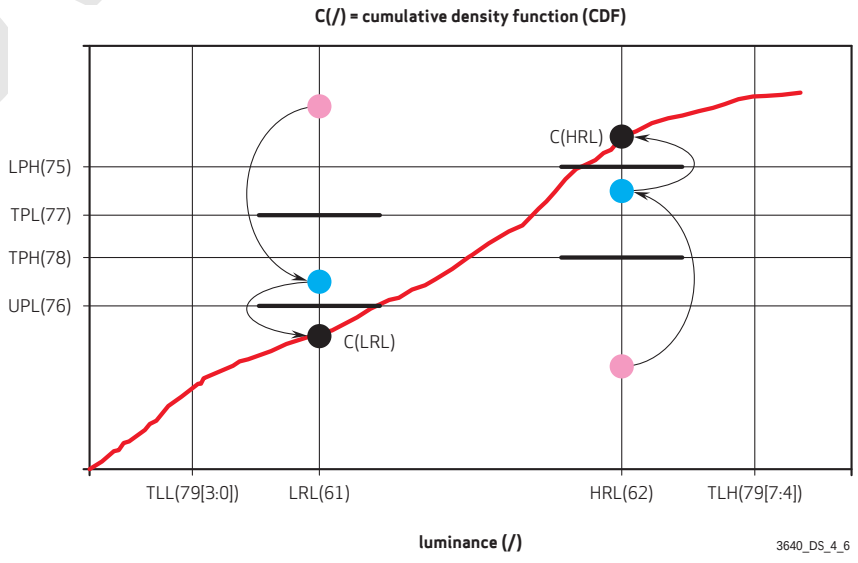


table 4-8 histogram-based AEC algorithm adjustment controls

control	selection	registers
luminance saturation control	more saturated	Decrease both LPH (0x3040) and UPL (0x3041)
	less saturated	Increase both LPH (0x3040) and UPL (0x3041)
image brightness control	brighter image	Increase both LRL (0x3019) and HRL (0x3018)
	darker image	Decrease both LRL (0x3019) and HRL (0x3018)
AEC speed control	higher speed	Decrease TLH (0x3044[7;4]) but not less than target image luminance and increase TLL (0x3044[3:0] but not more than target luminance.
	lower speed	TLH (0x3044[7:4]) should be more than 1.2 × target image luminance and TLL (0x3044[3:0] should be less than 0.8 × target image luminance.
AEC speed controlled by TPL and TPH	higher speed	Decrease TPL (0x3042) but not less than UPL (0x3041) and increase TPH (0x3043) but not bigger than LPH (0x3040).
	lower speed	Increase REG77 (0x3042) and decrease REG78 (0x3043).
AEC flickering versus LRL and HRL		HRL (0x3018) should be larger than LRL (0x3019). The recommended relationship between these two values in order to prevent flickering is shown below: HRL > 1.07 × LRL
AEC flickering versus LPH and UPL		LPL should be larger than UPL. If the difference (LPH - UPL) is big, AEC flickering can occur. The recommended relationship between these two values is shown below: LPH < 1.07 × UPL

4.5.3.1 histogram calculation control (FAVG)

The histogram calculator will output the ratio of pixels that are lower than histogram upper threshold and higher than the lower threshold. The estimated range of image is defined vertically by line_valid.

The user can adjust the reference area vertically from the image that will be used by the histogram-based AEC/AGC algorithm.

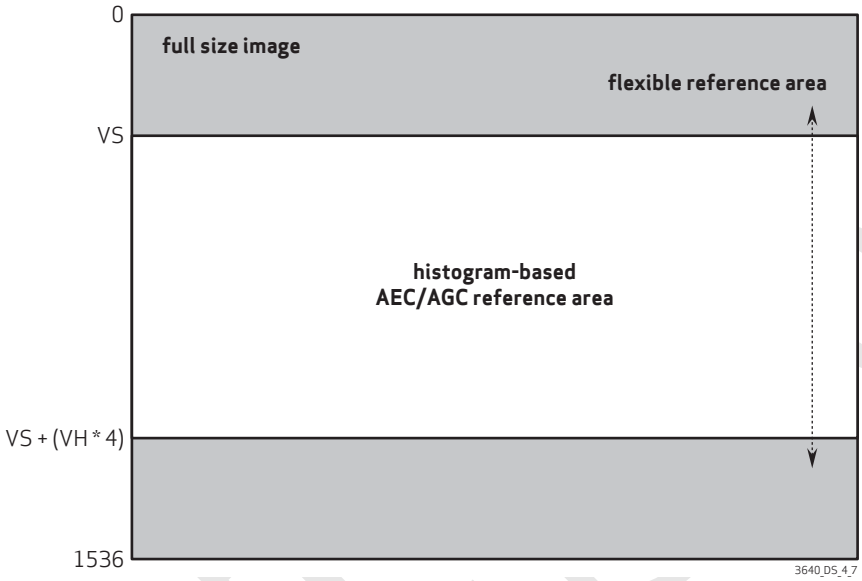
table 4-9 histogram calculation control

function	register	description
line_valid	{0x3022, 0x3023} {0x3026, 0x3027}	Vertical valid pixels sindow defined by VS and VH
histo_high	0x3018	Histogram upper threshold
histo_low	0x3019	Histogram lower threshold
aver_opt[1:0]	0x307D[3:2]	Saturated threshold selection
exc_255	0x307D[4]	Image histogram is calculated from non-saturated pixels when exc_255 is set high; otherwise, it is calculated from all pixels.
sys_rst	0x30AF[0]	Set high to disable image histogram calculation

table 4-10 histogram-based AEC/AGC reference area option

function	register	description
vertical starting pixel (AVS)	{0x303A, 0x303B}	AVS[10:8] = 0x303A[2:0] AVS[7:0] = 0x303B[7:0]
average section height (AVH)	{0x303E, 0x303F}	AVH[11:8] = 0x303E[3:0] AVH[7:0] = 0x303F[7:0]

figure 4-7 histogram-based AEC/AGC reference areas



4.6 AEC/AGC steps

The AEC and AGC work together to obtain adequate exposure/gain based on the current environmental illumination. In order to achieve the best SNR, extending the exposure time is always prefered than raising the analog gain when the current illumination is going brighter. Vice versa, under dark condition, the action to decrease the gain is always taken prior to shorten the exposure time.

4.6.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remian the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall in some bands.

4.6.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to the minimal of 1/16 row or so. LAEC On/Off can be set in 0x3013.

4.6.1.2 banding mode ON with AEC

In Banding ON mode, AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. This design is to reject image flickering when light source is not steady but periodical.

For a given operating frequency, band step can be expressed in terms of row timing.

Band Step = 'period of light intensity' x 'frame rate' x 'rows per frame'.

The band steps for 50hz and 60hz light sources can be set in 0x3070~0x3071 and 0x3072~0x3073, respectively.

When auto-banding is ON, if the next intergration time is less than the minimal band step, banding will automatically turn OFF. It will turn ON again until the next integration time becomes larger than minimal band. If auto-banding is disabled, the minimal integration time is one minimal band. Auto-banding can be set in 0x3013[4].

4.6.1.3 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.6.1.4 VAEC

In extremely dark situation, the intergration time needs to be longer than one frame.

OV3640 supports long integration time such as 2 frame, 3 frame, 4 frame and 8 frame. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in 0x3015. VAEC can be disable by setting 0x3014 to 0.

4.6.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise or between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases that adjacent AEC step changes are too large(>1/16), AGC step should be inserted in between. Otherwise, the integration time will keep switching from two adjacent step and the image flickers.

4.6.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC step is larger than 1/16, which possibly make the image occilates between two AEC levels. Thus, some AGC steps are added in between. For example, from AEC = 2 row to AEC = 3 rows, there are 7 more AGC steps(1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.6.2.2 gain insertion between AEC banding steps

In Banding ON mode, the minimal integration time change is the period of light intesity(10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band step, since the change between adjacent step is larger than 1/16, AGC steps are inserted to ensure image stability.

4.6.2.3 gain insertion between VAEC steps

Between VAEC steps, eg. Integration time = 1 frame and 2 frames, AGC steps are inserted to ensure no adjacent step change is larger than 1/16(6.25%).

4.6.2.4 when AEC reaches maximum

When AEC reaches its maximal step while the image is still too dark, AGC step starts to increase until new frame average falls into the no-adjust region or AGC reaches its maximal step. AGC step maximum can be set in 0x3015..

table 4-11 histogram-based AEC/AGC reference area option

function	register	description
LAEC ON/OFF	0x3014[1]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x3013[5]	Banding ON/OFF select 0: OFF 1: ON
VAEC ON/OFF	0x3014[3]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x3013[4]	Auto banding ON/OFF select 0:OFF 1:ON
max integration time	0x3015[6:4]	VAEC ceiling 000: 1 frame 001: 2 frames 010: 3 frames 011: 4 frames 1xx: 8 frames
max_band_50hz	0x301C[5:0]	Max banding for 50Hz in terms of row exposure.
max_band_60hz	0x301D[5:0]	Max banding for 60Hz in terms of row exposure.
banding step for 50Hz	{0x3070, 0x3071}	BD50st[9:8] = 0x3070[1:0] BD50st[7:0] = 0x3071[7:0]
banding step for 60Hz	{0x3072, 0x3073}	BD60st[9:8] = 0x3072[1:0] BD60st[7:0] = 0x3073[7:0]

4.7 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used to provide the data for black level calibration.

Black level adjustments can be made with registers 0x3069 through 0x306F.

table 4-12 BLC control functions

function	register	description
target	0x3069[3:0]	Target black level value that is used in the algorithm.
MBLC	0x306E[1]	When set, triggers BLC manually for 32 frames.
BLCX2	0x307C[2]	When set, BLC will be triggered when the gain is changing (high gain).

4.8 digital gain

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-13 digital gain control functions

function	register	description
digital gain enable	0x307C[5]	Digital gain enable 0: Disable 1: Enable
digital gain select	0x307E[7:6]	Range of digital gain 00: Apply digital gain only if gain ≥ 2x 01: Apply digital gain only if gain ≥ 4x 1x: Apply digital gain only if gain ≥ 8x

4.9 strobe flash control

To achieve the best image quality possible in low light conditions, the use of a strobe flash is recommended. The OV3640 provides a programmable strobe signal function.

4.9.1 sensor-controlled strobe flash

The OV3640 can generate a programmable strobe signal from the Strobe pad (pad 04). **table 4-14** lists the strobe pulse control registers.

table 4-14 strobe control functions

function	register	description
strobe function enable	0x307A[7]	Strobe function enable 0: Strobe disable 1: Start strobe enable
strobe output pulse polarity control	R0x307A[6] (TMC4[6])	Strobe output polarity control 0: Positive pulse 1: Negative pulse
xenon mode strobe pulse width	R0x307A[3:2] (TMC4[3:2])	Xenon mode pulse width 00: 1 line 01: 2 lines 10: 3 lines 11: 4 lines
strobe mode	R0x307A[1:0] (TMC4[1:0])	Strobe mode select 00: Xenon mode 01: LED 1 & 2 mode 10: LED 1 & 2 mode 11: LED 3 mode

4.9.1.1 strobe pulse

The strobe signal is programmable. It supports both LED and Xenon mode. The polarity of the pulse can be changed. The strobe signal is enabled (turned high / low depending on the pulse's polarity) by requesting the signal via the SCCB. Flash modules are typically triggered to the rising edge (falling edge, if signal polarity is changed). It supports the flashlight modes shown in **table 4-15**.

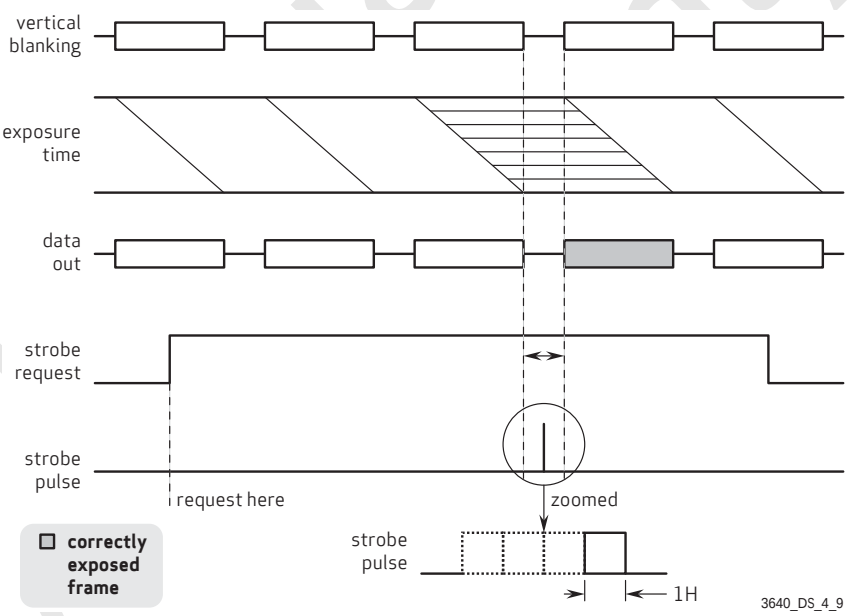
table 4-15 flashlight modes

function	register	description
xenon	one pulse	no
LED 1	pulse	no
LED 2	pulse	no
LED 3	continuous	yes

4.9.1.2 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see figure 4-8). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H, where H is one horizontal period ([1 / fps] x [1 / number of total lines] sec).

figure 4-8 xenon flash mode



4.9.1.3 LED 1 & 2 mode

Two frames after the strobe request is submitted, the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set correctly (see figure 4-9). If end request is not sent, the strobe signal is activated intermittently until the strobe end request is set (see figure 4-10). The number of skipped frames is programmable.

figure 4-9 LED 1 & 2 mode - one pulse output

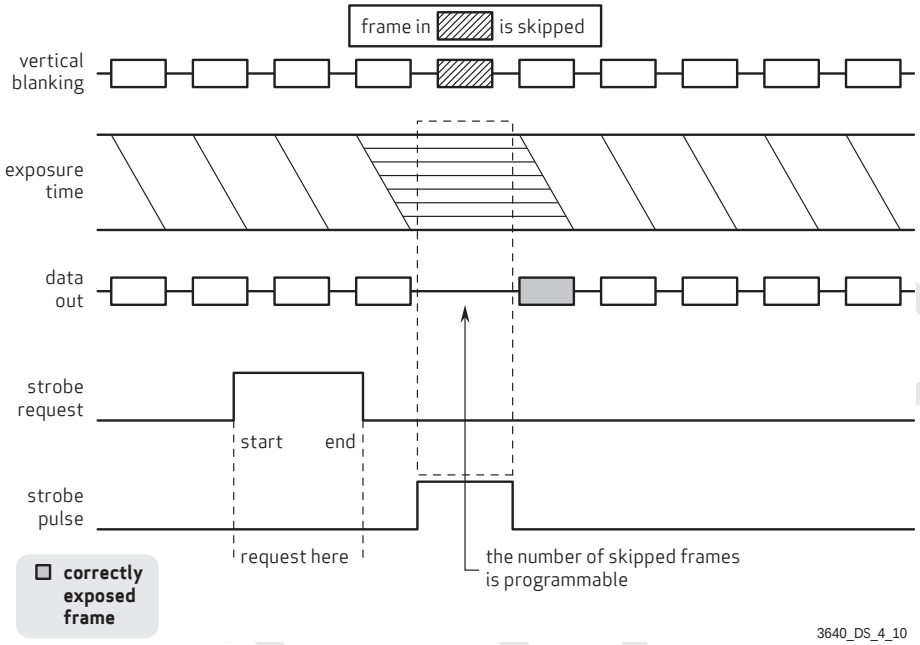
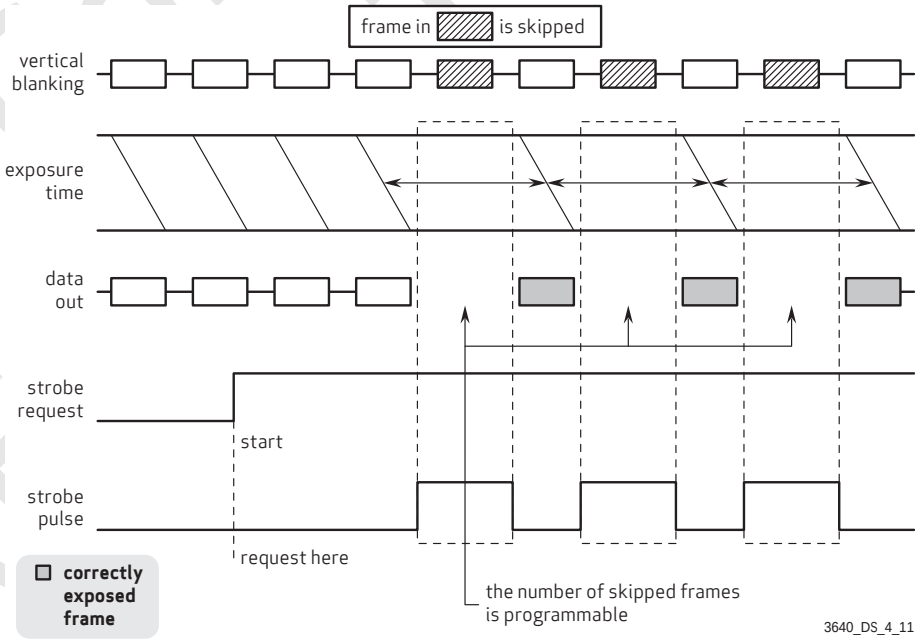


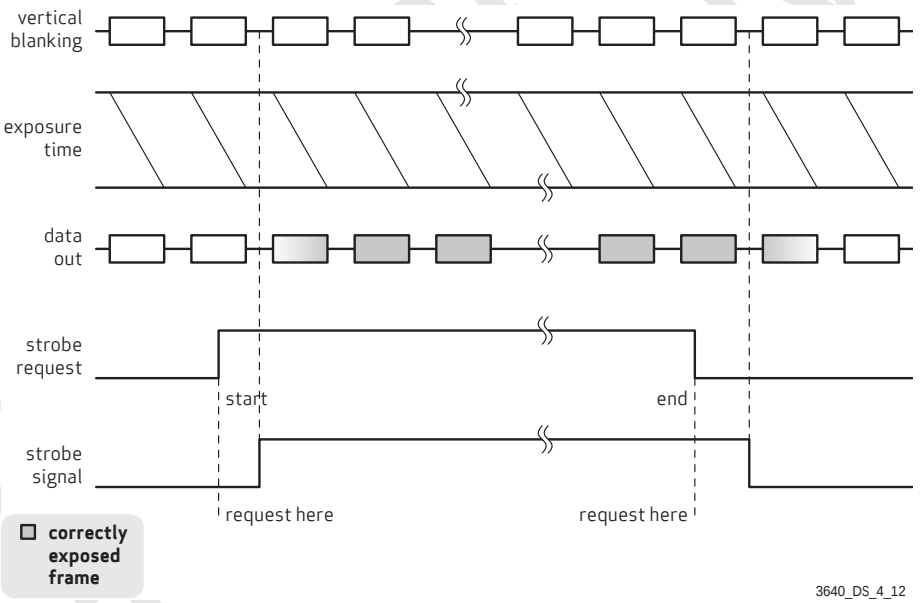
figure 4-10 LED 1 & 2 mode - multiple pulse output



4.9.1.4 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see figure 4-11).

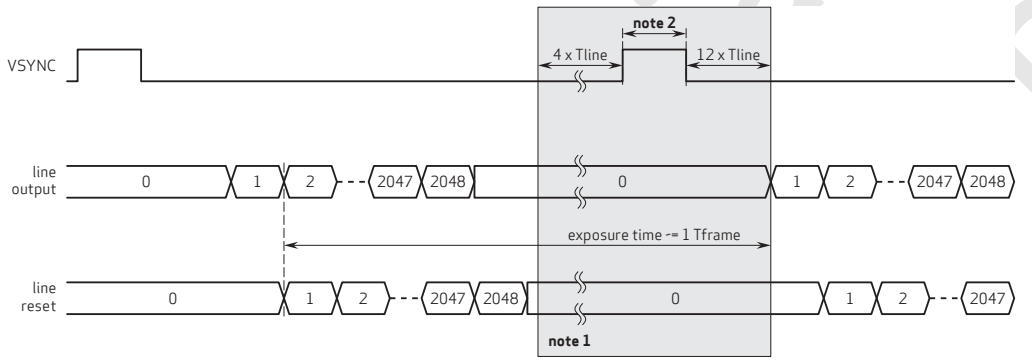
figure 4-11 LED 3 mode



4.9.2 external processor controlled

In the case where Strobe Flash is controlled by an external processor to avoid the need for a mechanical shutter, the OV3640 should be set to rolling shutter mode. When rolling shutter mode is enabled and the image requires strobe flash illumination, the strobe timing must be limited. Timing diagrams for strobe flash timing are shown in **figure 4-12** and **figure 4-12**.

figure 4-12 QXGA strobe flash timing diagram

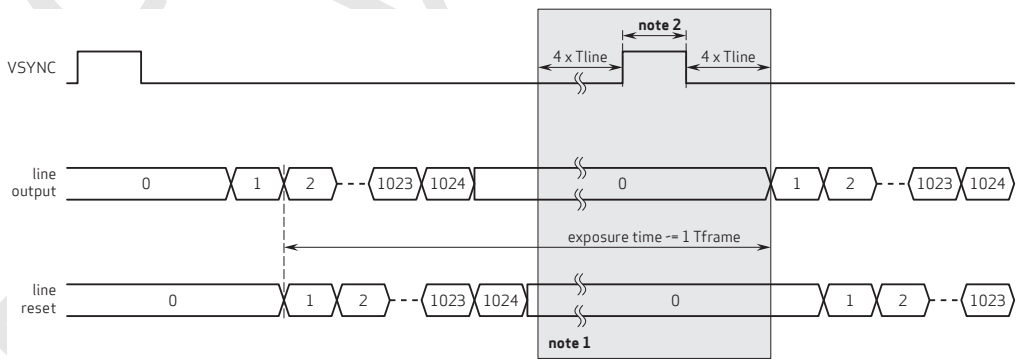


note 1 if using live video mode for still capture and if flash is required, use maximum exposure (1 frame) and turn on flash only between this gray period.

note 2 strobe width is controlled by register 0x307A[3:2] where:
00: 1 Tline
01: 2 Tlines
10: 3 Tlines
11: 4 Tlines
default strobe signal width is 1 Tline

3640_DS_4_13

figure 4-13 XGA strobe flash timing diagram



note 1 if using live video mode for still capture and if flash is required, use maximum exposure (1 frame) and turn on flash only between this gray period.

note 2 strobe width is controlled by register 0x307A[3:2] where:
00: 1 Tline
01: 2 Tlines
10: 3 Tlines
11: 4 Tlines
default strobe signal width is 1 Tline

3640_DS_4_14

4.10 one time programmable (OTP) memory

The OV3640 supports 128 bits maximum one-time programmable (OTP) memory to store chip identification and manufacturing information. Contact your local OmniVision FAE for more details.

5 image sensor processor digital functions

5.1 lens correction (LENC)

The main purpose of the LENC function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-1 LENC-related registers (sheet 1 of 4)

register address	register name	function
0x3300	DSP_CTRL_0	DSP Control 0 Bit[0]: LENC enable - corrects light variations introduced by the lens. 0: Disable 1: Enable
0x3304	DSP_CTRL4	DSP Control 4 Bit[3]: LENC_bias_ON - enables/disables the bias valid/invalid for the LENC function. 0: Disable LENC bias function 1: Enable LENC bias function Bit[2]: LENC_bias_plus - enables/disables the bias added to the LENC result. 0: Do not add bias to the LENC result 1: Add bias to the LENC result
0x3366	LENC_CTRL_0	LENC Control 0 Bit[7:6]: SOF_selection 00: VSYNC_in 01: CIP_SOF 10: DCW_SOF 11: Not used Bit[4]: RND_en - determines whether or not to round off the last two bits of the LENC input data. 0: Do not round off the last 2 bits 1: Round off the last 2 bits Bit[3:2]: V_skip - valid only when the image size is not the full size. 00: Does not skip a line 01: Skips 1 line every 2 lines 10: Skips 3 lines every 4 lines 11: Skips 7 iines every 8 lines Bit[1:0]: H_skip - valid only when the image size is not the full size. 00: Does not skip a pixel 01: Skips 1 pixel every 2 pixels 10: Skips 3 pixels every 4 pixels 11: Skips 7 pixels every 8 pixels

table 5-1 LENC-related registers (sheet 2 of 4)

register address	register name	function
0x3367	R_XY0	R_XY0 Bit[6:4]: R_Y0[10:8] (used with 0x3369[7:0]) - R_Y0 is the vertical center position in red color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047. Bit[2:0]: R_X0[10:8] (used with 0x3368[7:0]) - R_X0 is the horizontal center position in red color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x3368	R_X0	R_X0 Bit[7:0]: R_X0[7:0] (used with 0x3367[2:0]) - R_X0 is the horizontal center position in red color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x3369	R_Y0	R_Y0 Bit[7:0]: R_Y0[7:0] (used with 0x3367[6:4]) - R_Y0 is the vertical center position in red color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047.
0x336A	R_A1	R_A1 Bit[7:0]: R_A1 - composed of the first group of factors used in the LENC correction of the red color channels.
0x336B	R_A2/B2	R_A2/B2 Bit[7:4]: R_B2 - composed of the second group of factors used in the LENC correction of the red color channels. Bit[3:0]: R_A2 - composed of the first group of factors used in the LENC correction of the red color channels.
0x336C	R_B1	R_B1 Bit[7:0]: R_B1 - composed of the second group of factors used in the LENC correction of the red color channels.

table 5-1 LENC-related registers (sheet 3 of 4)

register address	register name	function
0x336D	G_XY0	G_XY0 Bit[6:4]: G_Y0[10:8] (used with 0x336F[7:0]) - G_Y0 is the vertical center position in green color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047. Bit[2:0]: G_X0[10:8] (used with 0x336E[7:0]) - G_X0 is the horizontal center position in green color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x336E	G_X0	G_X0 Bit[7:0]: G_X0[7:0] (used with 0x336D[2:0]) - G_X0 is the horizontal center position in green color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x336F	G_Y0	G_Y0 Bit[7:0]: G_Y0[7:0] (used with 0x336D[6:4]) - G_Y0 is the vertical center position in green color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047.
0x3370	G_A1	G_A1 Bit[7:0]: G_A1 - composed of the first group of factors used in the LENC correction of the green color channels.
0x3371	G_A2/B2	G_A2/B2 Bit[7:4]: G_B2 - composed of the second group of factors used in the LENC correction of the green color channels. Bit[3:0]: G_A2 - composed of the first group of factors used in the LENC correction of the green color channels.
0x3372	G_B1	G_B1 Bit[7:0]: G_B1 - composed of the second group of factors used in the LENC correction of the green color channels.

table 5-1 LENC-related registers (sheet 4 of 4)

register address	register name	function
0x3373	B_XY0	B_XY0 Bit[6:4]: B_Y0[10:8] (used with 0x3375[7:0]) - B_Y0 is the vertical center position in blue color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047. Bit[2:0]: B_X0[10:8] (used with 0x3374[7:0]) - B_X0 is the horizontal center position in blue color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x3374	B_X0	B_X0 Bit[7:0]: B_X0[7:0] (used with 0x3373[2:0]) - B_X0 is the horizontal center position in blue color channels. It should be fixed as the horizontal position of the image which comes from the middle of the lens. So, it is usually set as the horizontal position of the middle pixel of each image. Range is 0~2047.
0x3375	B_Y0	B_Y0 Bit[7:0]: B_Y0[7:0] (used with 0x3373[6:4]) - B_Y0 is the vertical center position in blue color channels. It should be fixed as the vertical position of the image which comes from the middle of the lens. So, it is usually set as the vertical position of the middle pixel of each image. Range is 0~2047.
0x3376	B_A1	B_A1 Bit[7:0]: B_A1 - composed of the first group of factors used in the LENC correction of the blue color channels.
0x3377	B_A2/B2	B_A2/B2 Bit[7:4]: B_B2 - composed of the second group of factors used in the LENC correction of the blue color channels. Bit[3:0]: B_A2 - composed of the first group of factors used in the LENC correction of the blue color channels.
0x3378	B_B1	B_B1 Bit[7:0]: B_B1 - composed of the second group of factors used in the LENC correction of the blue color channels.

5.2 auto white balance (AWB)

The main purpose of the Auto White Balance (AWB) function is to automatically correct the white balance of the image. It supports manual white balance, simple AWB and advanced AWB. For advanced AWB settings, contact your local OmniVision FAE.

table 5-2 AWB-related registers

register address	register name	function
0x3302	DSP_CTRL_2	DSP Control 2 Bit[1]: AWB_gain_en - adjusts the image gain according to the auto white balance function result. Bit[0]: AWB_en - The AWB function judges the image color temperature and decides how to balance the white color.
0x3308	AWB_CTRL_3	AWB Control 3 Bit[7]: AWB_simple - in many cases, the advanced mode is a better selection. 0: AWB advanced mode 1: AWB simple mode
0x332B	MISC_CTRL	MISC_CTRL Bit[3]: AWB_gain_man 0: Auto mode - AWB gain uses R/G/B channel gain calculated by AWB. 1: Manual mode - AWB_gain uses R/G/B channel gain is set manually. Refer to registers 0x33A7, 0x33A8, and 0x33A9 for AWB gain manual setting.
0x33A7	R_GAIN_M	R_GAIN_M Bit[7:0]: AWB R manual gain Range is 0~255
0x33A8	G_GAIN_M	G_GAIN_M Bit[7:0]: AWB G manual gain Range is 0~255
0x33A9	B_GAIN_M	B_GAIN_M Bit[7:0]: AWB B manual gain Range is 0~255

5.3 gamma curve (GMA)

The main purpose of the Gamma (GMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions.

table 5-3 GMA-related registers

register address	register name	function
0x3302	DSP_CTRL_2	DSP Control 2 Bit[2]: GMA_en - converts the image luminance according to the Gamma curve to compensate the image under different light strengths.
0x3304	DSP_CTRL4	DSP Control 4 Bit[5]: GMA_bias_on - enables/disables the bias valid/invalid for the Gamma function. 0: Disable Gamma bias function 1: Enable Gamma bias function Bit[4]: GMA_bias_plus - enables/disables the bias added to the Gamma result. 0: Do not add bias to the Gamma result 1: Add bias to the Gamma result
0x331B	YST1	YST1[7:0]
0x331C	YST2	YST2[7:0]
0x331D	YST3	YST3[7:0]
0x331E	YST4	YST4[7:0]
0x331F	YST5	YST5[7:0]
0x3320	YST6	YST6[7:0]
0x3321	YST7	YST7[7:0]
0x3322	YST8	YST8[7:0]
0x3323	YST9	YST9[7:0]
0x3324	YST10	YST10[7:0]
0x3325	YST11	YST11[7:0]
0x3326	YST12	YST12[7:0]
0x3327	YST13	YST13[7:0]
0x3328	YST14	YST14[7:0]
0x3329	YST15	YST15[7:0]
0x332A	YSLP15	YSLP15[7:0]

5.4 white black pixel cancellation (WBC)

The main purpose of White/Black pixel Cancellation (WBC) function is to remove the white/black pixels effect.

table 5-4 WBC-related registers

register address	register name	function
0x3301	DSP_CTRL_2	DSP Control 1 Bit[2]: WC_en This function removes the white pixels introduced by the sensor's defects. Bit[1]: BC_en This function removes the black pixels introduced by the sensor's defects.

5.5 interpolation/de-noise/edge enhancement (CIP)

The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge ehancement. CIP functions work in both manual and auto modes.

table 5-5 CIP-related registers (sheet 1 of 2)

register address	register name	function
0x3302	DSP_CTRL_2	DSP Control 2 Bit[3]: CIP_en The color interpolation function can transfer the image from RAW to RGB domain. The de-noise function is also integrated in the CIP function. Refer to CIP-related registers for de-noise settings.
0x332C	DNS_TH	DNS_TH Bit[7:0]: DNS_TH The bigger this value is, the stronger the de-noise effect will be. This register is valid only when the de-noise function is set to manual mode (0x332D[6] = 0).

table 5-5 CIP-related registers (sheet 2 of 2)

register address	register name	function
0x332D	Y_EDGE_MT	Y_EDGE_MT Bit[6]: De-noise auto mode 0: Manual mode - in manual mode, the de-noise threshold is set manually in register 0x332C[7:0]. 1: Auto mode - in auto mode, the de-noise threshold is calculated automatically. The calculated de-noise threshold range is 0~255. Bit[5]: Edge enhancement auto mode 0: Manual mode - in manual mode, the edge enhancement threshold is set manually in register 0x332D[4:0]. 1: Auto mode - in auto mode, the edge enhancement threshold is calculated automatically. The calculated edge enhancement threshold range is 0~31. Bit[4:0]: Edge enhancement threshold manual setting The bigger this value is, the sharper the image edges are.
0x332E	Y_EDGE_TH	Y_EDGE_TH Bit[3:0]: Y_edge_TH The strength factor for the sharpen function but its usage is negative with Y_edge_MT. If the value is smaller, the edge of the image will become sharper. Range is 0~9.
0x332F	BASE1	BASE1 Bit[4:0]: Base1 These register bits are effective when the edge enhancement threshold is calculated automatically. The bigger this value is, the sharper the image. This register is valid only in auto mode (0x332D[5] = 1). Range is 0~31.
0x3330	BASE2	BASE2 Bit[4:0]: Base2 These register bits are effective when the edge enhancement threshold is calculated automatically. The bigger this value is, the less sharp the image. This register is valid only in auto mode (0x332D[5] = 1). Range is 0~31.
0x3331	OFFSET	De-noise Offset Bit[7:0]: Offset This register is effective when the de-noise threshold is calculated automatically. It actually behaves as the bias. The bigger this value is, the bigger the de-noise threshold. This register is valid only in auto mode (0x332D[6] = 1)

5.6 color matrix (CMX)

The main purpose of the Color Matrix (CMX) function is to convert images from the RGB domain to YUV domain. For different color temperatures, the parameters in the transmitting function will be changed.

table 5-6 CMX-related registers

register address	register name	function
0x3301	DSP_CTRL1	DSP Control 1 Bit[4]: CMX_En Color matrix function enable. CMX will transfer image from RGB to YUV domain.
0x333F	CMXSIGN_MISC	CMXSIGN_MISC Bit[5]: CMX input switch 0: CMX input comes from CIP 1: CMX input comes from Gamma Bit[3]: CMX precision switch 0: 1.7 mode 1: 2.6 mode Bit[1]: CMXSIGN[8] for CMX (used with 0x3349[7:0])
0x3340	CMX_1	CMX1[7:0]
0x3341	CMX_2	CMX2[7:0]
0x3342	CMX_3	CMX3[7:0]
0x3343	CMX_4	CMX4[7:0]
0x3344	CMX_5	CMX5[7:0]
0x3345	CMX_6	CMX6[7:0]
0x3346	CMX_7	CMX7[7:0]
0x3347	CMX_8	CMX8[7:0]
0x3348	CMX_9	CMX9[7:0]
0x3349	CMXSIGN	CMXSIGN[7:0]
0x3379	BLC_CTRL	BLC Control Bit[5:4]: CMX_bias_manu Valid only when 0x3304[7] = 1 00: From AWB_bias[7:0] input 01: From CMX off_manual[7:0] (0x337C[7:0]) 10: From BLC_manu_BL[7:0] (0x3399[7:0]) 11: From sensor_bias[7:0]
0x337C	CMX_OFF_M	CMX_OFF_M Bit[7:0]: CMX_OFF_M

5.7 zoom out (ZOOM)

The main purpose of the Zoom out (ZOOM) function is to zoom out the image. According to the new_width and new_height of the new image, the module uses several pixels' values to generate one pixel's value. Some pixels' values are divided and used in two or more adjacent pixels. Calculating the algorithm uses finite float point to keep the mantissa when using this function.

table 5-7 ZOOM-related registers

register address	register name	function
0x3302	DSP_CTRL_2	DSP Control 2 Bit[5]: Scale_En This function allows the user to zoom out the image from full size.
0x335F	SIZE_IN_MISC	SIZE_IN_MISC Bit[6:4]: Vsize_In[10:8] (used with 0x3361[7:0]) Bit[3:0]: Hsize_In[11:8] (used with 0x3362[7:0])
0x3360	HSIZE_IN_L	HSIZE_IN_L Bit[7:0]: Hsize_In[7:0] (used with 0x335F[3:0])
0x3361	VSIZE_IN_L	VSIZE_IN_L Bit[7:0]: Vsize_In[7:0] (used with 0x335F[6:4])
0x3362	SIZE_OUT_MISC	SIZE_OUT_MISC Bit[6:4]: Vsize_Out[10:8] (used with 0x3364[7:0]) Vsize_Out must be smaller than Vsize_In in 0x335F and 0x3361 due to zoom out function limit. Bit[3:0]: Hsize_Out[11:8] (used with 0x3363[7:0]) Hsize_Out must be smaller than Hsize_In in 0x335F and 0x3360 due to zoom out function limit.
0x3363	HSIZE_OUT_L	HSIZE_OUT_L Bit[7:0]: Hsize_Out[7:0] for zoom out Zoom out output horizontal size low 8-bits in hex (used with 0x3362[3:0])
0x3364	VSIZE_OUT_L	VSIZE_OUT_L Bit[7:0]: Vsize_Out[7:0] for zoom out Zoom out output vertical size low 8-bits in hex (used with 0x3362[6:4])

5.8 special digital effects (SDE)

The Special Digital Effects (SDE) functions include hue/saturation control, brightness, contrast, etc. Use SDE_CTRL to add some special effects to the image. Calculate the new U and V from Hue Cos, Hue Sin, and parameter signs. Saturate U and V using the Sat_u and Sat_v; registers. Calculate Y using Y offset, Y gain, and Ybright or set the Y value. SDE supports negative, black/white, sepia, greenish, blueish, redish and other image effects which combine the effects already listed.

table 5-8 SDE-related registers

register address	register name	function
0x3302	DSP_CTRL2	DSP Control 2 Bit[7]: SDE_En - special DSP effects function can process images by adjusting hue/saturation/fixed YUV, etc.
0x3354	SGNSET	SGNSET Bit[7]: WG_Swap 0: GMA to WBC 1: WBC to GMA Bit[6]: Y_Avg_Mode 0: Y_Avg for SDE Y saturation comes from sensor. 1: Y_Avg for SDE Y saturation comes from register 0x335C[7:0] Bit[5:0]: Sign set for hue adjusting in SDE function. For each bit: Hue: Bit[5:4], Bit[1:0] U' = SGNST[5] (HueCos/0x80) × U + SGNSET[1] (HueSin/0x80) × V V' = SGNST[4] (HueCos/0x80) × U + SGNSET[0] (HueSin/0x80) × U YContrast: sign2: YOFFSET sign3: YBRIGHT
0x3355	SDE_CTRL	SDE CTRL[7:0]
0x3356	HUE_COS	HUE_COS[7:0]
0x3357	HUE_SIN	HUE_SIN[7:0]
0x3358	SAT_U	SAT_U[7:0]
0x3359	SAT_V	SAT_V[7:0]
0x335A	UREG	UREG[7:0]
0x335B	VREG	VREG[7:0]
0x335C	YOFFSET	YOFFSET[7:0]
0x335D	YGAIN	YGAIN[7:0]
0x335E	YBRIGHT	YBRIGHT[7:0]

5.9 overlay

The OV3640 supports an overlay function.

table 5-9 overlay-related registers

register address	register name	function
0x3300	DSP_CTRL_0	DSP Control 0 Bit[6]: OVLY_En The overlay function can draw a frame according to a coordinate user set.
0x33AA	OVLY_MISC1	OVLY_MISC1 Bit[6:4]: OVLY_Top[10:8] (used with 0x33AC[7:0]) Bit[3:0]: OVLY_Left[11:8] (used with 0x33AB[7:0])
0x33AB	OVLY_LEFT	OVLY_LEFT Bit[7:0]: OVLY_Left[7:0] (used with 0x33AA[3:0])
0x33AC	OVLY_TOP	OVLY_TOP Bit[7:0]: OVLY_Top[7:0] (used with 0x33AA[6:4])
0x33AD	OVLY_MISC2	OVLY_MISC2 Bit[6:4]: OVLY_Bottom[10:8] (used with 0x33AF[7:0]) Bit[3:0]: OVLY_Right[11:8] (used with 0x33AE[7:0])
0x33AE	OVLY_RIGHT	OVLY_RIGHT Bit[7:0]: OVLY_Right[7:0] (used with 0x33AD[3:0])
0x33AF	OVLY_BOTTOM	OVLY_BOTTOM Bit[7:0]: OVLY_Bottom[7:0] (used with 0x33AD[6:4])
0x33B0	OVLY_MISC3	OVLY_MISC3 Bit[5:4]: OVLY_Ext_Width_V[9:8] (used with 0x33B2[7:0]) Bit[2:0]: OVLY_Ext_Width_H[10:8] (used with 0x33B1[7:0])
0x33B1	OVLY_EXT_WIDTH_H	OVLY_EXT_WIDTH_H Bit[7:0]: OVLY_Ext_Width_H[7:0] (used with 0x33B0[2:0])
0x33B2	OVLY_EXT_WIDTH_V	OVLY_EXT_WIDTH_V[7:0] Bit[7:0]: OVLY_Ext_Width_V[7:0] (used with 0x33B0[5:4])
0x33B3	OVLY_Y	OVLY_Y[7:0]
0x33B4	OVLY_U	OVLY_U[7:0]
0x33B5	OVLY_V	OVLY_V[7:0]

5.10 autofocus (AFC)

AFC has three required functions:

- Local Statistics - calculate maximum, minimum, and mean separately for R, G, and B in nine programmable zones
- Histograms - calculates intensity histograms of R, G, and B pixels separately in at least three different programmable zones
- Edge information - collects edge information for at least sixteen programmable zones

Contact your local OmniVision FAE for further details.

5.11 compression engine

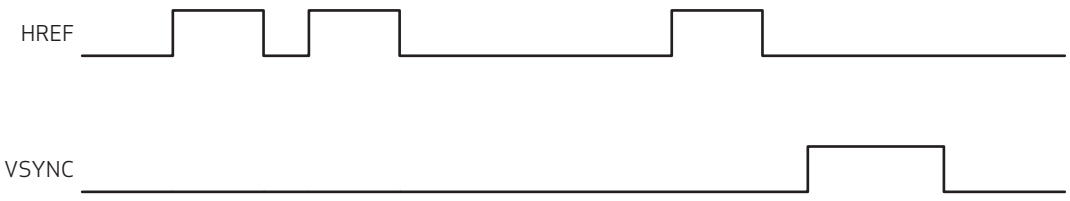
5.11.1 compression mode 0, 1, 2, 3, 4

In compression modes 1,2,3, the image width and image height are both fixed and set by width_man and height_man, respectively.

5.11.2 compression mode timing

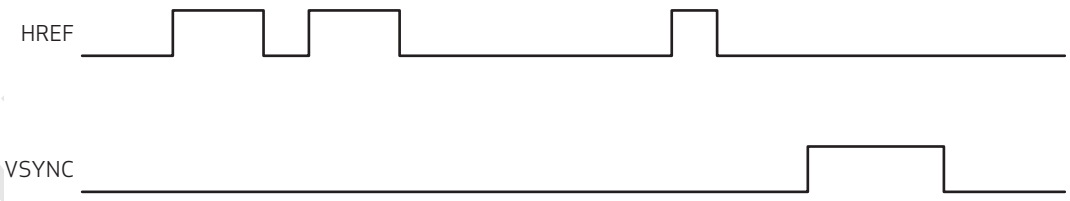
figure 5-1 compression mode 0 timing

a) dummy data padding at the last line



note 1 compression data is output with programmable width,
the last line may contain dummy data to match the width.
in each frame, the line numbers are different.

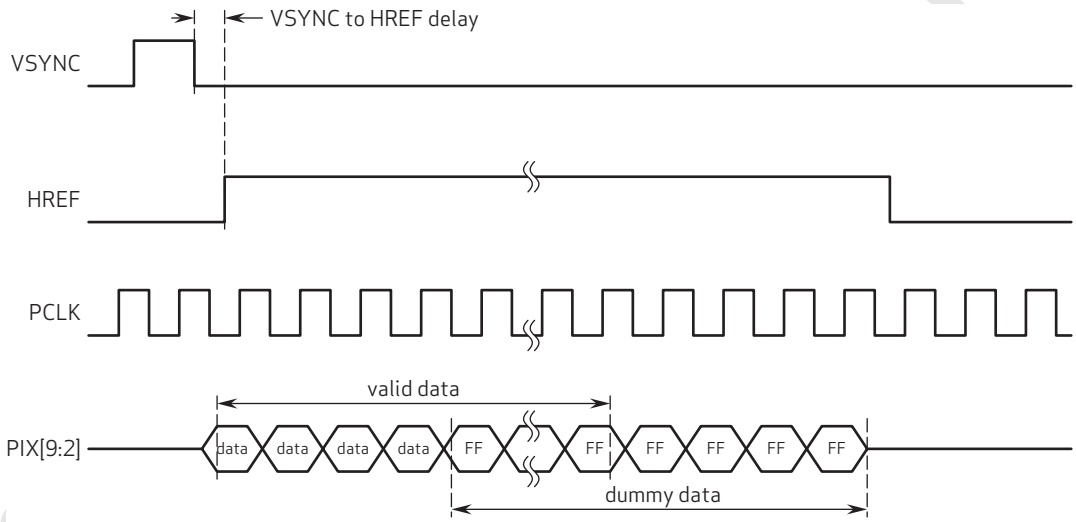
b) no dummy data padding at the last line



note 1 compression data is output with programmable width,
the last line may be less than others (there is no dummy data).
in each frame, the line numbers are different.

3640_DS_5_1

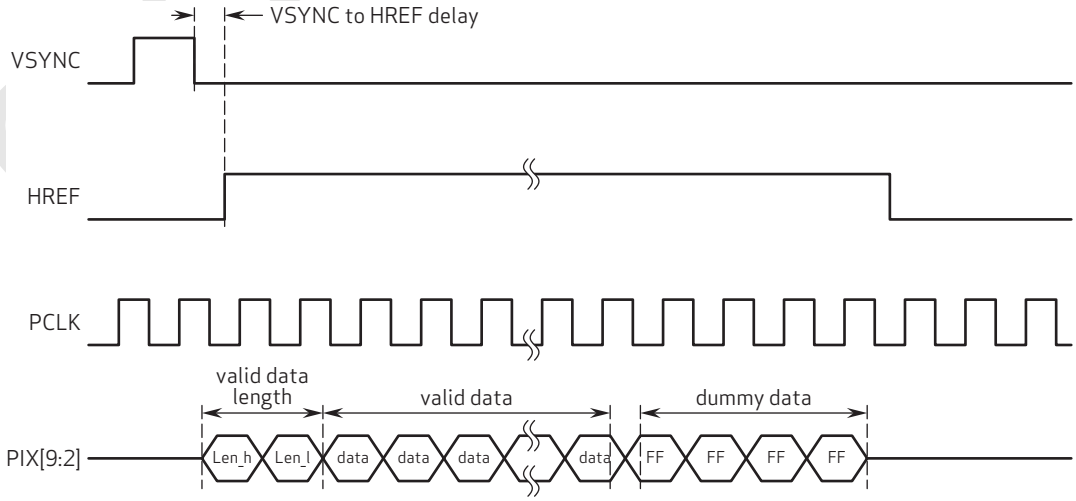
figure 5-2 compression mode 1 timing



note 1 user can set image width and height, the image line may contain dummy data (0xFF),
the number of the HREF in each frame is constant (=height).
the pixel number of each HREF is constant (=width).
the line blanking time and VSYNC to first HREF delay are both constant in each frame.

3640_DS_5_2

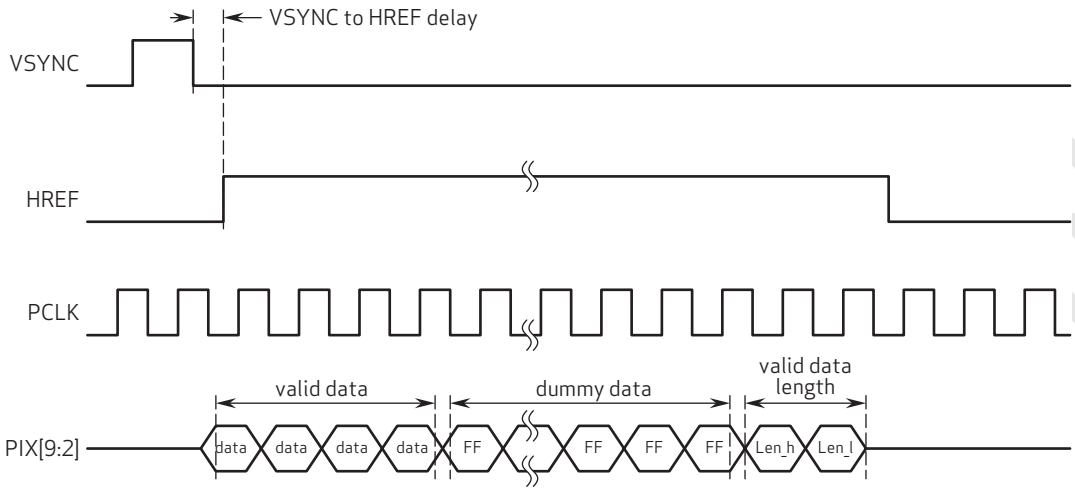
figure 5-3 compression mode 2 timing



note 1 user can set image width and height, the image line may contain dummy data (0xFF).
the first two bytes of each line is valid data length.
the number of the HREF in each frame is constant (=height).
the pixel number of each HREF is constant (=width).
the line blanking time and VSYNC to first HREF delay are both constant in each frame.

3640_DS_5_3

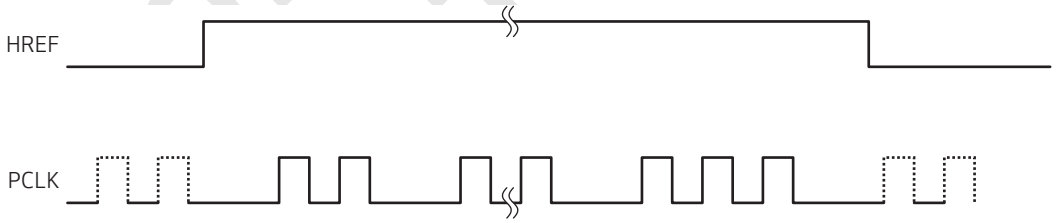
figure 5-4 compression mode 3 timing



note 1 user can set image width and height, the image line may contain dummy data (0xFF),
the last two bytes of each line is valid data length.
the number of the HREF in each frame is constant (=height).
the pixel number of each HREF is constant (=width).
the line blanking time and VSYNC to first HREF delay are both constant in each frame.

3640_DS_5_4

figure 5-5 compression mode 4 timing



note 1 the whole frame has only one HREF
PCLK will be gated when there is no image data to transmit

3640_DS_5_5

5.11.3 compression mode control

table 5-10 compression-related registers

register address	register name	function
0x3100	SC_CTRL0	SC_CTRL0 Bit[4]: Compression enable 0: Compression mode disabled 1: Compression mode enabled
0x3608	DVP_CTRL08	DVP Control 08 Bit[7:4]: HREF_dly, href delay PCLK2x number after VYSNC goes high when JFIFO overflows
0x3610	DVP_CTRL10	DVP Control 10 Bit[7:0]: Width_man[7:0]/4 Manual output image width
0x3611	DVP_CTRL11	DVP Control 11 Bit[7:5]: width_man[10:8], width_man_real=width_man*4
0x361E	DVP_CTRL1E	DVP Control 1E Bit[7]: Height_sel 0: Select height_in 1: Select height_man
0x363D	DVP_CTRL3D	DVP Control 3D Bit[2:0]: Compression_mode 000: Mode 0 001: Mode 1 010: Mode 2 011: Mode 3 100: Mode 4 100~111:Reserved
0x364A	DVP_CTRL4A	DVP Control 4A Bit[7:5]: Height_man_h
0x364B	DVP_CTRL4B	DVP Control 4B Bit[7:0]: Height_man_l For compression_mode, use height_man to set y_output_size

5.12 ISP system control

System control registers include clock and reset gated control. Individual modules can be reset or clock gated by setting registers 0x3104, 0x3105, 0x3106 and 0x3107.

table 5-11 system control-related registers (sheet 1 of 2)

register address	register name	function
0x3100	SC_CTRL0	SC_CTRL0 Bit[4]: Compression enable 0: Compression mode disabled 1: Compression mode enabled Bit[0]: DSP power down 0: DSP resume 1: DSP power down
0x3102	SC_CTRL2	SC_CTRL2 Bit[5]: DSP sensor/internal RGB gain control 0: DSP uses internal RGB gain 1: DSP uses sensor RGB gain
0x3104	SC_SYN_CTRL0	SC_SYN_CTRL0 Gated reset0 controls individual module reset (0: module enable; 1: module reset) Bit[7]: ISP_pad_rst Bit[6]: DSP_rst Bit[5]: CIF_ptn_rst Bit[4]: MIPI_top_rst Bit[3]: Format_rst Bit[2]: MIPI_rst_pclk Bit[1]: MC_top_rst Bit[0]: CIF_top_rst
0x3105	SC_SYN_CTRL1	SC_SYN_CTRL1 Gated clk0 controls individual module clock enable (0: module clock reset; 1: module clock enable) Bit[7]: ISP_pad_clk Bit[6]: DSP_clk Bit[5]: CIF_ptn_clk Bit[4]: MIPI_top_clk Bit[3]: Format_clk Bit[2]: MIPI_pclk Bit[1]: MC_top_clk Bit[0]: CIF_top_clk

table 5-11 system control-related registers (sheet 2 of 2)

register address	register name	function
0x3106	SC_SYN_CTRL2	SC_SYN_CTRL2 Gated reset1 controls individual module reset (0: module enable; 1: module reset) Bit[7]: CIF_pad_rst Bit[6]: RGB_dither_rst Bit[5]: YUV2RGB_rst Bit[4]: Compression2x_rst Bit[3]: Fmt_mux_rst Bit[2]: CIF_ext_rst Bit[1]: SCCB_arb_rst Bit[0]: Compression_top_rst
0x3107	SC_SYN_CTRL3	SC_SYN_CTRL3 Gated clk1 controls individual module clock enable (0: module clock reset; 1: module clock enable) Bit[6]: RGB_dither_clk Bit[5]: YUV2RGB_clk Bit[4]: Compression2x_clk Bit[3]: Fmt_mux_clk Bit[2]: CIF_ext_clk Bit[1]: SCCB_arb_clk Bit[0]: Compression_top_clk

5.13 MCU description

Microprocessor firmware can be downloaded by writing to registers starting from 0x8000. A total of 6 kB of program memory can be used for program storage. Before downloading the firmware, the user must enable the MCU clock by setting 0x3105[1] to one. After downloading the firmware, set 0x3104[1] to zero to enable MCU.

MCU interrupts are triggered by several internal signals for firmware development.

table 5-12 MCU-related registers

register address	register name	function
0x3700	INTR_MASK0	INTR_MASK0 MCU interrupt0 mask (0: enable interrupt; 1: mask interrupt) Bit[7]: Interrupt0 mask[7] Bit[6]: Interrupt0 mask[6] Bit[5]: Interrupt0 mask[5] Bit[4]: Interrupt0 mask[4] Bit[3]: Interrupt0 mask[3] Bit[2]: Interrupt0 mask[2] Bit[1]: Interrupt0 mask[1] Bit[0]: Interrupt0 mask[0]
0x3701	INTR_MASK1	INTR_MASK1 MCU interrupt1 mask (0: enable interrupt; 1: mask interrupt) Bit[7]: Interrupt1 mask[7] Bit[6]: Interrupt1 mask[6] Bit[5]: Interrupt1 mask[5] Bit[4]: Interrupt1 mask[4] Bit[3]: Interrupt1 mask[3] Bit[2]: Interrupt1 mask[2] Bit[1]: Interrupt1 mask[1] Bit[0]: Interrupt1 mask[0]
0x3708	INTR0	MCU Interrupt 0 Bit[7]: Interrupt 0[7] Bit[6]: Interrupt 0[6] Bit[5]: Interrupt 0[5] Bit[4]: Interrupt 0[4] Bit[3]: Interrupt 0[3] Bit[2]: Interrupt 0[2] Bit[1]: Interrupt 0[1] Bit[0]: Interrupt 0[0]
0x3709	INTR1	MCU Interrupt 1 Bit[7]: Interrupt 1[7] Bit[6]: Interrupt 1[6] Bit[5]: Interrupt 1[5] Bit[4]: Interrupt 1[4] Bit[3]: Interrupt 1[3] Bit[2]: Interrupt 1[2] Bit[1]: Interrupt 1[1] Bit[0]: Interrupt 1[0]

5.14 CIF description

The Camera Interface (CIF) receives asynchronous stream data from various sources and provides buffering and synchronization. CIF also supports internal sensor and external sensor modes. The input source can be selected by setting register 0x3200.

table 5-13 CIF register list

register address	register name	function
0x3200	CIF_CTRL_0	CIF Control 0 Bit[7:5]: CIF_mode[2:0] This function selects the camera interface image source. 000: Internal sensor mode 001: Reserved 010: External sensor mode - data input through DVP port 011~111:Reserved

5.15 format description

Format control converts internal data format into the desirable output format including YUV, RGB, raw, compression data, CCIR656, HSYNC mode, etc.

table 5-14 format control register list (sheet 1 of 3)

register address	register name	function
0x3400	FMT_MUX_CTRL0	FMT_MUX_CTRL0 Bit[2:0]: Format input source select 000: DSP YUV444 001: DSP RGB888 010: DSP YUV422 011: DSP raw 100: Internal CIF raw 101: External CIF raw 110: External CIF YUV422 bypass 111: Not used
0x3403	ISP_PAD_CTRL2	ISP_PAD_CTRL2 Bit[7:4]: Xstart - x start address for DVP windowing Bit[3:0]: Ystart - y start address for DVP windowing

table 5-14 format control register list (sheet 2 of 3)

register address	register name	function
0x3404	FMT_CTRL00	FMT_CTRL00 Bit[7]: UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in Bit[5:0]: YUV422: 0x00: yuyvyuyv..../yuyvyuyv.... 0x01: yvyuyvyu..../yvyuyvyu.... 0x02: uyvyuyvy..../uyvyuyvy.... 0x03: vyuyvyuy..../vyuyvyuy.... YUV420: 0x04: yyyy..../yuyvyuyv.... 0x05: yyyy..../yvyuyvyu.... 0x06: yyyy..../uyvyuyvy.... 0x07: yyyy..../vyuyvyuy.... 0x08: yuyvyuyv..../yyyy.... 0x09: yvyuyvyu..../yyyy.... 0x0A: uyvyuyvy..../yyyy.... 0x0B: vyuyvyuy..../yyyy.... 0x0C: uyyuyy..../vyyvyy Y8: 0x0D: yyyy..../yyyy.... YUV444 (RGB888) 0x0E: yuvyuv..../yuvyuv.... (gbrgbr..../gbrgbr....) 0x0F: yvuyvu..../yvuyvu.... (grbgrb..../grbgrb....) 0x1C: uyvuyv..../uyvuyv.... (bgrbgr..../bgrbgr....) 0x1D: vyuvyu..../vyuvyu.... (rgbrgb..../rgbrgb....) 0x1E: uvyuvy..../uvyuvy.... (brgbrg..../brgbrg....) 0x1F: vuyvuy..../vuyvuy.... (rbgrbg..../rbgrbg....) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565) RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0]} 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} RGB444: 0x14: {b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15: {r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34: {g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37: {4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38: {4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... RAW: 0x18: bgbg..../grgr.... 0x19: gbgb..../rgrg.... 0x1A: grgr..../bgbg.... 0x1B: rgrg..../gbgb....

table 5-14 format control register list (sheet 3 of 3)

register address	register name	function
0x3405	DITHER_CTRL0	DITHER_CTRL0 Bit[6]: Dither_sel 0: Use register setting 1: Dithering according to fmt_control Bit[5:4]: R_dithering 00: No dithering 01: 4 bit 10: 5 bit 11: 6 bit Bit[3:2]: G_dithering 00: No dithering 01: 4 bit 10: 5 bit 11: 6 bit Bit[1:0]: B_dithering 00: No dithering 01: 4 bit 10: 5 bit 11: 6 bit

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including compression mode, CCIR656 format, HSYNC mode and test pattern output.

6.1.2 HSYNC mode

In this mode, the line blanking time and VSYNC to the first image line are fixed. Also, there are dummy lines when vertical blanking. Only full size Raw/YUV format is supported.

table 6-1 DVP-related registers (sheet 1 of 2)

register address	register name	function
0x3600	OUT_CTRL00	DVP Control 00 Bit[7]: VSYNC_sel2 1: VSYNC mode 3 select Bit[6]: VSYNC_gate 1: Gate DVP_PCLK when VSYNC and PCLK_gate_en Bit[4]: PCLK_pol 1: PCLK will be reversed Bit[3]: HREF_pol 1: HREF will be reversed Bit[2]: VSYNC_pol 1: VSYNC will be reversed Bit[1]: VSYNC_sel 0: VSYNC mode 1 select 1: VSYNC mode 2 select Bit[0]: Data_order 0: DVP output DVP_data[9:0] 1: DVP output DVP_data[0:9]
0x3601	OUT_CTRL01	DVP Control 01 Bit[7]: PCLK_gate_en 1: Manual line width enable Bit[4]: CCIR656_en
0x3609	OUT_CTRL09	DVP Control 09 The user can use this register to set VSYNC width when VSYNC_sel = 0 and VSYNC_sel2 = 0 Bit[7:0]: VSYNC_width, VSYNC_width_real = VSYNC_width × 16
0x360D	OUT_CTRL0D	DVP Control 0D Bit[7]: Tst_bit8 0: 10-bit mode 1: Test mode for 8-bit mode

table 6-1 DVP-related registers (sheet 2 of 2)

register address	register name	function
0x3614	OUT_CTRL14	DVP Control 14 Bit[7:0]: Clip_min, minimum clipping value Clip_min and cilp_max specifies the minimum and the maximum value of output data respectively.
0x3615	OUT_CTRL15	DVP Control 15 Bit[7:0]: Clip_max, clipping max value
0x3616	OUT_CTRL16	DVP Control 16 Bit[3:2]: Clip_max_h[1:0] Bit[1:0]: Clip_min_h[1:0]
0x361D	OUT_CTRL1D	DVP Control 1D Bit[1:0]: Test pattern selection 00: No test pattern 01: Test pattern 1 10: Test pattern 2
0x363C	OUT_CTRL3C	DVP Control 3C Bit[6:5]: H2v_dly, the last HREF to VSYNC delay for VSYNC mode 3 Bit[4:3]: V2h_dly, VSYNC to HREF delay for VSYNC mode 3
0x363D	OUT_CTRL3D	DVP Control 3D Bit[7]: DVP_H 0: Output DVP_data[9:0] 1: Output DVP_data[7:0,9:8] Bit[3]: DVP_L 0: Select DVP_data[9:2] when in 8-bit DVP mode 1: Select DVP_data[7:0]
0x363E	OUT_CTRL3E	DVP Control 3E Bit[7:0]: EOF2v_dly_h, when VSYNC_sel2 = 1. After the last HREF, VSYNC will be high after EOF2v_dly cycles. There are 3 bytes for EOF2v_dly.
0x363F	OUT_CTRL3F	DVP Control 3F Bit[7:0]: EOF2v_dly_m
0x3640	OUT_CTRL40	DVP Control 40 Bit[7:0]: EOF2v_dly_l
0x3646	OUT_CTRL46	DVP Control 46 Bit[6]: HSYNC_en, enable HSYNC mode for DVP, MIPI is disabled Bit[2]: HSYNC_DVP_en HSYNC_GEN output DVP mode, line blanking and VSYNC to HREF are both constant

6.1.3 DVP timing

figure 6-1 DVP timing diagram

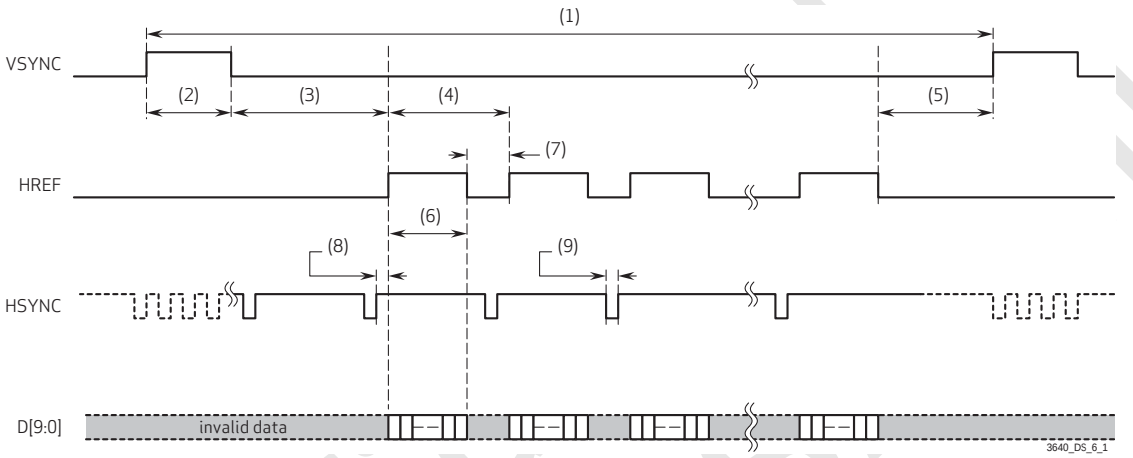


table 6-2 DVP timing specifications (sheet 1 of 2)

mode	timing
QXGA 2048x1536	(1) 3725568 tp ≅ 1568 tline (2) 2048 tp (4 tline = 2376 × 4 = 9504 tp in HSYNC mode) (3) 28724 tp (4) 2376 tp (5) 45588 tp (6) 2048 tp (7) 328 tp (8) 0 tp (9) 328 tp
UXGA 1600x1200	(1) 2901177 tp ≅ 1221 tline (2) 2048 tp (3) 31638 tp (4) 2376 tp (5) 17067 tp (6) 1600 tp (7) 776 tp (8) 0 tp (9) 776 tp

note
The timing values shown in table 6-2 may vary depending upon register settings.

table 6-2 DVP timing specifications (sheet 2 of 2)

mode	timing
XGA 1024x768 (PCLK/2)	(1) 1849715 tp ≅ 779 tline (2) 2048 tp (4 tline = 2376 x 4 = 9504 tp in HSYNC mode) (3) 15787 tp (4) 2376 tp (5) 8464 tp (6) 1024 tp (7) 1352 tp (8) 0 tp (9) 1352 tp
SQCIF 128x96 (PCLK/14)	(1) 264300 tp ≅ 97 tline (2) 2048 tp (3) 2967 tp (4) 2716 tp (5) 1137 tp (6) 128 tp (7) 2588 tp (8) 0 tp (9) 2588 tp

6.1.4 DVP image formats

6.1.4.1 YUV422 format

Uncompressed YUV422 data is sent out through DATA[9:2] and the sequence can be YUYV, UYVY, YVYU, VYUY.

table 6-3 YUYV format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]
odd	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]

table 6-4 UYVY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]
odd	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]

table 6-5 YVYU format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]
odd	Y[7:0]	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]

table 6-6 VYUY format

DATA[9:2]	first pixel	first pixel	second pixel	second pixel	third pixel	third pixel
even	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]
odd	V[7:0]	Y[7:0]	U[7:0]	Y[7:0]	V[7:0]	Y[7:0]

6.1.4.2 YUV420 format

The data format of uncompressed YUV420 is similar to that of uncompressed YUV422 except that UV data of either even or odd lines is dropped by de-asserting PCLK.

6.1.4.3 Y8 format

Uncompressed Y8 data is sent out through DATA[9:2]. The frequency of PCLK is the same as that of raw data or half of YUV422/420.

6.1.4.4 RGB565 format

Uncompressed RGB565 data is sent out through DATA[9:2].

table 6-7 RGB565 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	G2	B7	B6	B5	B4	B3

6.1.4.5 RGB555 format

table 6-8 RGB555 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	R7	R6	R5	R4	R3	G7	G6	G5
odd	G4	G3	0	B7	B6	B5	B4	B3

6.1.4.6 RGB444 format

The data format of uncompressed RGB444 is similar to RGB565 except that the lowest bit of R, B, and the lowest 2 bits of G are dummy bits.

table 6-9 RGB444 format

bytes	D9	D8	D7	D6	D5	D4	D3	D2
even	X	X	X	X	R7	R6	R5	R4
odd	G7	G6	G5	G4	B7	B6	B5	B4

6.2 mobile industry processor interface (MIPI)

MIPI provides a single uni-directional clock lane and two bi-directional data lane solution for communication links between components inside a mobile device. Two data lanes have full support for HS(uni-direction) and LP (bi-directions) data transfer mode. Contact your local OmniVision FAE for more details.

7 register tables

The following tables provide descriptions of the device control registers contained in the OV3640. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x78 for write and 0x79 for read.

table 7-1 system control registers (sheet 1 of 15)

address	register name	default value	R/W	description
0x3000	AGC[15:8]	0x00	RW	Auto Gain Control Bit[7:0]: AGC RSVD gain register
0x3001	AGC[7:0]	0x00	RW	Auto Gain Control - AGC[7:0] Bit[7:0]: Actual Gain – Range from 1x to 32x Gain = (Bit[7]+1) x (Bit[6]+1) × (Bit[5]+1) × (Bit[4]+1) × (1+Bit[3:0]/16) Set Auto1[2] (R0x3013[2]) = 0 to disable AGC.
0x3002	AEC[15:8]	0x00	RW	Auto Exposure Control - AEC[15:8]
0x3003	AEC[7:0]	0x01	RW	Auto Exposure Control - AEC[7:0] AEC[15:0]: Exposure time Tex = Tline × AEC[15:0] Tline ≤ Tex ≤ 1 frame period The maximum exposure time will be 1 frame period even if Tex is set longer than 1 frame period. Set Auto1[0] (R0x3013[0]) = 0 to disable AEC.
0x3004	AECL[7:0]	0x00	RW	Manual Extreme Bright Exposure Control - AECL[7:0] In extremely bright conditions where Tex must be less than Tline, the exposure time may be set manually by this control. Tex = Tline – L1AEC[7:0] steps Tex min. ≤ Tex ≤ Tline Set Auto2[1] (R0x3014[1]) = 1 to enable manual AECL.
0x3005	RED[7:0]	0x40	RW	AWB Red Gain
0x3006	GREEN[7:0]	0x40	RW	AWB Green Gain
0x3007	BLUE[7:0]	0x40	RW	AWB Blue Gain
0x3008~ 0x3009	RSVD	–	–	Not used
0x300A	PIDH	0x36	RW	Product ID MSBs (read only)
0x300B	PIDL	0x40	RW	Product ID LSBs (read only)
0x300C	SCCB ID	0x78	RW	SCCB ID

table 7-1 system control registers (sheet 2 of 15)

address	register name	default value	R/W	description
0x300D	PCLK[7:0]	0x00	RW	Pixel Clock Output Control Bit[7:6]: Not used Bit[5]: PCLK output selection 0: PCLK always output 1: PCLK output qualified by HREF Bit[4]: PCLK reverse Bit[3:2]: Not used Bit[1]: PCLK divided by 4 Bit[0]: PCLK divided by 2
0x300E	PLL_1[7:0]	0x33	RW	PLL Control 1 Bit[7:6]: Reserved Bit[5:0]: Rx_PLL[5:0] PLL divider control bits PLLDiv = 64 - Rx_PLL[5:0]
0x300F	PLL_2[7:0]	0x81	RW	PLL Control 2 Bit[7:6]: FreqDiv control bits 00: FreqDiv = 1 01: FreqDiv = 1.5 10: FreqDiv = 2 11: FreqDiv = 3 Bit[5:4]: Bit8Div control bits 00: Bit8Div = 1 01: Bit8Div = 1 10: Bit8Div = 4 11: Bit8Div = 5 Bit[3]: Bypass 0: Sysclk = Serclk = Dvpclk = Refclk 1: Default, shut down PLL and dividers, pass input Refclk signal directly to outputs Bit[2]: Not used Bit[1:0]: InDiv control bits 00: InDiv = 1 01: InDiv = 1.5 10: InDiv = 2 11: InDiv = 3

table 7-1 system control registers (sheet 3 of 15)

address	register name	default value	R/W	description
0x3010	PLL_3[7:0]	0x41	RW	PLL Control 3 Bit[7:6]: DvpDiv control bit 00: DvpDiv = 1 01: DvpDiv = 2 10: DvpDiv = 8 11: DvpDiv = 16 Bit[5]: LaneDiv control bit 0: LaneDiv = 1 1: LaneDiv = 2 Bit[4]: SensorDiv control bit 0: SensorDiv=1 1: SensorDiv=2 Bit[3:0]: ScaleDiv control bits ScaleDiv = Rx_PLL[9:6] × 2 @ RxPLL[9:6] > 0 ScaleDiv = 1 @ RxPLL[9:6]=0
0x3011	CLK[7:0]	0x00	RW	Clock Rate Control Bit[7]: Digital frequency doubler 0: OFF 1: ON Bit[6]: PLL and clock divider bypass 0: Master mode, sensor provides PCLK 1: Slave mode, external PCLK input from XCLK1 pin Bit[5:0]: Clock divider CLK = XCLK1/(decimal value of CLK[5:0] + 1)
0x3012	SYS[7:0]	0x00	RW	Format Control Bit[7]: SRST 1: Initiates soft reset. All register are set to factory default values after which the chip resumes normal operation Bit[6:4]: Sensor array resolution 000: QXGA (full size) mode 001: XGA mode 111: SXGA (full size) mode Bit[3]: CC656 protocal on/off (not used) Bit[2:0]: Output format selection (not used)

table 7-1 system control registers (sheet 4 of 15)

address	register name	default value	R/W	description
0x3013	AUTO_1[7:0]	0xE7	RW	Auto Control 1 Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: AEC speed/step selection 0: Small steps, slow 1: Big steps, fast Bit[5]: Banding filter selection 0: OFF 1: ON, set minimum exposure to 1/120s Bit[4]: Auto banding filter 0: Banding filter is always ON/OFF depending on AUTO_1[5] (R0x3013[5]) setting 1: Automatically disable the banding filter under strong light condition Bit[3]: Extreme bright exposure control enable 0: OFF, Tline <= Tex min. 1: ON, enable minimum exposure Tex min. ≤ Tline Bit[2]: Auto gain control auto/manual mode selection 0: Manual 1: Auto Bit[1]: Not used Bit[0]: Auto exposure control auto/manual mode selection 0: Manual 1: Auto

table 7-1 system control registers (sheet 5 of 15)

address	register name	default value	R/W	description
0x3014	AUTO_2[7:0]	0x04	RW	Auto Control 2 Bit[7]: Manually assign banding 0: 60Hz 1: 50Hz Bit[6]: Auto banding detection enable 0: Banding according to AUTO_2[7] (R0x3014[7]) manual setting 1: Banding depending on auto 50/60 Hz detection result Bit[5]: AddLT1F in AGC Bit[4]: Freeze AEC/AGC Bit[3]: Night mode enable 0: Disable 1: Enable Bit[2]: BDcAEC - enable banding AEC smooth switch between 50/60 Bit[1]: Manually assign extreme bright exposure enable 0: Auto exposure 1: Exposure based on AECL[7:0] (R0x3004[7:0]) steps Bit[0]: Banding filter option 0: Disable 1: Enable
0x3015	AUTO_3[7:0]	0x02	RW	Auto Control 3 Bit[7]: Not used Bit[6:4]: Dummy frame control 000: No dummy frame 001: Allow 1 dummy frame 010: Allow 2 dummy frames 011: Allow 3 dummy frames 100: Allow 7 dummy frames Bit[3]: Not used Bit[2:0]: AGC gain ceiling, GH[2:0]: 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x 111: 128x
0x3016	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 6 of 15)

address	register name	default value	R/W	description
0x3017	AUTO_5[7:0]	0x00	RW	Auto Control 5 Bit[7:6]: Not used Bit[5:0]: Manual banding counter
0x3018	WPT/HISH[7:0]	0x78	RW	Luminance Signal/Higtogram High Range for AEC/AGC operation Shared by average and higtogram based algorithm AEC/AGC value decreases in auto mode when average luminance/higtogram is greater than WPT/HisH[7:0]
0x3019	BPT/HISL[7:0]	0x68	RW	Luminance Signal/Higtogram Low Range for AEC/AGC operation Shared by average and higtogram based algorithm AEC/AGC value increases in auto mode when average luminance/higtogram is less than BPT/HisL[7:0]
0x301A	VPT[7:0]	0xD4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than VV[7:4] or less than VV[3:0]
0x301B	YAVG	0x00	RW	Luminance Average - this register will auto update Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
0x301C	AECG_MAX50	0x05	RW	50 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX50[5:0] 50 Hz smooth banding maximum steps
0x301D	AECG_MAX60	0x07	RW	60 Hz Smooth Banding Maximum Steps Control Bit[7:6]: Reserved Bit[5:0]: AECG_MAX60[5:0] 60 Hz smooth banding maximum steps
0x301E	RZM[15:8]	0x00	RW	Zoom Mode Array Vertical Entry Start Point 8 MSBs

table 7-1 system control registers (sheet 7 of 15)

address	register name	default value	R/W	description
0x301F	RZM[7:0]	0x00	RW	Zoom Mode Array Vertical Entry Start Point 8 LSBs
0x3020	HS[15:8]	0x01	RW	Horizontal Window Start 8 MSBs HS[15:0]:Horizontal start point of array, each bit represents 1 pixel
0x3021	HS[7:0]	0x0D	RW	Horizontal Window Start 8 LSBs HS[15:0]:Horizontal start point of array, each bit represents 1 pixel
0x3022	VS[15:8]	0x00	RW	Vertical Window Start 8 MSBs VS[15:0]:Vertical start point of array, each bit represents 1 scan line
0x3023	VS[7:0]	0x0A	RW	Vertical Window Start 8 LSBs VS[15:0]:Vertical start point of array, each bit represents 1 scan line
0x3024	HW[15:8]	0x18	RW	Horizontal Width 8 MSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3025	HW[7:0]	0x00	RW	Horizontal Width 8 LSBs HW[15:0]:Output raw image pixels are from HS[15:0] to HS[15:0] + HW[15:0]
0x3026	VH[15:8]	0x06	RW	Vertical Height 8 MSBs VH[15:0]:Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3027	VH[7:0]	0x0C	RW	Vertical Height 8 LSBs VH[15:0]:Output raw image pixels are from VS[15:0] to VS[15:0] + VH[15:0]
0x3028	HTS[15:8]	0x09	RW	Horizontal Total Size 8 MSBs HTS[15:0]:Horizontal total size for 1 line
0x3029	HTS[7:0]	0x47	RW	Horizontal Total Size 8 LSBs HTS[15:0]:Horizontal total size for 1 line
0x302A	VTS[15:8]	0x06	RW	Vertical Total Size 8 MSBs VTS[15:0]:Vertical total size for 1 frame
0x302B	VTS[7:0]	0x20	RW	Vertical Total Size 9 LSBs VTS[15:0]:Vertical total size for 1 frame
0x302C	EXHTS[7:0]	0x00	RW	Line Interval Adjustment Value (dummy pixels) The frame rate will be adjusted by changing the line interval. Each LSB will add 1/2376 Tframe to the frame period

table 7-1 system control registers (sheet 8 of 15)

address	register name	default value	R/W	description
0x302D	EXVTS[15:8]	0x00	RW	VSYNC Pulse Width 8 MSBs EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x302E	EXVTS[7:0]	0x00	RW	VSYNC Pulse Width LSB 8 bits EXVTS[15:0]:Line periods added to VSYNC width. Default VSYNC output width is 4 × tline. Each LSB count will add 1 × Tline to the VSYNC active period.
0x302F	RSVD	–	–	Reserved
0x3030	WEIGHT0	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 1, weight from 0 to 15 Bit[3:0]: Zone 0, weight from 0 to 15
0x3031	WEIGHT1	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 3, weight from 0 to 15 Bit[3:0]: Zone 2, weight from 0 to 15
0x3032	WEIGHT2	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 5, weight from 0 to 15 Bit[3:0]: Zone 4, weight from 0 to 15
0x3033	WEIGHT3	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 7, weight from 0 to 15 Bit[3:0]: Zone 6, weight from 0 to 15
0x3034	WEIGHT4	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 9, weight from 0 to 15 Bit[3:0]: Zone 8, weight from 0 to 15
0x3035	WEIGHT5	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 11, weight from 0 to 15 Bit[3:0]: Zone 10, weight from 0 to 15
0x3036	WEIGHT6	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 13, weight from 0 to 15 Bit[3:0]: Zone 12, weight from 0 to 15
0x3037	WEIGHT7	0x11	RW	16-Zone Average Weight Bit[7:4]: Zone 15, weight from 0 to 15 Bit[3:0]: Zone 14, weight from 0 to 15
0x3038	AHS[15:8]	0x01	RW	Average Window Horizontal Start 8 MSBs AHS[15:0]:Horizontal average start point, each bit represents 1 pixel

table 7-1 system control registers (sheet 9 of 15)

address	register name	default value	R/W	description
0x3039	AHS[7:0]	0x09	RW	Average Window Horizontal Start 8 LSBs AHS[15:0]:Horizontal average start point, each bit represents 1 pixel
0x303A	AVS[15:8]	0x00	RW	Average Window Vertical Start 8 MSBs AVS[15:0]:Vertical average start point, each bit represents 1 scan line
0x303B	AVS[7:0]	0x0A	RW	Average Window Vertical Start 8 LSBs AVS[15:0]:Vertical average start point, each bit represents 1 scan line
0x303C	RSVD/AHW[11:8]	0x02	RW	Average Window Horizontal Width 8 MSBs Bit[7:4]: Reserved Bit[3:0]: AHW[11:8] AHW[11:0]:Average window horizontal width, each bit represents 1 pixel
0x303D	AHW[7:0]	0x00	RW	Average Window Horizontal Width 8 LSBs AHW[11:0]:Average window horizontal width, each bit represents 1 pixel
0x303E	RSVD/AVH[11:8]	0x01	RW	Average Window Vertical Height 8 MSBs Bit[7:4]: Reserved Bit[3:0]: AVH[11:8] AVH[11:0]:Average window vertical height, each bit represents 1 line
0x303F	AVH[7:0]	0x80	RW	Average Window Vertical Height 8 LSBs AVH[11:0]:Average window vertical height, each bit represents 1 line
0x3040	HISTO0	0xD0	RW	LPH – Lower Limit of Probability for HRL, after exposure/gain stabilizes
0x3041	HISTO1	0xD0	RW	UPL – Upper Limit of Probability for LRL, after exposure/gain stabilizes
0x3042	HISTO2	0xF0	RW	TPL – Probability Threshold for LRL to control AEC/AGC speed
0x3043	HISTO3	0x90	RW	TPH – Probability Threshold for HRL to control AEC/AGC speed

table 7-1 system control registers (sheet 10 of 15)

address	register name	default value	R/W	description
0x3044	HISTO4	0xE5	RW	Bit[7:4]: TLH – High nibble of Luminance Threshold for AEC/AGC speed control Bit[3:0]: TLL – Low nibble of Luminance Threshold for AEC/AGC speed control
0x3045	HISTO5	0xE3	RW	Reserved
0x3046	HISTO6	0x04	RW	Reserved
0x3047	HISTO7	0x05	RW	Reserved
0x3048	D56C1	0x00	RW	D56 Control 1 Reserved for 50/60Hz auto detection Bit[7:6]: D56 clock divider 00: /2 01: /4 10: /8 11: /1 Bit[5]: Frame50/60 select 0: Frame50 1: Frame60 Bit[4]: Stop D50 processing Bit[3:2]: Maximum allowed gain 00: Any 01: x16 10: x8 11: x4, when gain is larger than max gain, current frame will be ignored Bit[1:0]: VS divider 00: /1 01: /2 1x: /4, when frame rate is too fast (>50), D56 operations cannot complete within 1 frame, this divider need to be set.
0x3049~ 0x3068	RSVD	–	–	Reserved
0x3069	BLC9	0x44	RW	Black Level Calibration Control 9 Bit[7:4]: Reserved Bit[3:0]: Target black level value
0x306A~ 0x306F	RSVD	–	–	Reserved
0x3070	BD50[15:8]	0x00	RW	50Hz Banding 8 MSBs 50Hz = 1 / (BD50[15:0] × Tline)

table 7-1 system control registers (sheet 11 of 15)

address	register name	default value	R/W	description
0x3071	BD50[7:0]	0xEB	RW	50Hz Banding 8 LSBs 50Hz = 1 / (BD50[15:0] × Tline)
0x3072	BD60[15:8]	0x00	RW	60Hz Banding 8 MSBs 60Hz = 1 / (BD60[15:0] × Tline)
0x3073	BD60[7:0]	0xC4	RW	60Hz Banding 8 LSBs 60Hz = 1 / (BD60[15:0] × Tline)
0x3074	RSVD	–	–	Reserved
0x3075	VSYNCOPT	0x44	RW	Vsync Pulse Options Bit[7]: Not used Bit[6:4]: VSYNC start point option where each bit represents 1 Tline Bit[3]: Not used Bit[2:0]: VSYNC pulse width option where each bit represents 1 Tline
0x3076	RSVD	–	–	Reserved
0x3077	TMC1	0x00	RW	Timing Control 1 Bit[7]: CHSYNC pin output swap 0: CHSYNC 1: HREF Bit[6]: HREF pin output swap 0: HREF 1: CHSYNC Bit[5:4]: Reserved Bit[3]: HREF output polarity 0: Output positive HREF 1: Output negative HREF, HREF negative for data valid Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: HSYNC polarity 0: Positive 1: Negative

table 7-1 system control registers (sheet 12 of 15)

address	register name	default value	R/W	description
0x3078	TMC2	0x00	RW	Timing Control 2 Bit[7:2]: Reserved Bit[1]: VSYNC drop option 0: VSYNC is always output 1: VSYNC is dropped if frame data is dropped Bit[0]: Frame data drop 0: Disable data drop 1: Drop frame data if exposure is not within tolerance. In AEC mode, data is normally dropped when data is out of range.
0x3079	TMC3	0x20	RW	Timing Control 3 Bit[7]: VSLatopt - group latch pulse option Bit[6:0]: Reserved
0x307A	TMC4	0x00	RW	Timing Control 4 Bit[7:0]:RSTRB[7:0] - flash light control
0x307B	TMC5	0x40	RW	Timing Control 5 Bit[7]: AWB B/R/G gain write disable option Bit[6:4]: Reserved Bit[3]: Digital color bar enable Bit[2:0]: Pattern - select digital color bar pattern
0x307C	TMC6	0x00	RW	Timing Control 6 Bit[7:6]: Reserved Bit[5]: Digital gain enable Bit[4:2]: Reserved Bit[1]: Horizontal mirror Bit[0]: Vertical flip
0x307D	TMC7	0x00	RW	Timing Control 7 Bit[7]: Color bar test pattern 0: OFF 1: ON Bit[6]: Reserved Bit[5]: Avg_raw - select data for avg/histo calculation 0: Data from DSP 1: Data from Sensor Bit[4]: Reserved Bit[3:2]: aver_opt for histogram calculation Bit[1:0]: sample_opt for histogram calculation

table 7-1 system control registers (sheet 13 of 15)

address	register name	default value	R/W	description
0x307E	TMC8	0xC5	RW	Timing Control 8 Bit[7:6]: Digital gain source 00: From AGC[5:4] 01: From AGC[6:5] 1x: From AGC[7:6] Bit[5:0]: Reserved
0x307F	RSVD	–	–	Reserved
0x3080	TMCA	0x11	RW	Timing Control A Bit[7]: Output pattern option Bit[6:0]: Reserved
0x3081	TMCB	0x04	RW	Timing Control B Bit[7]: MIRROR_OPT - pixel shift while mirroring 0: OFF 1: ON Bit[6]: OTP memory clock option 0: Slow 1: Fast Bit[5:1]: Reserved Bit[0]: Swap MSB and LSB at the output port
0x3082~ 0x3084	RSVD	–	–	Reserved
0x3085	TMCF	0x00	RW	Timing Control F Bit[7:6]: Reserved Bit[5]: Pixel shift Bit[4:1]: Reserved Bit[0]: Out8b option for color bar use
0x3086	TMC10	0x00	RW	Timing Control 10 Bit[7:4]: Reserved Bit[3]: Sys_reset, Sys_rest_pll Enable Bit[2]: RegSleep option Bit[1]: Sleep option Bit[0]: Sleep ON/OFF 0: OFF 1: ON
0x3087	TMC11	0x02	RW	Timing Control 11 Bit[7:5]: Reserved Bit[4]: Average block clock option 0: From ISP_SCLK_in 1: From DSPCK Bit[3:2]: Not used Bit[1:0]: Pixel order for color bar use

table 7-1 system control registers (sheet 14 of 15)

address	register name	default value	R/W	description
0x3088	ISP_XOUT[15:8]	0x80	RW	ISP X-direction Output Size [15:8] Bit[7:4]: Not used Bit[3:0]: X_size_in[11:8]
0x3089	ISP_XOUT[7:0]	0x00	RW	ISP X-direction Output Size [7:0]
0x308A	ISP_YOUT[15:8]	0x06	RW	ISP Y-direction Output Size [15:8] Bit[7:3]: Not used Bit[2:0]: X_size_in[10:8]
0x308B	ISP_YOUT[7:0]	0x00	RW	ISP Y-direction Output Size [7:0]
0x308C	RSVD	–	–	Reserved
0x308D	TMC13	0x00	RW	Timing Control 13 Bit[7]: RegSleep setting Bit[6:5]: Reserved Bit[4]: MIPI disable Bit[3]: OUT_I2C_susp option2 Bit[2]: RESET block sleep enable Bit[1]: RegSleep option
0x308E	5060	–	R	50/60 Auto Detection Internal Data Readout
0x308F	OTP	–	R	OTP Memory Internal Registers Data Readout
0x3090~ 0x30AF	RSVD	–	–	Reserved
0x30B0	IO_CTRL0	0xFF	RW	IO Control 0 CY[7:0]
0x30B1	IO_CTRL1	0xEF	RW	IO Control 1 C_GP[1:0], C_VSYNC, C_STROBE, C_PCLK, C_HREF, CY[9:8]
0x30B2	IO_CTRL2	0x00	RW	IO Control 2 GPO_monitor, C_FREX, R_PAD[3:0]
0x30B3	RSVD	–	–	Reserved
0x30B4	DVP0	0x00	RW	GPO[3:0]
0x30B5	DVP1	0x00	R	Data Readout, DATR[7:0] = {4'b0, DI[1:0], GPI[1:0]}
0x30B6	DVP2	0x00	RW	–
0x30B7	DVP3	0x00	RW	–
0x30B8	DSPC0	0x00	RW	UV Adjust Setting Bit[7:0]: uvadj_k[7:0]
0x30B9	DSPC1	0x1F	RW	UV Adjust Setting Bit[4:0]: uvadj_offs[4:0]

table 7-1 system control registers (sheet 15 of 15)

address	register name	default value	R/W	description
0x30BA	DSPC2	0x00	RW	UV Adjust Setting Bit[3:0]: uvadj_gth1[3:0]
0x30BB	DSPC3	0x00	RW	UV Adjust Setting Bit[4:0]: uvadj_gth2[4:0]
0x30BC~ 0x30BE	RSVD	–	–	Reserved
0x30BF	DSPC7	0x00	RW	-
0x30C0~ 0x30DF	RSVD	–	–	Reserved

table 7-2 SC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3100	SC_CTRL0	0x00	RW	Bit[7:6]: Reserved Bit[5]: Format bypass Bit[4]: Compression mode enable Bit[3:2]: Reserved Bit[1]: MC power down Bit[0]: DSP power down
0x3101	RSVD	–	–	Reserved
0x3102	SC_CTRL2	0x00	RW	Bit[5]: DSP sensor/internal RGB gain control 0: DSP use internal RGB gain 1: DSP use sensor RGB gain
0x3103	RSVD	–	–	Reserved
0x3104	SC_SYN_CTRL0	0xEF	RW	Gated Reset0 Bit[7]: ISP_pad_rst Bit[6]: DSP_rst Bit[5]: CIF_ptn_rst Bit[4]: OUT_top_rst Bit[3]: Format_rst Bit[2]: OUT_rst_pclk Bit[1]: MC_top_rst Bit[0]: CIF_top_rst

table 7-2 SC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3105	SC_SYN_CTRL1	0x10	RW	Gated Clk0 Bit[7]: ISP_pad_clk Bit[6]: DSP_clk Bit[5]: CIF_ptn_clk Bit[4]: OUT_top_clk Bit[3]: Format_clk Bit[2]: OUT_pclk Bit[1]: MC_top_clk Bit[0]: CIF_top_clk
0x3106	SC_SYN_CTRL2	0xFD	RW	Gated Reset1 Bit[7]: CIF_pad_rst Bit[6]: RGB_dither_rst Bit[5]: YUV2RGB_rst Bit[4:3]: Reserved Bit[2]: CIF_ext_rst Bit[1]: SCCB_arb_rst Bit[0]: Compression_top_rst
0x3107	SC_SYN_CTRL3	0x02	RW	Gated Clk1 Bit[7]: Reserved Bit[6]: RGB_dither_clk Bit[5]: YUV2RGB_clk Bit[4:3]: Reserved Bit[2]: CIF_ext_clk Bit[1]: SCCB_arb_clk Bit[0]: Compression_top_clk

table 7-3 CIF control registers

address	register name	default value	R/W	description
0x3200	CIF_CTRL0	0x00	RW	Bit[7:5]: CIF_mode[2:0] 000: Internal sensor 010: External sensor Bit[4:0]: Reserved
0x3201~ 0x3203	RSVD	–	–	Reserved
0x3204	CIF_CTRL4	0x00	RW	Bit[7:6]: Reserved Bit[5]: Reverse input_PCLK Bit[4]: Reverse input_HREF Bit[3]: Reverse input_VSYNC Bit[2:0]: Reserved

table 7-4 DSP control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3300	DSP_CTRL_0	0x17	RW	Bit[7]: Reserved Bit[6]: OVLY_en Bit[5]: YUV422_IN_en Bit[4]: Reserved Bit[3]: BAR_en Bit[2]: Reserved Bit[1]: AFC_en Bit[0]: LENC_en
0x3301	DSP_CTRL_1	0xD6	RW	Bit[7]: Reserved Bit[6]: UV_avg_en Bit[5]: Reserved Bit[4]: CMX_en Bit[3]: Reserved Bit[2]: WC_en Bit[1]: BC_en Bit[0]: Reserved
0x3302	DSP_CTRL_2	0x4F	RW	Bit[7]: SDE_en Bit[6]: UV_adjust_en Bit[5]: Scale_en Bit[4]: Reserved Bit[3]: CIP_en Bit[2]: GMA_en Bit[1]: AWB_gain_en Bit[0]: AWB_en
0x3303	RSVD	–	–	Reserved
0x3304	DSP_CTRL_4	0xFC	RW	Bit[7]: CMX_Bias_On Bit[6]: CMX_Bias_plus Bit[5]: GMA_Bias_On ; Bit[4]: GMA_Bias_plus Bit[3]: LENC_Bias_On Bit[2]: LENC_Bias_plus Bit[1:0]: Out_sel 00: YUV444 01: RAW10_GMA 10: RAW8_CIP 11: RAW8_CMX
0x3305~ 0x3307	RSVD	–	–	Reserved
0x3308	AWB_CTRL_3	0xA5	RW	Bit[7]: AWB_SIMPLE 0: Advanced 1: Simple Bit[6:0]: Reserved
0x3309~ 0x331A	RSVD	–	–	Reserved

table 7-4 DSP control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x331B	YST1	0x02	RW	YST1[7:0]
0x331C	YST2	0x07	RW	YST2[7:0]
0x331D	YST3	0x1F	RW	YST3[7:0]
0x331E	YST4	0x49	RW	YST4[7:0]
0x331F	YST5	0x5A	RW	YST5[7:0]
0x3320	YST6	0x6A	RW	YST6[7:0]
0x3321	YST7	0x79	RW	YST7[7:0]
0x3322	YST8	0x87	RW	YST8[7:0]
0x3323	YST9	0x94	RW	YST9[7:0]
0x3324	YST10	0x9F	RW	YST10[7:0]
0x3325	YST11	0xAF	RW	YST11[7:0]
0x3326	YST12	0xBB	RW	YST12[7:0]
0x3327	YST13	0xCF	RW	YST13[7:0]
0x3328	YST14	0xDF	RW	YST14[7:0]
0x3329	YST15	0xEE	RW	YST15[7:0]
0x332A	YSLP15	0x18	RW	YSLP15[7:0]
0x332B	MISC_CTRL	0x00	RW	Bit[7:4]: Reserved Bit[3]: AWB_gain_man 0: Auto 1: Manual Bit[2:0]: Reserved
0x332C	DNS_TH	0x14	RW	DNS_TH_Manual[7:0]
0x332D	Y_EDGE_MT	0x6D	RW	Bit[7]: Up_8x Bit[6]: Dns_auto 0: Manual 1: Auto Bit[5]: Edge_auto 0: Manual 1: Auto Bit[4:0]: Y_EDGE_MT
0x332E	Y_EDGE_TH_TM	0x00	RW	Bit[7:6]: EDGE_SLP_MT Bit[5]: Reserved Bit[3:0]: Y_EDGE_TH_tm
0x332F	BASE1	0x0F	RW	Bit[7:6]: DNS_SLP_TH Bit[5]: Reserved Bit[4:0]: Base1

table 7-4 DSP control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3330	BASE2	0x81	RW	Bit[7:5]: Reserved Bit[4:0]: Base2
0x3331	OFFSET	0x10	RW	Bit[7:0]: Offset
0x3332~ 0x333E	RSVD	–	–	Reserved
0x333F	CMXSIGN_MISC	0x06	RW	Bit[7:2]: Reserved Bit[1]: CMXSIGN[8] for CMX_9 Bit[0]: Reserved
0x3340	CMX_1	0x20	RW	CMX_1[7:0]
0x3341	CMX_2	0x64	RW	CMX_2[7:0]
0x3342	CMX_3	0x08	RW	CMX_3[7:0]
0x3343	CMX_4	0x30	RW	CMX_4[7:0]
0x3344	CMX_5	0x90	RW	CMX_5[7:0]
0x3345	CMX_6	0xC0	RW	CMX_6[7:0]
0x3346	CMX_7	0xA0	RW	CMX_7[7:0]
0x3347	CMX_8	0x98	RW	CMX_8[7:0]
0x3348	CMX_9	0x08	RW	CMX_9[7:0]
0x3349	CMXSIGN	0x98	RW	CMXSIGN[7:0] for CMX_1 to CMX_8
0x334A~ 0x3353	RSVD	–	–	Reserved
0x3354	SGNSET	0x01	RW	Bit[7:6]: Reserved Bit[5:0]: SgnSet[5:0] Hue: Bit[5:4], Bit[1:0] U' =SGNST[4] (HueCos/0x80) × U + SGNSET[1] (HueSin/0x80) × V V' =SGNST[5] (HueCos/0x80) × V + SGNSET[0] (HueSin/0x80) × U YContrast: sign2: YOFFSET sign3: YBRIGHT
0x3355	SDE_CTRL	0x00	RW	SDE_Ctrl[7:0]
0x3356	HUE_COS	0x80	RW	Hue_cos[7:0]
0x3357	HUE_SIN	0x00	RW	Hue_sin[7:0]
0x3358	SAT_U	0x40	RW	Sat_u[7:0]
0x3359	SAT_V	0x40	RW	Sat_v[7:0]

table 7-4 DSP control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x335A	UREG	0x80	RW	Ureg[7:0]
0x335B	VREG	0x80	RW	Vreg[7:0]
0x335C	YOFFSET	0x00	RW	YOffset[7:0]
0x335D	YGAIN	0x20	RW	YGain[7:0]
0x335E	YBRIGHT	0x00	RW	YBright[7:0]
0x335F	SIZE_IN_MISC	0x68	RW	Bit[7]: Reserved Bit[6:4]: Vsize_In[10:8] Bit[3:0]: Hsize_In[11:8]
0x3360	HSIZE_IN_L	0x18	RW	Hsize_In[7:0]
0x3361	VSIZE_IN_L	0x0c	RW	Vsize_In[7:0]
0x3362	SIZE_OUT_MISC	0x68	RW	Bit[7]: Reserved Bit[6:4]: Vsize_Out[10:8] for zoom_out Bit[3:0]: Hsize_Out[11:8] for zoom_out
0x3363	HSIZE_OUT_L	0x18	RW	Hsize_Out[7:0] for zoom_out
0x3364	VSIZE_OUT_L	0x0C	RW	Vsize_Out[7:0] for zoom_out
0x3365~ 0x3366	RSVD	–	–	Reserved
0x3367	R_XY0	0x34	RW	Bit[7]: Reserved Bit[6:4]: R_Y0[10:8] Bit[3]: Reserved Bit[2:0]: R_X0[10:8]
0x3368	R_X0	0x0C	RW	R_X0[7:0]
0x3369	R_Y0	0x06	RW	R_Y0[7:0]
0x336A	R_A1	0x22	RW	R_A1[6:0]
0x336B	R_A2/B2	0x87	RW	Bit[7:4]: R_B2 Bit[3:0]: R_A2
0x336C	R_B1	0xC2	RW	R_B1[7:0]
0x336D	G_XY0	0x34	RW	Bit[7]: Reserved Bit[6:4]: G_Y0[10:8] Bit[3]: Reserved Bit[2:0]: G_X0[10:8]
0x336E	G_X0	0x0C	RW	G_X0[7:0]
0x336F	G_Y0	0x06	RW	G_Y0[7:0]

table 7-4 DSP control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x3370	G_A1	0x22	RW	G_A1[6:0]
0x3371	G_A2/B2	0x87	RW	Bit[7:4]: G_B2 Bit[3:0]: G_A2
0x3372	G_B1	0xC2	RW	G_B1[7:0]
0x3373	B_XY0	0x34	RW	Bit[7]: Reserved Bit[6:4]: B_Y0[10:8] Bit[3]: Reserved Bit[2:0]: B_X0[10:8]
0x3374	B_X0	0x0C	RW	B_X0[7:0]
0x3375	B_Y0	0x06	RW	B_Y0[7:0]
0x3376	B_A1	0x22	RW	B_A1[6:0]
0x3377	B_A2/B2	0x87	RW	Bit[7:4]: B_B2 Bit[3:0]: B_A2
0x3378	B_B1	0xC2	RW	B_B1[7:0]
0x3379~ 0x33A3	RSVD	–	–	Reserved
0x33A4	MISC_DCW_SIZE	0x68	RW	Bit[7]: Sat_v_switch 0: From sat_v 1: From sat_u Bit[6:4]: DCW_OV[10:8] Bit[3:0]: DCW_OH[11:8]
0x33A5	DCW_OH[7:0]	0x18	RW	DCW_OH[7:0]
0x33A6	DCW_OV[7:0]	0x0C	RW	DCW_OV[7:0]
0x33A7	R_GAIN_M	0x40	RW	AWB R manual Gain [7:0]
0x33A8	G_GAIN_M	0x40	RW	AWB G manual Gain [7:0]
0x33A9	B_GAIN_M	0x40	RW	AWB B manual Gain [7:0]
0x33AA	OVLY_MISC1	0x23	RW	Bit[7]: Reserved Bit[6:4]: OVLY_Top[10:8] Bit[3:0]: OVLY_Left[11:8]
0x33AB	OVLY_LEFT	0x6C	RW	OVLY_Left[7:0]
0x33AC	OVLY_TOP	0x91	RW	OVLY_Top[7:0]
0x33AD	OVLY_MISC2	0x34	RW	Bit[7]: Reserved Bit[6:4]: OVLY_Bottem[10:8] Bit[3:0]: OVLY_Right[11:8]
0x33AE	OVLY_RIGHT	0xAC	RW	OVLY_Right[7:0]

table 7-4 DSP control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x33AF	OVLY_BOTTEM	0x81	RW	OVLY_Bottem[7:0]
0x33B0	OVLY_MISC3	0x00	RW	Bit[7]: Reserved Bit[5:4]: OVLY_ext_width_V[9:8] Bit[3]: Reserved Bit[2:0]: OVLY_ext_width_H[10:8]
0x33B1	OVLY_EXT_WIDTH_H	0x14	RW	OVLY_ext_width_H[7:0]
0x33B2	OVLY_EXT_WIDTH_V	0x14	RW	OVLY_Ext_Width_V[7:0]
0x33B3	OVLY_Y	0x80	RW	OVLY_Y[7:0]
0x33B4	OVLY_U	0x2A	RW	OVLY_U[7:0]
0x33B5	OVLY_V	0x14	RW	OVLY_V[7:0]

table 7-5 FMT_MUX registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3400	FMT_MUX_CTRL0	0x04	RW	Bit[7:3]: Reserved Bit[2:0]: Fmt_sel 000: ISP YUV 001: ISP RGB 010: ISP YUV422 011: ISP RAW 100: Int CIF RAW 101: Ext CIF RAW 110: Ext CIF YUV422 bypass
0x3401~0x3402	RSVD	–	–	Reserved
0x3403	ISP_PAD_CTR2	0x00	RW	Bit[7:4]: X start Bit[3:0]: Y start

table 7-5 FMT_MUX registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3404	FMT_CTRL00	0x02	RW	Bit[7] UV_sel 0: Use UV_avg, Y 1: Use U0Y0, V0Y1 Bit[6]: YUV422_in 0: Input to FORMAT is raw data 1: Input to FORMAT is YUV422 data when bypassing FORMAT Bit[5:0]: YUV422: 0x00: yuyvyuyv..../yuyvyuyv.... 0x01: yvyuyvyu..../yvyuyvyu.... 0x02: uyvyuyvy..../uyvyuyvy.... 0x03: vyuyvyuy..../vyuyvyuy.... YUV420: 0x04: yyyy..../yuyvyuyv.... 0x05: yyyy..../yvyuyvyu.... 0x06: yyyy..../uyvyuyvy.... 0x07: yyyy..../vyuyvyuy.... 0x08: yuyvyuyv..../yyyy.... 0x09: yvyuyvyu..../yyyy.... 0x0A: uyvyuyvy..../yyyy.... 0x0B: vyuyvyuy..../yyyy.... 0x0C: uyyuyy..../vyyvyy Y8: 0x0D: yyyy..../yyyy.... YUV444(RGB888): 0x0E: yuvyuv..../yuvyuv.... (gbrgbr..../gbrgbr....) 0x0F: yvuyvu..../yvuyvu.... (grbgrb..../grbgrb....) 0x1C: uyvuyv..../uyvuyv.... (bgrbgr..../bgrbgr....) 0x1D: vyuvyu..../vyuvyu.... (rgbrgb..../rgbrgb....) 0x1E: uvyuvy..../uvyuvy.... (brgbrg..../brgbrg....) 0x1F: vuyvuy..../vuyvuy.... (rbgrbg..../rbgrbg....) RGB565: 0x10: {b[4:0],g[5:3]}, {g[2:0],r[4:0]} 0x11: {r[4:0],g[5:3]}, {g[2:0],b[4:0]} 0x30: {g[2:0],b[4:0]}, {r[4:0],g[5:3]} (MIPI RGB565)

table 7-5 FMT_MUX registers (sheet 3 of 3)

address	register name	default value	R/W	description
				RGB555: 0x12: {b[4:0],g[4:2]}, {g[1:0],1'b0,r[4:0]} 0x13: {r[4:0],g[4:2]}, {g[1:0],1'b0,b[4:0] 0x32: {g[1:0],1'b0,b[4:0]}, {r[4:0],g[4:2]} (MIPI RGB555) RGB444: 0x14:{b[3:0],1'b0,g[3:1]}, {g[0],2'h0,r[3:0],1'b0} 0x15:{r[3:0],1'b0,g[3:1]}, {g[0],2'h0,b[3:0],1'b0} 0x34:{g[0],2'h0,b[3:0],1'b0}, {r[3:0],1'b0,g[3:1]} (MIPI RGB444) 0x37:{4'b0,r[3:0]}, {g[3:0],b[3:0]} 0x38:{4'b0,b[3:0]}, {g[3:0],r[3:0]} 0x16: {b[3:0],g[3:0]}, {r[3:0],b[3:0]} ... 0x17: {r[3:0],g[3:0]}, {b[3:0],r[3:0]} ... Raw: 0x18:bgbg..../grgr.... 0x19:gbgb..../rgrg.... 0x1A:grgr..../bgbg.... 0x1B:rgrg..../gbgb....
0x3405	DITHER_CTRL0	0x40	RW	Bit[6]: Dither_sel 0: Use register seting 1: Follow with fmt_control Bit[5:4]: R_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[3:2]: G_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit Bit[1:0]: B_dithering 00: No 01: 4-bit 10: 5-bit 11: 6-bit

table 7-6 OUT_TOP control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3600	OUT_CTRL00	0xC0	RW	Bit[7]: VSYNC_sel2 1: VSYNC mode 3 select Bit[6]: VSYNC_gate Gate DVP_PCLK when VSYNC and PCLK_gate_en Bit[5]: Reserved Bit[4]: PCLK_pol Bit[3]: HREF_pol Bit[2]: VSYNC_pol Bit[1]: VSYNC_sel 0: VSYNC mode 1 select 1: VSYNC mode 2 select Bit[0]: Data_order 0: DVP output DVP_data[9:0] 1: DVP output DVP_data[0:9]
0x3601	OUT_CTRL01	0x01	RW	Bit[7]: PCLK_gate_en 1: Gate DVP_PCLK when no data transfer Bit[6:5]: Reserved Bit[4]: CCIR656_en Bit[3:0]: Reserved
0x3602	OUT_CTRL02	0x22	RW	Bit[7:5]: Reserved Bit[4]: DVP_disable Bit[3:0]: Reserved
0x3603~ 0x3607	RSVD	–	–	Reserved
0x3608	OUT_CTRL08	0x80	RW	Bit[7:4]: HREF_dly HREF delay PCLK2x number after VYSNC goes high when JFIFO overflow Bit[3:0]: Reserved
0x3609	OUT_CTRL09	0x80	RW	Bit[7:0]: VSYNC_width VSYNC_width_real = VSYNC_width × 16
0x360A	OUT_CTRL0A	0x10	RW	Bit[7:0]: HSYNC_dly Delay between the first HSYNC_HREF and HREF_int
0x360B	OUT_CTRL0B	0x02	RW	Bit[7:0]: hl_size Line blanking time/8
0x360C	RSVD	–	–	Reserved

table 7-6 OUT_TOP control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x360D	OUT_CTRL0D	0x5E	RW	Bit[7]: tst_bit8 0: 10-bit mode 1: Test mode 8-bit mode Bit[6:0]: Reserved
0x360E~ 0x360F	RSVD	–	–	Reserved
0x3610	WIDTH_CTRL	0x40	RW	Bit[7:0]: Width_man[7:0]/4
0x3611	OUT_CTRL11	0x0C	RW	Bit[7:5]: width_man[10:8], Width_man_real = width_man × 4 Bit[4:0]: Reserved
0x3612~ 0x3613	RSVD	–	–	Reserved
0x3614	CLIP_MIN	0x00	RW	Bit[7:0]: Clip_min Clipping min value
0x3615	CLIP_MAX	0xFF	RW	Bit[7:0]: Clip_max Clipping max_value
0x3616	OUT_CTRL16	0x0C	RW	Bit[7:4]: Reserved Bit[3:2]: clip_max[1:0] Bit[1:0]: clip_min[1:0]
0x3617~ 0x361C	RSVD	–	–	Reserved
0x361D	OUT_CTRL1D	0x50	RW	Bit[7:2]: Reserved Bit[1:0]: Test pattern select 00: No test pattern 01: Test pattern 1 10: Test pattern 2
0x361E	OUT_CTRL1E	0x33	RW	Bit[7]: height_sel 0: Select height_in 1: Select height_man Bit[6:0]: Reserved
0x361F~ 0x363B	RSVD	–	–	Reserved
0x363C	OUT_CTRL3C	0x04	RW	Bit[7]: Reserved Bit[6:5]: h2v_dly HREF to VSYNC delay for VSYNC mode 2 Bit[4:3]: v2h_dly VSYNC to HREF delay for DVP mode Bit[2:0]: Reserved

table 7-6 OUT_TOP control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x363D	OUT_CTRL3D	0x60	RW	Bit[7]: DVP_H 0: Output DVP_data[9:0] 1: Output DVP_data{7:0,9:8} Bit[6]: Compression_pad_en 1: Pad pixels to meet width_man Bit[5:4]: Reserved Bit[3]: DVP_L 0: Select DVP_data[9:2] when DVP 8-bit mode 1: Select DVP_data[7:0] Bit[2:0]: Compression_mode 000: Mode 0 001: Mode 1 010: Mode 2 011: Mode 3 100: Mode 4 101-111:Reserved
0x363E	OUT_CTRL3E	0x00	RW	Bit[7:0]: EOF2v_dly_h Width VSYNC_sel2, after frame end, VSYNC will be high after EOF2v_dly DVP_PCLK cycles
0x363F	OUT_CTRL3F	0x01	RW	Bit[7:0]: EOF2v_dly_m Width VSYNC_sel2, after frame end, vsync will be high after EOF2v_dly DVP_PCLK cycles
0x3640	OUT_CTRL40	0x00	RW	Bit[7:0]: EOF2v_dly_l Width VSYNC_sel2, after frame end, VSYNC will be high after EOF2v_dly DVP_PCLK cycles
0x3641~ 0x3642	RSVD	–	–	Reserved
0x3643	OUT_CTRL43	0xFF	RW	Bit[7:0]: Line_length_h
0x3644	OUT_CTRL44	0xFF	RW	Bit[7:0]: Line_length_l
0x3645	RSVD	–	–	Reserved
0x3646	OUT_CTRL46	0x09	RW	HSYNC Control Bit[7]: Reserved Bit[6]: HSYNC_en - enable HSYNC mode for DVP, MIPI is disabled Bit[5:2]: Reserved Bit[1]: line_length_sel 0: Auto calculate line_length 1: Select line_length Bit[0]: Reserved

table 7-7 MC control registers

address	register name	default value	R/W	description
0x3700	INTR_MASK0	0xFF	RW	INTR_MASK0 MCU interrupt0 mask (0: enable interrupt; 1: mask interrupt) Bit[7]: Interrupt0 mask[7] Bit[6]: Interrupt0 mask[6] Bit[5]: Interrupt0 mask[5] Bit[4]: Interrupt0 mask[4] Bit[3]: Interrupt0 mask[3] Bit[2]: Interrupt0 mask[2] Bit[1]: Interrupt0 mask[1] Bit[0]: Interrupt0 mask[0]
0x3701	INTR_MASK1	0xFF	RW	INTR_MASK1 MCU interrupt1 mask (0: enable interrupt; 1: mask interrupt) Bit[7]: Interrupt1 mask[7] Bit[6]: Interrupt1 mask[6] Bit[5]: Interrupt1 mask[5] Bit[4]: Interrupt1 mask[4] Bit[3]: Interrupt1 mask[3] Bit[2]: Interrupt1 mask[2] Bit[1]: Interrupt1 mask[1] Bit[0]: Interrupt1 mask[0]
0x3702~ 0x3707	RSVD	–	–	Reserved
0x3708	INTR0	0x00	R	MCU Interrupt 0 Bit[7]: Interrupt 0[7] Bit[6]: Interrupt 0[6] Bit[5]: Interrupt 0[5] Bit[4]: Interrupt 0[4] Bit[3]: Interrupt 0[3] Bit[2]: Interrupt 0[2] Bit[1]: Interrupt 0[1] Bit[0]: Interrupt 0[0]
0x3709	INTR1	0x00	R	MCU Interrupt 1 Bit[7]: Interrupt 1[7] Bit[6]: Interrupt 1[6] Bit[5]: Interrupt 1[5] Bit[4]: Interrupt 1[4] Bit[3]: Interrupt 1[3] Bit[2]: Interrupt 1[2] Bit[1]: Interrupt 1[1] Bit[0]: Interrupt 1[0]

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
stable operating temperature		0°C to +50°C
operating temerature		-20°C to +70°C
ambient storage temperature		-40°C to +95°C
ambient humidity		TBD
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V

a. Exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device.

table 8-2 DC characteristics (-20°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.5	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.425	1.5	1.575	V
V_{DD-IO}	supply voltage (digital I/O)	1.71	1.8	3.0	V
I_{DD-A}	active (operating) current	TBD	TBD	TBD	mA
I_{DD-D}		TBD	TBD	TBD	mA
I_{DD-IO}		TBD	TBD	TBD	mA
$I_{DDS-SCCB}$	standby current	TBD	TBD	TBD	mA
$I_{DDS-PWDN}$		TBD	TBD	TBD	µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.5V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[a]	SCL and SDA	-0.5	0	0.54	V
V_{IH}[a]	SCL and SDA	1.26	1.8	2.3	V

a. Based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 2.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		30		MHz
DLE	DC differential linearity error		0.5		LSB
ILE	DC integral linearity error		1		LSB
	setting time for hardware reset			<1	ms
	setting time for software reset			<1	ms
	setting time for UXGA/SVGA mode change			<1	ms
	setting time for register setting			<300	ms
digital inputs					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.26	1.8	2.3	V

table 8-4 timing characteristics

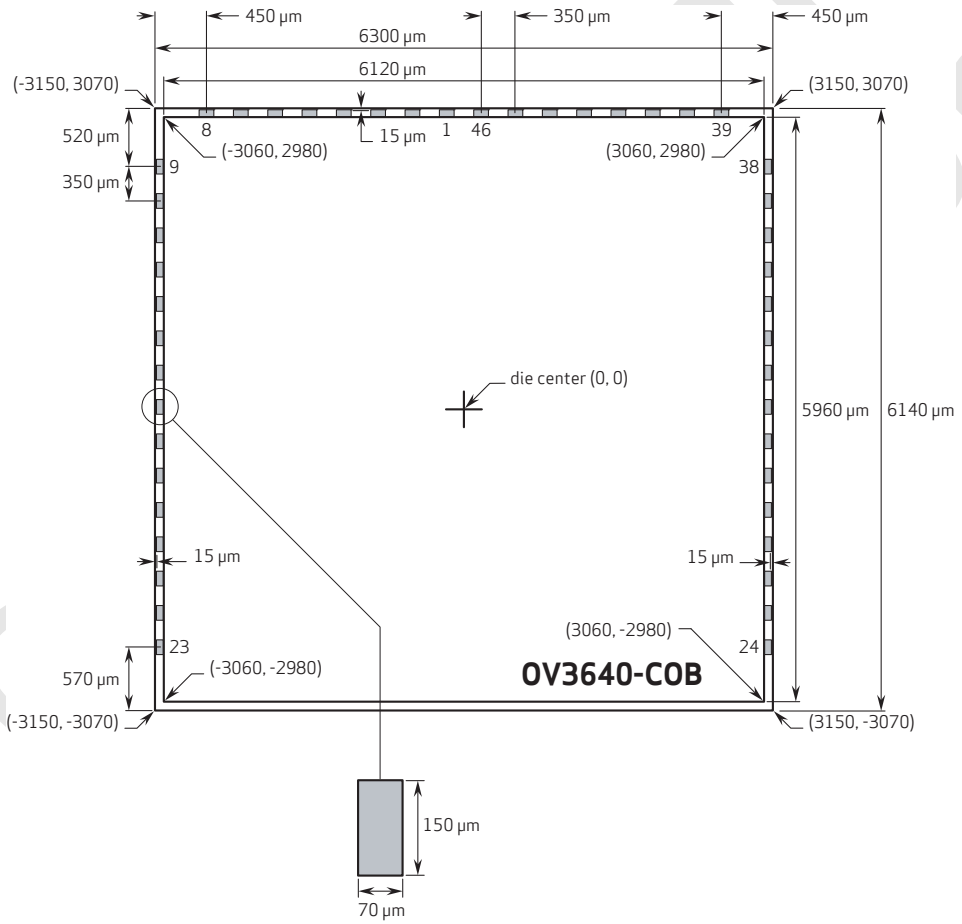
symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 die specifications



note 1 all dimensions and coordinates are in µm.

3640_COB_DS_9_1

table 9-1 pad location coordinates (sheet 1 of 2)

pad number	pad name	x coordinate	y coordinate	x pitch	y pitch	pad size
01	SGND	-175	3020			150 x 70
02	SVDD	-525	3020	-350	0	150 x 70
03	FREX	-875	3020	-350	0	150 x 70
04	STROBE	-1225	3020	-350	0	150 x 70
05	VSYNC	-1575	3020	-350	0	150 x 70
06	AVDD	-1925	3020	-350	0	150 x 70
07	AGND	-2275	3020	-350	0	150 x 70
08	HREF	-2625	3020	-350	0	150 x 70
09	DATA9	-3100	2475	-475	-545	70 x 150
10	DATA8	-3100	2125	0	-350	70 x 150
11	DATA7	-3100	1775	0	-350	70 x 150
12	DATA6	-3100	1425	0	-350	70 x 150
13	DATA5	-3100	1075	0	-350	70 x 150
14	DATA4	-3100	725	0	-350	70 x 150
15	DATA3	-3100	375	0	-350	70 x 150
16	DATA2	-3100	25	0	-350	70 x 150
17	DATA1	-3100	-325	0	-350	70 x 150
18	DATA0	-3100	-675	0	-350	70 x 150
19	DOVDD	-3100	-1025	0	-350	70 x 150
20	DOGND	-3100	-1375	0	-350	70 x 150
21	PCLK	-3100	-1725	0	-350	70 x 150
22	DVDD	-3100	-2075	0	-350	70 x 150
23	DGND	-3100	-2425	0	-350	70 x 150
24	DGND	3100	-2425	6200	0	70 x 150
25	DVDD	3100	-2075	0	350	70 x 150
26	DOVDD	3100	-1725	0	350	70 x 150
27	DOVDD	3100	-1375	0	350	70 x 150
28	GPIO2	3100	-1025	0	350	70 x 150
29	DOGND	3100	-675	0	350	70 x 150

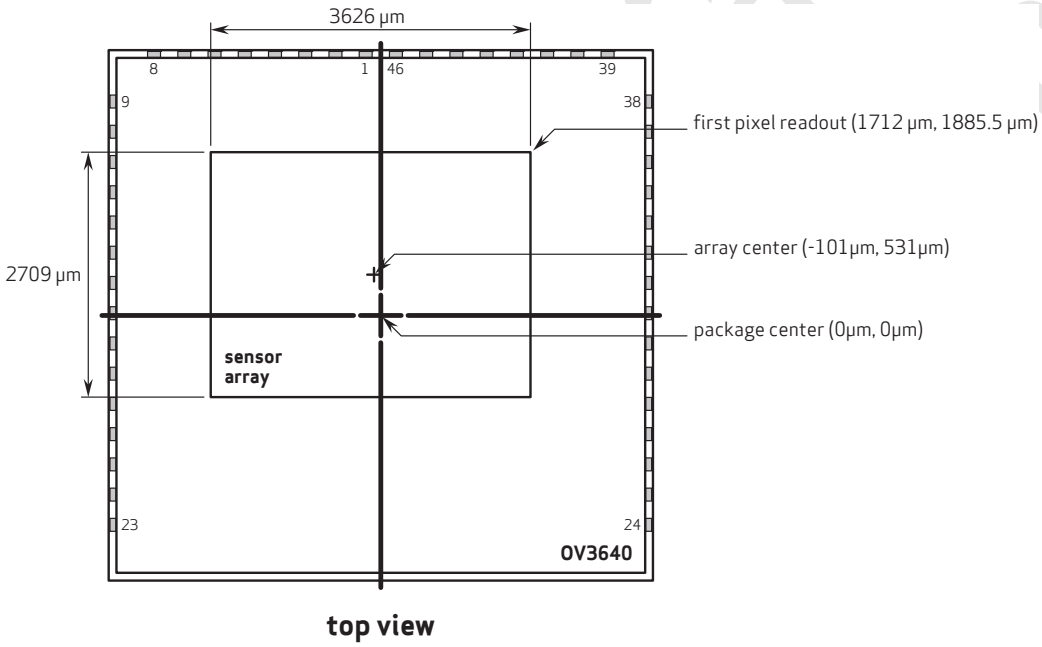
table 9-1 pad location coordinates (sheet 2 of 2)

pad number	pad name	x coordinate	y coordinate	x pitch	y pitch	pad size
30	MDP2	3100	-325	0	350	70 x 150
31	MDN2	3100	25	0	350	70 x 150
32	MCP	3100	375	0	350	70 x 150
33	MCN	3100	725	0	350	70 x 150
34	EVDD	3100	1075	0	350	70 x 150
35	EGND	3100	1425	0	350	70 x 150
36	MDP1	3100	1775	0	350	70 x 150
37	MDN1	3100	2125	0	350	70 x 150
38	EGND	3100	2475	0	350	70 x 150
39	GPIO1	2625	3020	-475	545	150 x 70
40	XVCLK	2275	3020	-350	0	150 x 70
41	VREFN	1925	3020	-350	0	150 x 70
42	VREFH	1575	3020	-350	0	150 x 70
43	SCL	1225	3020	-350	0	150 x 70
44	SDA	875	3020	-350	0	150 x 70
45	RESET_B	525	3020	-350	0	150 x 70
46	PWDN	175	3020	-350	0	150 x 70

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

3640_COB_DS_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

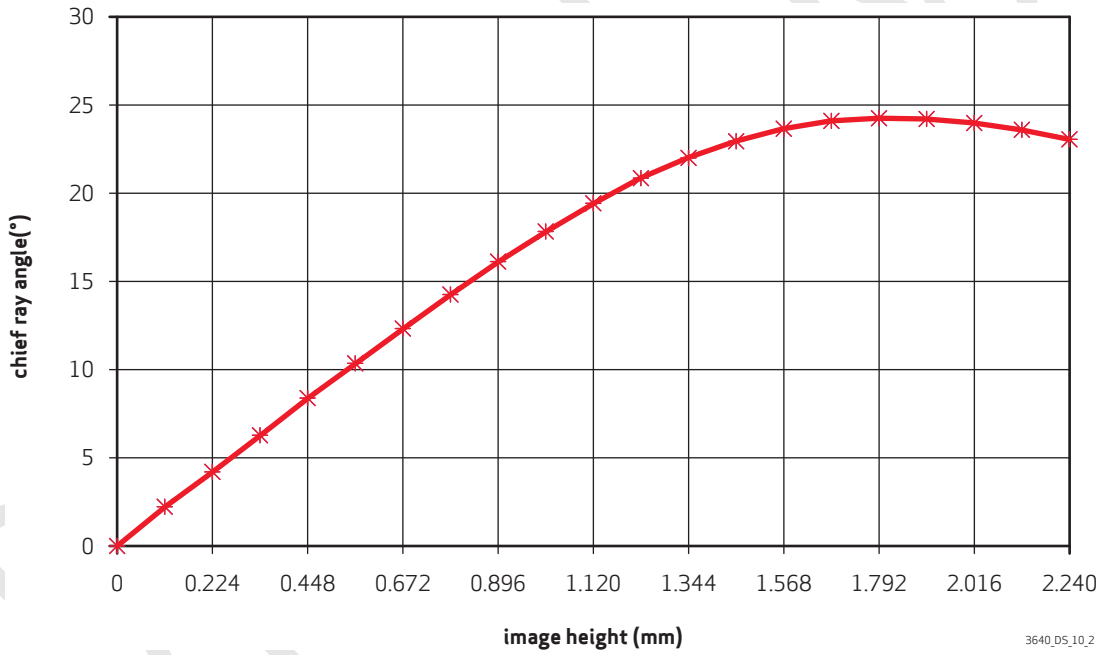


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0	0
0.05	0.112	2.18
0.1	0.224	4.2
0.15	0.336	6.28
0.2	0.448	8.34
0.25	0.56	10.36
0.3	0.672	12.35
0.35	0.784	14.28
0.4	0.896	16.13
0.45	1.008	17.86

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	1.12	19.45
0.55	1.232	20.85
0.6	1.344	22.03
0.65	1.456	22.98
0.7	1.568	23.67
0.75	1.68	24.11
0.8	1.792	24.29
0.85	1.904	24.24
0.9	2.016	23.99
0.95	2.128	23.6
1	2.24	23.07

the clear advantage™

OmniVision Technologies, Inc.

UNITED STATES

1341 Orleans Drive
Sunnyvale, CA 94089

tel: + 1 408 542 3000

fax: + 1 408 542 3001

email: salesamerican@ovt.xom

Indianapolis + 1 317 297 7240

Philadelphia + 1 610 688 3436

UNITED KINGDOM

Hampshire + 44 1256 744 610

FINLAND

Nokia + 358 3 341 1898

CHINA

Beijing + 86 10 6580 1690

Shanghai + 86 21 6105 5100

Shenzhen + 86 755 8384 9733

Hong Kong + 852 2403 4011

JAPAN

Tokyo + 81 3 5765 6321

KOREA

Seoul + 82 2 3478 2812

SINGAPORE + 65 6562 8250

TAIWAN

Taipei + 886 2 2657 9800 - ext.#100

website: **www.ovt.com**