

## Features

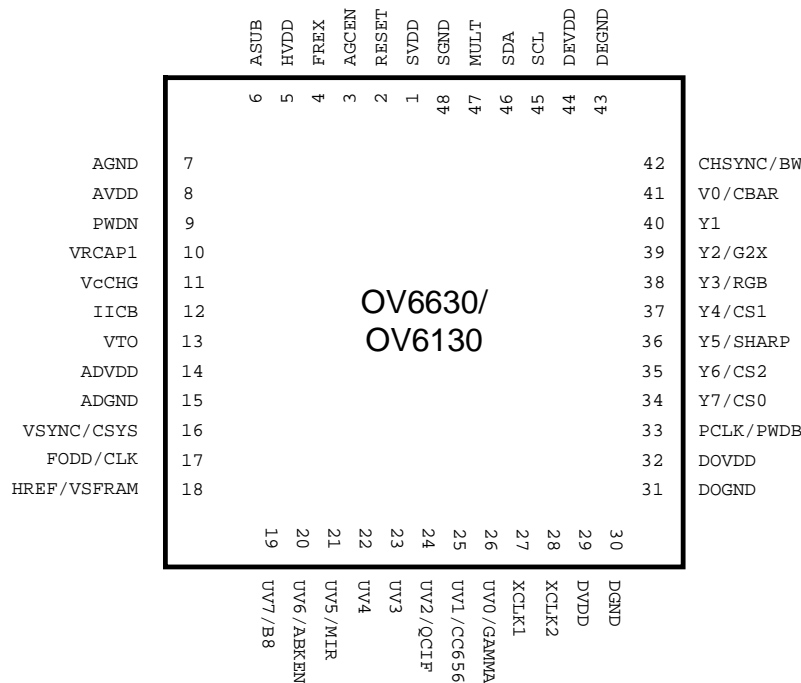
- 101,376 pixels, 1/4" lens, CIF/QCIF format
- Progressive scan read out
- Data format - YCrCb 4:2:2, GRB 4:2:2, RGB Raw Data
- 8/16 bit video data: ITU-601, ITU-656, ZV port
- Wide dynamic range, anti-blooming, zero smearing
- Electronic exposure/gain/white balance control
- Image enhancement - brightness, contrast, gamma, saturation, sharpness, window, etc.
- Internal/external synchronization
- Frame exposure/line exposure option
- 3.3-Volt operation, low power dissipation
  - < 20 mA active power
  - < 10  $\mu$ A in power-save mode
- Gamma correction (0.45/0.55/1.00)
- I<sup>2</sup>C programmable (400 kb/s):
  - Color saturation, brightness, contrast, white balance, exposure time, gain

## General Description

The OV6630 (color) and OV6130 (black and white) CMOS Image sensors are single-chip video/imaging camera devices designed to provide a high level of functionality in a single, small-footprint package. Both devices incorporate a 352 x 288 image array capable of operating up to 60 frames per second image capture. Proprietary sensor technology utilizes advanced algorithms to cancel Fixed Pattern Noise (FPN), eliminate

smearing, and drastically reduce blooming. All needed camera functions including exposure control, gamma, gain, white balance, color matrix, windowing, and more, are programmable through an I<sup>2</sup>C interface. Both devices can be programmed to provide image output in 4-bit, 8-bit or 16-bit digital formats.

Applications include: Video Conferencing, Video Phone, Video Mail, Still Image, and PC Multimedia.



|                                  |  |
|----------------------------------|--|
| <b>Array Element(CIF)(QCIF)</b>  | 356x292<br>(176x144)                               |
| <b>Pixel Size</b>                | 9 $\mu$ m x 8.2 $\mu$ m                            |
| <b>Image Area</b>                | 3.1mm x 2.5mm                                      |
| <b>Max Frames/Sec</b>            | Up to 60 FPS                                       |
| <b>Electronics Exposure</b>      | Up to 500:1 (for selected FPS)                     |
| <b>Scan Mode</b>                 | Progressive  |
| <b>Gamma Correction</b>          | 0.45/0.55/1.0                                      |
| <b>Min. Illumination (3000K)</b> | OV6630 - < 3lux @ f1.2<br>OV6130 - < 0.5lux @ f1.2 |
| <b>S/N Ration</b>                | > 48 dB<br>(AGC off, Gamma=1)                      |
| <b>FPN</b>                       | < 0.03% V <sub>PP</sub>                            |
| <b>Dark Current</b>              | < 0.2nA/cm <sup>2</sup>                            |
| <b>Dynamic Range</b>             | > 72 dB  |
| <b>Power Supply</b>              | 2.7-3.6VDC<br>5VDC/3.3VDC (DIO)                    |
| <b>Power Requirements</b>        | < 20mA active<br>< 10 $\mu$ A Standby              |
| <b>Package</b>                   | 48 pin LCC   |

**Figure 1. OV6630/OV6130 Pin Assignments**

Note: Outputs UV0-UV7 are not available on the OV6130. The inputs associated with these respective pins are still functional.

**Table 1. Pin Description**

| Pin No. | Name               | Pin Type                | Function/Description  |
|---------|--------------------|-------------------------|---|
| 01      | SVDD               | V <sub>IN</sub>         | Array power (+3.3VDC)   |
| 02      | RESET              | Function<br>(Default=0) | Chip reset, active high   |
| 03      | AGCEN              | Function<br>(Default=0) | Automatic Gain Control (AGC) selection<br>"0" – Disable AGC<br>"1" – Enable AGC<br><i>Note: This function is disabled when OV6630/OV6130 sensor is configured in I<sup>2</sup>C mode.</i> |
| 04      | FREX               | Function<br>(Default=0) | Frame exposure control<br>"0" – Disable frame exposure control<br>"1" – Enable frame exposure control   |
| 05      | HVDD               | V <sub>REF</sub> (4V)   | Charge pump voltage. Connect to ground through 10µF capacitor.  |
| 06      | ASUB               | V <sub>IN</sub>         | Analog substrate voltage.   |
| 07      | AGND               | V <sub>IN</sub>         | Analog ground   |
| 08      | AVDD               | V <sub>IN</sub>         | Analog power supply (+3.3VDC)   |
| 09      | PWDN               | Function<br>(Default=0) | Power down mode selection.<br>"0" – Normal mode.<br>"1" – Power down mode.  |
| 10      | VRCAP1             | V <sub>REF</sub> (1.5V) | Array reference. Connect to ground through 0.1µF capacitor.   |
| 11      | V <sub>C</sub> CHG | V <sub>REF</sub> (2.7V) | Internal voltage reference. Connect to ground through 1µF capacitor.  |
| 12      | IICB               | Function<br>(Default=0) | I <sup>2</sup> C enable selection.<br>"0" – Enable I <sup>2</sup> C<br>"1" – Enable auto-control mode   |
| 13      | VTO                | O                       | Luminance composite signal output (black/white in PAL standard).  |
| 14      | ADVDD              | V <sub>IN</sub>         | Analog power supply (+3.3VDC)   |
| 15      | ADGND              | V <sub>IN</sub>         | Analog signal ground  |
| 16      | VSYNC/CSYS         | I/O                     | Vertical sync output. At power up, read as CSYS.  |
| 17      | FODD/CLK           | I/O                     | Field ID FODD output or main clock output   |
| 18      | HREF/VSFRAM        | I/O                     | HREF output. At power up, read as VSFRAM  |
| 19      | *UV7/B8            | I/O                     | Bit 7 of U video component output. At power up, sampled as B8.<br><i>* Note: Output UV7 is not available on the OV6130 sensor.</i>  |
| 20      | *UV6/ABKEN         | I/O                     | Bit 6 of U video component output. At power up, sampled as ABKEN.<br><i>* Note: Output UV6 is not available on the OV6130 sensor.</i>   |
| 21      | *UV5/MIR           | I/O                     | Bit 5 of U video component output. At power up, sampled as MIR.<br><i>* Note: Output UV5 is not available on the OV6130 sensor.</i>   |
| 22      | *UV4               | I/O                     | Bit 4 of U video component output.<br><i>* Note: Output UV4 is not available on the OV6130 sensor.</i>  |
| 23      | *UV3               | I/O                     | Bit 3 of U video component output.<br><i>* Note: Output UV3 is not available on the OV6130 sensor.</i>  |
| 24      | *UV2/QCIF          | I/O                     | Bit 2 of U video component output. At power up, sampled as QCIF.<br><i>* Note: Output UV2 is not available on the OV6130 sensor.</i>  |
| 25      | *UV1/CC656         | I/O                     | Bit 1 of U video component output. At power up, sampled as CC656.<br><i>* Note: Output UV1 is not available on the OV6130 sensor.</i>   |
| 26      | *UV0/GAMMA         | I/O                     | Bit 0 of U video component output. At power up, sampled as GAMMA.<br><i>* Note: Output UV0 is not available on the OV6130 sensor.</i>   |
| 27      | XCLK1              | I                       | Crystal clock input   |
| 28      | XCLK2              | O                       | Crystal clock output  |
| 29      | DVDD               | V <sub>IN</sub>         | Digital power supply (+3.3VDC)  |
| 30      | DGND               | V <sub>IN</sub>         | Digital ground  |
| 31      | DOGND              | V <sub>IN</sub>         | Digital interface output buffer ground  |
| 32      | DOVDD              | V <sub>IN</sub>         | Digital interface output buffer power supply (+3.3VDC or 5VDC)  |
| 33      | PCLK/PWDB          | I/O                     | PCLK output. At power up sampled as PWDB.   |
| 34      | Y7/CS0             | I/O                     | Bit 7 of Y video component output. At power up, sampled as CS0.   |
| 35      | Y6/CS2             | I/O                     | Bit 6 of Y video component output. At power up, sampled as CS2.   |
| 36      | Y5/SHARP           | I/O                     | Bit 5 of Y video component output. At power up, sampled as SHARP.   |
| 37      | Y4/CS1             | I/O                     | Bit 4 of Y video component output. At power up, sampled as CS1.   |
| 38      | Y3/RGB             | I/O                     | Bit 3 of Y video component output. At power up, sampled as RGB.   |

|    |           |                         |  |
|----|-----------|-------------------------|--|
| 39 | Y2/G2X    | I/O                     | Bit 2 of Y video component output. At power up, sampled as G2X.  |
| 40 | Y1        | I/O                     | Bit 1 of Y video component output.   |
| 41 | Y0/CBAR   | I/O                     | Bit 0 of Y video component output. At power up, sampled as CBAR.                                       |
| 42 | CHSYNC/BW | I/O                     | CHSYNC output. At power up, sampled as BW.   |
| 43 | DEGND     | V <sub>IN</sub>         | Decoder ground.  |
| 44 | DEVDD     | V <sub>IN</sub>         | Decoder power supply (+3.3VDC)   |
| 45 | SCL       | I                       | I <sup>2</sup> C serial interface clock input.   |
| 46 | SDA       | I/O                     | I <sup>2</sup> C serial interface data input and output.   |
| 47 | MULT      | Function<br>(Default=0) | I <sup>2</sup> C slave selection<br>"0" – Select single slave ID.<br>"1" – Enable multiple (8) slaves. |
| 48 | SGND      | V <sub>IN</sub>         | Array ground   |

## 1 Function Description

(Note: References to color features do not apply to the OV6130 B&W Digital Image Sensor.)

### 1.1 Overview

Referring to Figure 2 below, the OV6630 sensor includes a 356 x 292 resolution image array, an analog signal processor, dual 8-bit A/D converters, analog video multiplexer, digital data formatter, video port, I<sup>2</sup>C interface, registers, and digital controls that include timing block, exposure control, black level control, and white balance.

The OV6630/OV6130 sensor is a 1/4 inch CMOS imaging device. The sensor contains approximately 101,376 pixels. Its design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read out scheme. The color filter of the sensor consists of a primary color RG/GB array arranged in line-alternating fashion.

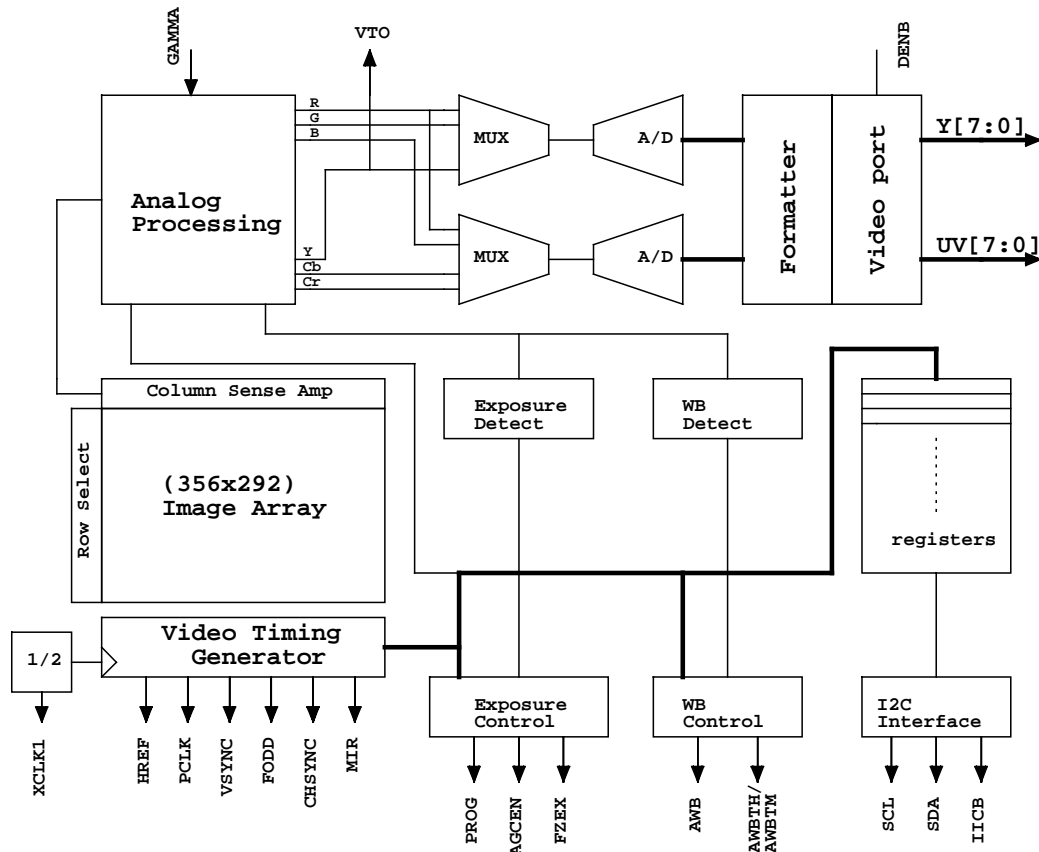


Figure 2. OV6630/OV6130 CMOS Image Sensor Block Diagram

## 1.2 Analog Processor Circuits

### 1.2.1 Overview

The image is captured by the 356 x 292 pixel image array and routed to the analog processing section where the majority of signal processing occurs. This block contains the circuitry that performs color separation, color correction, automatic gain control (AGC), gamma correction, color balance, black level calibration, “knee” smoothing, aperture correction, controls for picture luminance and chrominance, and anti-alias filtering. The analog video signals are based on the following formula:

$$Y = 0.59G + 0.31R + 0.11B$$

$$U = R - Y$$

$$V = B - Y$$

Where *R,G,B* are the equivalent color components in each pixel.

YCrCb format is also supported, based on the formula below:

$$Y = 0.59G + 0.31R + 0.11B$$

$$Cr = 0.713 (R - Y)$$

$$Cb = 0.564 (B - Y)$$

The YCrCb/RGB data signal from the analog processing section is fed to two on-chip 8-bit analog-to-digital (A/D) converters: one for the Y/RG channel and one shared by the CrCb/BG channels. The converted data stream is further conditioned in the digital formatter. The processed signal is delivered to the digital video port through the video multiplexer which routes the user-selected 16-, 8-, or 4-bit video data to the correct output pins.

The on-chip 8-bit A/D operates up to 9 MHz, and fully synchronous to the pixel rate. Actual conversion rate is related to the frame rate. A/D black-level calibration circuitry ensures:

- ⇒ The black level of Y/RGB is normalized to a value of 16
- ⇒ The peak white level is limited to 240
- ⇒ CrCb black level is 128
- ⇒ CrCb Peak/bottom is 240/16
- ⇒ RGB raw data output range is 16/240

(Note: Values 0 and 255 are reserved for sync flag)

### 1.2.2 Image Processing

The algorithm used for the electronic exposure control is based on the brightness of the full image. The exposure is optimized for a “normal” scene that assumes the subject is well lit relative to the background. In situations where the image is not well lit, the automatic exposure control (AEC) white/black ratio may be adjusted to suit the needs of the application.

Additional on-chip functions include

- ⇒ AGC that provides a gain boost of up to 24dB
- ⇒ White balance control that enables setting of proper color temperature and can be programmed for automatic or manual operation.
- ⇒ Separate saturation, brightness, contrast, and sharpness adjustments allow for further fine-tuning of the picture quality and characteristics.

The OV6630 image sensor also provides control over the White Balance ratio for increasing/decreasing the image field Red/Blue component ratio. The sensor provides a default setting that may be sufficient for many applications.

### 1.2.3 Windowing

The windowing feature of the OV6630/OV6130 image sensors allows user-definable window sizing as required by the application. Window size setting (in pixels) ranges from 2 x 2 to 356 x 292, and can be positioned anywhere inside the 356 x 292 boundary. Note that modifying window size and/or position does not change frame or data rate. The OV6630/OV6130 imager alters the assertion of the HREF signal to be consistent with the programmed horizontal and vertical region. The default output window is 352 x 288.

### 1.2.4 Zoom Video Port (ZV)

The OV6630/OV6130 image sensor includes a Zoom Video (ZV) function that supports standard ZV Port interface timing. Signals available include VSYNC, CHSYNC, PCLK and 16-bit data bus: Y[7:0] and UV[7:0]. The rising edge of PCLK clocks data into the ZV port. See Figure 3. Zoom Video Port Timing below.

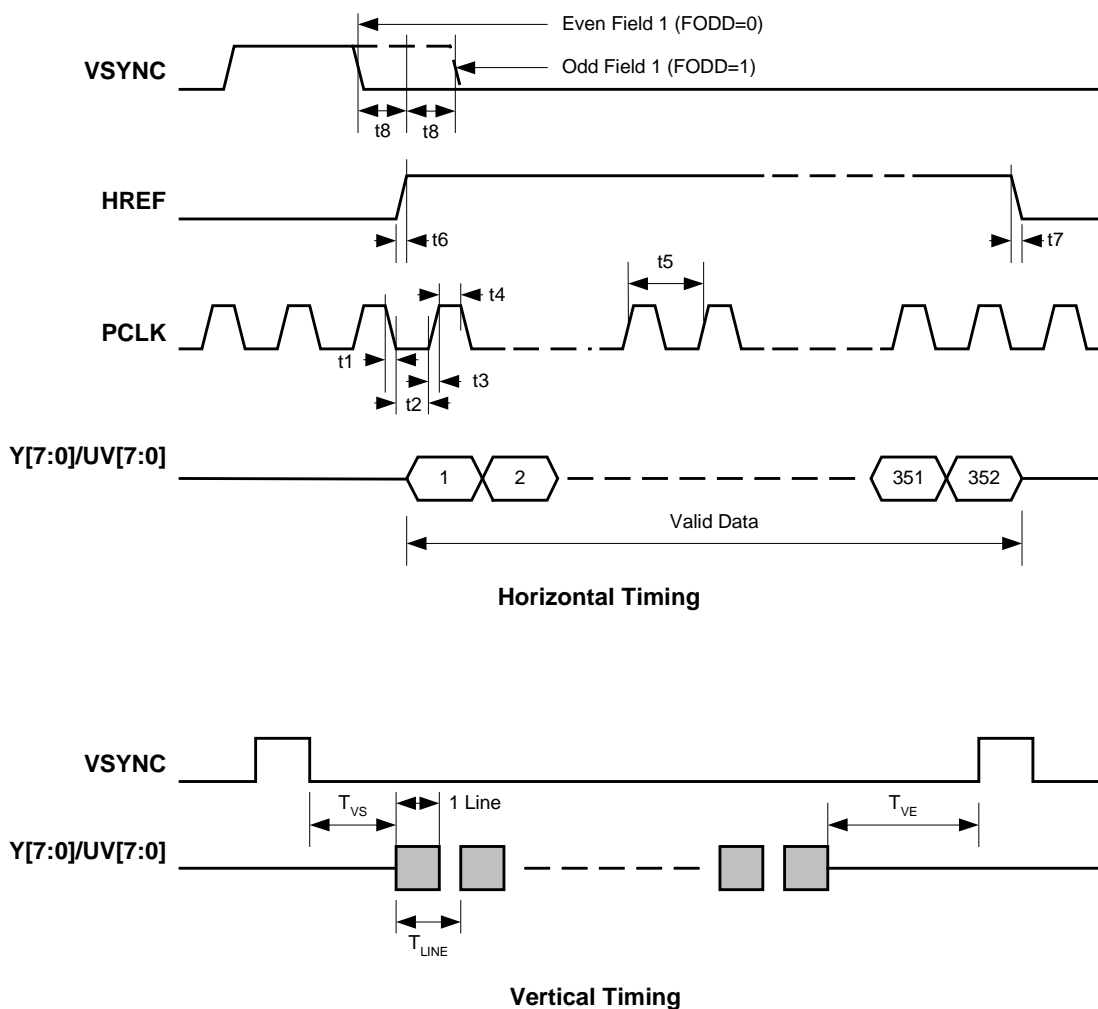


Figure 3. Zoom Video Port Timing

**Notes:**

- Zoom Video Port format output signal includes:  
 VSYNC: Vertical sync pulse.  
 HREF: Horizontal valid data output window.  
 PCLK: Pixel clock used to clock valid data and CHSYNC into Zoom V Port. Default frequency is 8.86MHz when use 17.73MHz as system clock. Rising edge of PCLK is used to clock the 16 Bit data.  
 Y[7:0]: 8 Bit luminance data bus.  
 UV[7:0]: 8 Bit chrominance data bus.
- All timing parameters are provided in Table 13. Zoom Video Port AC Parameters.

**1.2.5 QCIF Format**

A QCIF mode is available for applications where higher resolution image capture is not required. Only half of the pixel rate is required when programmed in this mode. Default resolution is 176 x 144 pixels and can be programmed for other resolutions. Refer to Table 7. QCIF Digital Output Format (YUV beginning of line) and Table 8. QCIF Digital Output Format (RGB raw data beginning of line) for further information.

**1.2.6 Video Output**

The video output port of the OV6630/OV6130 image sensors provides a number of output format/standard options to suit many different application requirements. Table 2. Digital Output Format, below, indicates the output formats available. These formats are user programmable through the I<sup>2</sup>C interface (See I<sup>2</sup>C Bus Protocol Format).

The OV6630/OV6130 imager supports both ITU-601 and ITU-656 output formats in the following configurations (See Table 3. 4:2:2 16-bit Format for further details):

- 16-bit, 4:2:2 format  
*(This mode complies with the 60/50 Hz ITU-601 timing standard. See Table 3. 4:2:2 16-bit Format below)*
- 8-bit data mode  
*(In this mode, video information is output in Cb Y Cr Y order using the Y port only and running at twice the pixel rate during which the UV port is inactive. See Table 4. 4:2:2 8-bit Format below)*
- 4-bit nibble mode  
*(In the nibble mode, video output data appears at bits Y4-Y7. The clock rate for the output runs at twice the normal output speed when in B/W mode, and 4 times the normal output speed in when in color mode.)*
- 704 x 288 format  
*(When programmed in this mode, the pixel clock is doubled and the video output sequence is Y<sub>0</sub>Y<sub>0</sub>Y<sub>1</sub>Y<sub>1</sub> . . . and U<sub>0</sub>U<sub>0</sub>V<sub>0</sub>V<sub>0</sub> . . . . See Figure 4. Pixel Data Bus (YUV Output) below.)*

The OV6630/OV6130 imager provides VSYNC, HREF, PCLK, FODD, and CHSYNC as standard output video timing signals.

The OV6630/OV6130 imager can also be programmed to provide RGB raw data in 16-bit, 8-bit, and 4-bit format. The output sequence is matched to the OV6630 color filter pattern (See Figure 5. Pixel Data Bus (RGB Output) below):

- Y channel output sequence is G R G R

**Table 2. Digital Output Format**

| Resolution             | Pixel Clock          | 352 x 288 | 704 x 288 | 176 x 144 |
|------------------------|----------------------|-----------|-----------|-----------|
| YUV 4:2:2              | 16-bit               | Y         | Y         | Y         |
|                        | 8-bit                | Y         | Y         | Y         |
|                        | ITU-656              | Y         | Y         | Y         |
|                        | Nibble               | Y         | Y         | Y         |
| RGB                    | 16-bit               | Y         | Y         | Y         |
|                        | 8-bit                | Y         | Y         | Y         |
|                        | ITU-656 <sup>1</sup> | Y         | Y         | Y         |
|                        | Nibble               | Y         | Y         | Y         |
| Y/UV swap <sup>2</sup> | 16-bit               |           |           |           |
|                        | 8-bit                | Y         | Y         | Y         |
| U/V swap               | YUV <sup>3</sup>     | Y         | Y         | Y         |
|                        | RGB <sup>4</sup>     | Y         | Y         | Y         |
| YG                     | 16-bit               | Y         | Y         | Y         |
|                        | 8-bit                |           |           |           |
| One Line               | 16-bit               | Y         |           |           |
|                        | 8-bit                |           |           |           |
| MSB/LSB swap           |                      | Y         | Y         | Y         |

**Note:**

(“Y” indicates mode/combination is supported by OV6630/OV6130)

1. Output is 8-bit in RGB ITU-656 format. SAV and EAV are inserted at the beginning and ending of HREF, which synchronize the acquisition of VSYNC and HSYNC. 8-bit data bus configuration (without VSYNC and CHSYNC) can provide timing and data in this format.

- UV channel output sequence is B G B G

The video output appears in Y channel only and the UV channel is disabled in 8-bit RGB raw data. The output sequence is B G R G.

In RGB raw data ITU-656 modes, the OV6630/OV6130 imager asserts SAV (Start of Active Video) and EAV (End of Active Video) to indicate the beginning and the ending of HREF window. As a result, SAV and EAV change with the active pixel window. The 8-bit RGB raw data is also accessible without SAV and EAV information.

The OV6630/OV6130 imager offers flexibility in YUV output format. The device may be programmed as standard YUV 4:2:2. The device may also be configured to “swap” the U V sequence. When swapped, the UV channel output sequence in the 16-bit configuration becomes:

- V U V U . . . .

The 8-bit configuration becomes:

- V Y U Y . . . .

The third format available in the 8-bit configuration is the Y/UV sequence swap:

- Y U Y V . . . .

The single-chip camera can be configured for use as a black and white image device. The vertical resolution is higher than in color mode. Video data output is provided at the Y port and the UV port is tristated. The data (Y/RGB) rate is equivalent to 16-bit in color mode.

The MSB and LSB of Y/UV or RGB output can be reversed. Y7 is MSB and Y0 is LSB in the default setting. Y7 becomes LSB and Y0 becomes MSB in the reserve order configuration. Y2-Y6 are also reversed appropriately.

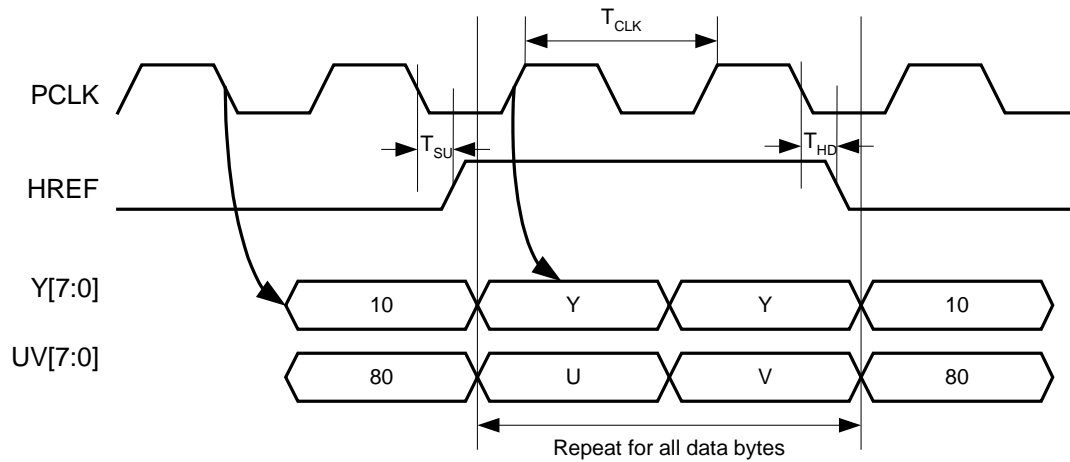
2. Y/UV swap is valid in 8-bit only. Y channel output sequence is Y U Y V . . .
3. U/V swap means UV channel output sequence swap in YUV format, i.e., V U V U . . . for 16 bit and V Y U Y . . . for 8-bit.
4. U/V swap means neighbor row B R output sequence swap in RGB format. Refer to RGB raw data output format for further details.

**Table 3. 4:2:2 16-bit Format**

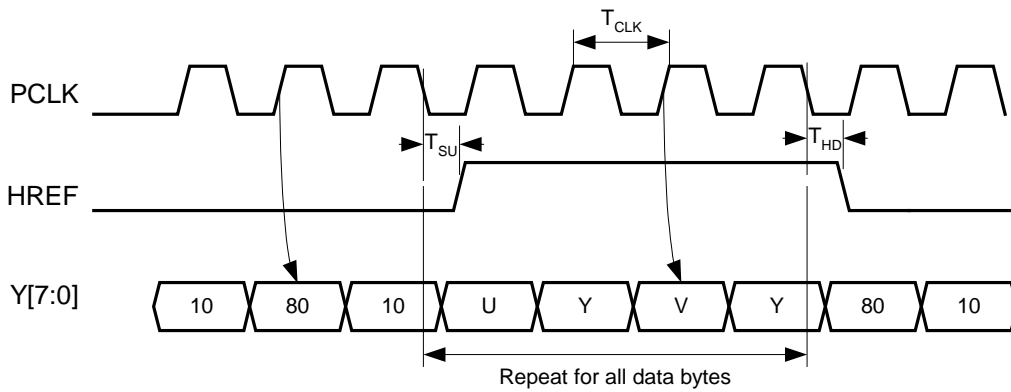
| Data Bus | Pixel Byte Sequence |     |     |     |     |     |
|----------|---------------------|-----|-----|-----|-----|-----|
| Y7       | Y7                  | Y7  | Y7  | Y7  | Y7  | Y7  |
| Y6       | Y6                  | Y6  | Y6  | Y6  | Y6  | Y6  |
| Y5       | Y5                  | Y5  | Y5  | Y5  | Y5  | Y5  |
| Y4       | Y4                  | Y4  | Y4  | Y4  | Y4  | Y4  |
| Y3       | Y3                  | Y3  | Y3  | Y3  | Y3  | Y3  |
| Y2       | Y2                  | Y2  | Y2  | Y2  | Y2  | Y2  |
| Y1       | Y1                  | Y1  | Y1  | Y1  | Y1  | Y1  |
| Y0       | Y0                  | Y0  | Y0  | Y0  | Y0  | Y0  |
| UV7      | UV7                 | UV7 | UV7 | UV7 | UV7 | UV7 |
| UV6      | UV6                 | UV6 | UV6 | UV6 | UV6 | UV6 |
| UV5      | UV5                 | UV5 | UV5 | UV5 | UV5 | UV5 |
| UV4      | UV4                 | UV4 | UV4 | UV4 | UV4 | UV4 |
| UV3      | UV3                 | UV3 | UV3 | UV3 | UV3 | UV3 |
| UV2      | UV2                 | UV2 | UV2 | UV2 | UV2 | UV2 |
| UV1      | UV1                 | UV1 | UV1 | UV1 | UV1 | UV1 |
| UV0      | UV0                 | UV0 | UV0 | UV0 | UV0 | UV0 |
| Y Frame  | 0                   | 1   | 2   | 3   | 4   | 5   |
| UV Frame | 0                   |     | 2   |     | 4   |     |

**Table 4. 4:2:2 8-bit Format**

| Data Bus | Pixel Byte Sequence |    |    |     |    |    |    |
|----------|---------------------|----|----|-----|----|----|----|
| Y7       | U7                  | Y7 | V7 | Y7  | U7 | Y7 | V7 |
| Y6       | U6                  | Y6 | V6 | Y6  | U6 | Y6 | V6 |
| Y5       | U5                  | Y5 | V5 | Y5  | U5 | Y5 | V5 |
| Y4       | U4                  | Y4 | V4 | Y4  | U4 | Y4 | V4 |
| Y3       | U3                  | Y3 | V3 | Y3  | U3 | Y3 | V3 |
| Y2       | U2                  | Y2 | V2 | Y2  | U2 | Y2 | V2 |
| Y1       | U1                  | Y1 | V1 | Y1  | U1 | Y1 | V1 |
| Y0       | U0                  | Y0 | V0 | Y0  | U0 | Y0 | V0 |
| Y Frame  | 0                   |    | 1  |     | 2  |    | 3  |
| UV Frame | 0 1                 |    |    | 2 3 |    |    |    |



**Pixel Data 16-bit Timing**  
(PCLK rising edge latches data bus)

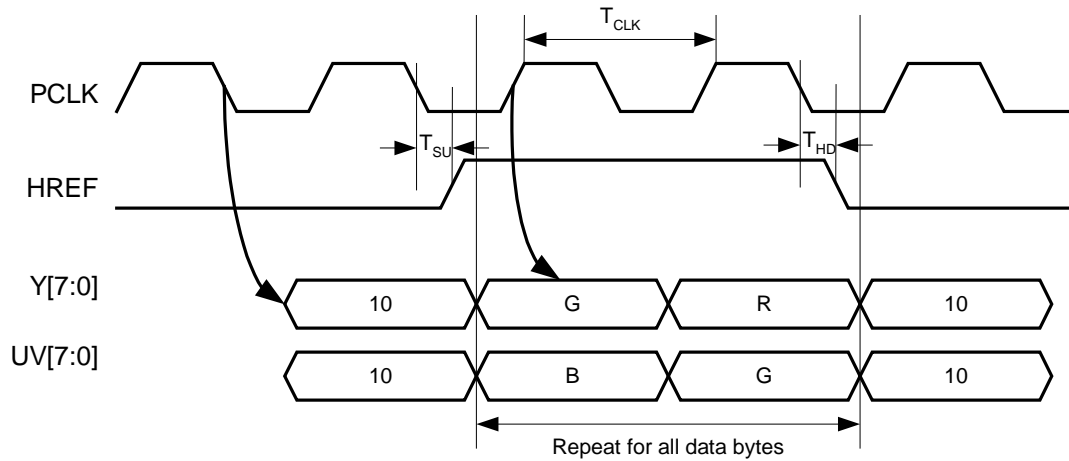


**Pixel Data 8-bit Timing**  
(PCLK rising edge latches data bus)

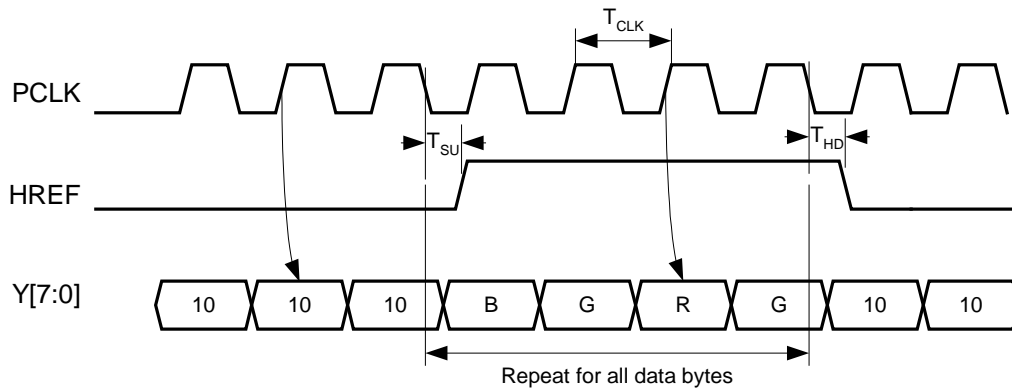
**Note:**  $T_{CLK}$  is pixel clock period..  $T_{CLK}=112ns$  for 16-bit output and  $T_{CLK}=56ns$  for 8-bit output if the system clock is 17.73MHz.  $T_{SU}$  is the setup time of HREF. The maximum is 15ns.  $T_{HD}$  is the hold time of HREF. The maximum is 15ns.

**Figure 4. Pixel Data Bus (YUV Output)**





**Pixel Data 16-bit Timing  
(PCLK rising edge latches data bus)**



**Pixel Data 8-bit Timing  
(PCLK rising edge latches data bus)**

**Note:**  $T_{CLK}$  is pixel clock period..  $T_{CLK}=112ns$  for 16-bit output and  $T_{CLK}=56ns$  for 8-bit output if the system clock is 17.73MHz.  $T_{SU}$  is the setup time of HREF. The maximum is 15ns.  $T_{HD}$  is the hold time of HREF. The maximum is 15ns.

**Figure 5. Pixel Data Bus (RGB Output)**

The default U/UV channel output port relation before MSB/LSB swap

**Table 5. Default Output Sequence**

|                      | MSB |    |    |    |    |    |    | LSB |
|----------------------|-----|----|----|----|----|----|----|-----|
| Output port          | Y7  | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0  |
| Internal output data | Y7  | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0  |

The relation after MSB/LSB swap changes to

**Table 6. Swapped MSB/LSB Output Sequence**

|                      | MSB |    |    |    |    |    |    | LSB |
|----------------------|-----|----|----|----|----|----|----|-----|
| Output port          | Y7  | Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0  |
| Internal output data | Y0  | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7  |

**Table 7. QCIF Digital Output Format (YUV beginning of line)**

| Pixel # | 1      | 2      | 3      | 4      | 5      | 6      | 7      | 8      |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|
| Y       | Y0     | Y1     | Y2     | Y3     | Y4     | Y5     | Y6     | Y7     |
| UV      | U0, V0 | U1, V1 | U2, V2 | U3, V3 | U4, V4 | U5, V5 | U6, V6 | U7, V7 |

- Y channel output Y2 Y3 Y6 Y7 Y10 Y11 . . .
- UV channel output U2 V3 U6 V7 U10 V11 . . .
- Half (176 pixels) data are outputted every line and only half line data (every other line, total 144 lines) in one frame.

**Table 8. QCIF Digital Output Format (RGB raw data beginning of line)**

| Pixel # | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  |
|---------|----|----|----|----|----|----|----|----|
| Line 1  | B0 | G1 | B2 | G3 | B4 | G5 | B6 | G7 |
| Line 2  | G0 | R1 | G2 | R3 | G4 | R5 | G6 | R7 |

1. Default RGB two line output mode:
  - Y channel output G0 R1 G4 R5 G8 R9 . . .
  - UV channel output B0 G1 B4 G5 B8 G9 . . .
  - Every line output half data (176 pixels) and all lines (144 lines) data in one frame will be output.
2. YG two line output mode:
  - Y channel output G0 R1 G4 R5 G8 R9 . . .
  - UV channel output B0 G1 B4 G5 B8 G9 . . .
3. QCIF Resolution Digital Output Format
  - Y channel output Y2 Y3 Y6 Y7 Y10 Y11 . . .
  - UV channel output U2 V3 U6 V7 U10 V11 . . .
  - Every line output data number is half (176 pixels) and only one half line data (every other line, total 144 lines) in one frame will be output.

**Table 9. RGB Raw Data Format**

| R\C | 1                  | 2                  | 3                  | 4                  | ... | 353                  | 354                  | 355                  | 356                  |
|-----|--------------------|--------------------|--------------------|--------------------|-----|----------------------|----------------------|----------------------|----------------------|
| 1   | B <sub>1,1</sub>   | G <sub>1,2</sub>   | B <sub>1,3</sub>   | G <sub>1,4</sub>   |     | B <sub>1,353</sub>   | G <sub>1,354</sub>   | B <sub>1,355</sub>   | G <sub>1,356</sub>   |
| 2   | G <sub>2,1</sub>   | R <sub>2,2</sub>   | G <sub>2,3</sub>   | R <sub>2,4</sub>   |     | G <sub>2,353</sub>   | R <sub>2,354</sub>   | G <sub>2,355</sub>   | R <sub>2,356</sub>   |
| 3   | B <sub>3,1</sub>   | G <sub>3,2</sub>   | B <sub>3,3</sub>   | G <sub>3,4</sub>   |     | B <sub>3,353</sub>   | G <sub>3,354</sub>   | B <sub>3,355</sub>   | G <sub>3,356</sub>   |
| 4   | G <sub>4,1</sub>   | R <sub>4,2</sub>   | G <sub>4,3</sub>   | R <sub>4,4</sub>   |     | G <sub>4,353</sub>   | R <sub>4,354</sub>   | G <sub>4,355</sub>   | R <sub>4,356</sub>   |
| 289 | B <sub>289,1</sub> | G <sub>289,2</sub> | B <sub>289,3</sub> | G <sub>289,4</sub> |     | B <sub>289,353</sub> | G <sub>289,354</sub> | B <sub>289,355</sub> | G <sub>289,356</sub> |
| 290 | G <sub>290,1</sub> | R <sub>290,2</sub> | G <sub>290,3</sub> | R <sub>290,4</sub> |     | G <sub>290,353</sub> | R <sub>290,354</sub> | G <sub>290,355</sub> | R <sub>290,356</sub> |
| 291 | B <sub>291,1</sub> | G <sub>291,2</sub> | B <sub>291,3</sub> | G <sub>291,4</sub> |     | B <sub>291,353</sub> | G <sub>291,354</sub> | B <sub>291,355</sub> | G <sub>291,356</sub> |
| 292 | G <sub>292,1</sub> | R <sub>292,2</sub> | G <sub>292,3</sub> | R <sub>292,4</sub> |     | G <sub>292,353</sub> | R <sub>292,354</sub> | G <sub>292,355</sub> | R <sub>292,356</sub> |

**Notes:**

- A. Y port output data sequence: G R G R G R . . . or G G G G . . .; UV port output data sequence: B G B G B G . . . or B R B R . . .; and the array color filter pattern is Bayer-Pattern.
- B. Output Modes
  1. 16-bit Format (Total 292 HREFs)

- ❖ Default mode:
  - 1st HREF Y channel output unstable data, UV output  $B_{11} G_{12} B_{13} G_{14} \dots$
  - 2nd HREF Y channel output  $G_{21} R_{22} G_{23} R_{24} \dots$ , UV output  $B_{11} G_{12} B_{13} G_{14} \dots$
  - 3rd HREF Y channel output  $G_{21} R_{22} G_{23} R_{24} \dots$ , UV output  $B_{31} G_{23} B_{33} G_{34} \dots$
  - Every line of data is output twice.
- ❖ YG mode:
  - 1st HREF Y and UV output unstable data.
  - 2nd HREF Y channel output  $G_{21} G_{12} G_{23} G_{14} \dots$ , UV output  $B_{11} R_{22} B_{13} R_{24} \dots$
  - 3rd HREF Y is  $G_{21} G_{32} G_{23} G_{34} \dots$ , UV channel is  $B_{31} R_{22} B_{33} R_{24} \dots$
  - Every line data output twice.
- ❖ One line mode:
  - 1st HREF Y channel output  $B_{11} G_{12} B_{13} G_{14} \dots$
  - 2nd HREF Y channel output  $G_{21} R_{22} G_{23} R_{24} \dots$
  - UV channel tri-state.

#### 2. 8-bit Format (Total 292 HREFs)

- 1st HREF Y channel output unstable data.
- 2nd HREF Y channel output  $B_{11} G_{21} R_{22} G_{12} \dots$
- 3rd HREF Y channel output  $B_{31} G_{21} R_{22} G_{32} \dots$
- PCLK timing is doubled and PCLK rising edge latch data bus. UV channel tri-state. Every line data output twice.

#### 3. 4-bit Nibble Mode Output Format

- Uses higher 4 bits of Y port (Y[7:4]) as output port.
- Supports YCrCb/RGB data, ITU-601/ITU-656 timing, Color/B&W.
- Output sequence: High order 4 bits followed by lower order 4 bits  
 $Y_{0H} Y_{0L} Y_{1H} Y_{1L} \dots$   
 $U_{0H} U_{0L} V_{0H} V_{0L} \dots$

For B/W or one-line RGB raw data, the output data clock speed is doubled. For color YUV, output clock is four times that of the 16-bit output data. In color mode, sensor must be set to 8-bit mode, and the nibble timing, clock divided by 2.

Output sequence:  $U_{0H} U_{0L} Y_{0H} Y_{0L} V_{0H} V_{0L} Y_{1H} Y_{1L} \dots$

### 1.2.7 Slave Mode Operation

The OV6630/OV6130 can be programmed to operate in slave mode (COMI[6] = 1, default is master mode). HSYNC and VSYNC output signals are provided.

When used as a slave device, the external master must provide the following clocks to OV6630/OV6130 imager:

1. System clock CLK to XCLK1 pin
2. Horizontal sync, HSYNC, to CHSYNC pin, positive assertion
3. Vertical frame sync, VSYNC, to VSYNC pin, positive assertion

In slave mode, the OV6630/OV6130 tri-states CHSYNC (pin 42) and VSYNC (pin 16) output pins, and used as input pins. To synchronize multiple devices, OV6630/OV6130 uses external system clock, CLK, to synchronize external horizontal sync, HSYNC, which is then used to synchronize external vertical frame sync, VSYNC. See Figure 6. Slave Mode External Sync Timing for timing considerations.

### 1.2.8 Frame Exposure Mode

OV6630/OV6130 supports frame. FREX (pin 4) is asserted by an external master device to set exposure time. The pixel array is quickly pre-charged when FREX is set to "1". OV6630/OV6130 captures the image in the time period when FREX remains high. The video data stream is delivered to output port in a line-by-line manner after FREX switches to "0".

It should be noted that FREX must remain high long enough to ensure the entire image array has been pre-charged.

When data is being output from OV6630/OV6130, care must be taken so as not to expose the image array to light. This may affect the integrity of the image data captured. A mechanical shutter synchronized with the frame exposure rate can be used to minimize this situation. The timing of frame exposure is shown in Figure 7. Frame Exposure Timing below.

### 1.2.9 Reset

OV6630/OV6130 includes a RESET pin (pin 2) that forces a complete hardware reset when it is pulled high (VCC). OV6630/OV6130 clears all registers and resets to their default values when a hardware reset occurs. Reset can also be initiated through the I<sup>2</sup>C interface.

### 1.2.10 Power Down Mode

Two methods are available to place OV6630/OV6130 into power-down mode: hardware power down and I<sup>2</sup>C software power down.

To initiate hardware power down, the PWDN pin (pin 9) must be tied to high (+3.3VDC). When this occurs, OV6630/OV6130 internal device clock is halted and all internal counters are reset. The current draw is less than 10 $\mu$ A in this standby mode.

Executing a software power down through the I<sup>2</sup>C interface suspends internal circuit activity, but does not halt the device clock. The current requirements drop to less than 1mA in this mode.

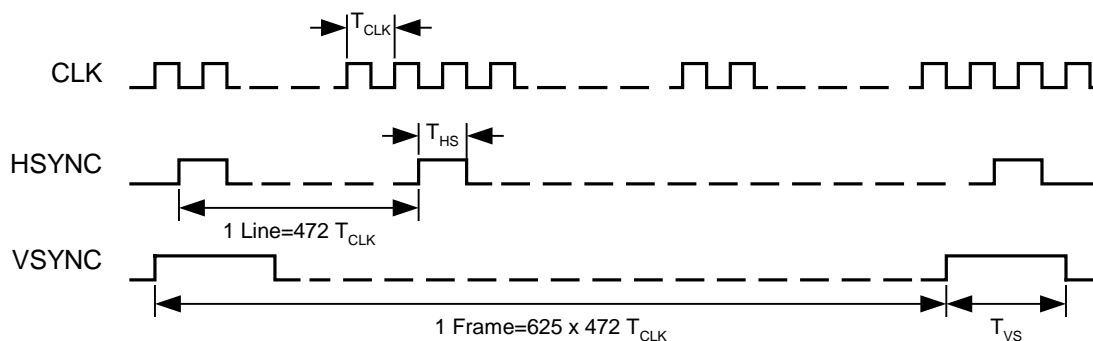
### 1.2.11 Configure OV6630/OV6130

Two methods are provided to configure OV6630/OV6130 for specific application requirements.

At power up, OV6630/OV6130 reads the status of certain pins to determine what, if any, power up pin programming default settings are requested. Once the reading of the external pins status is completed, the device configures its internal registers according to the

specified pins. Not all device functions are available for configuration through external pins. Power up pin programming occurs in 1024 system clock cycles.

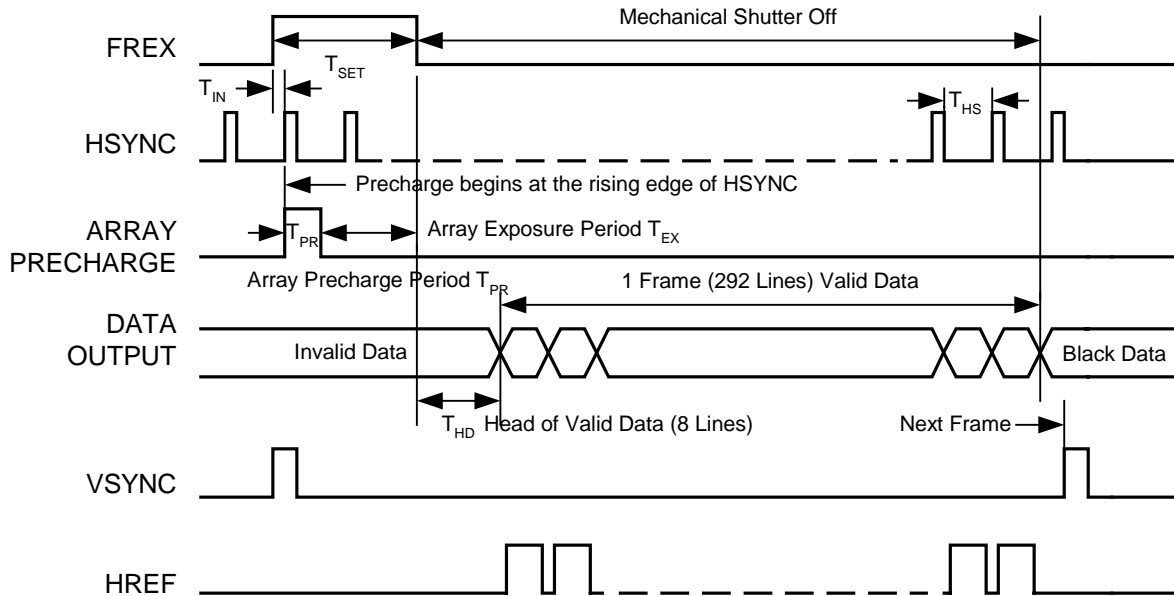
A more flexible and comprehensive method to configure OV6630/OV6130 is to use its on-chip I<sup>2</sup>C register programming capability. The I<sup>2</sup>C interface provides access to all of the device's programmable internal registers. See I2C Bus Protocol Format for further details about using the I<sup>2</sup>C interface on the OV6630/OV6130 camera device.



**Notes:**

- $T_{HS} > 6 T_{CLK} (2), T_{HS} < T_{VS} < 472 T_{CLK}$
- *HSYNC period is  $(472 T_{CLK})$*
- *VSYNC period is  $(625 \times 472 T_{CLK})$*
- *OV6630/OV6130 will be stable after 1 field (2nd VSYNC)*

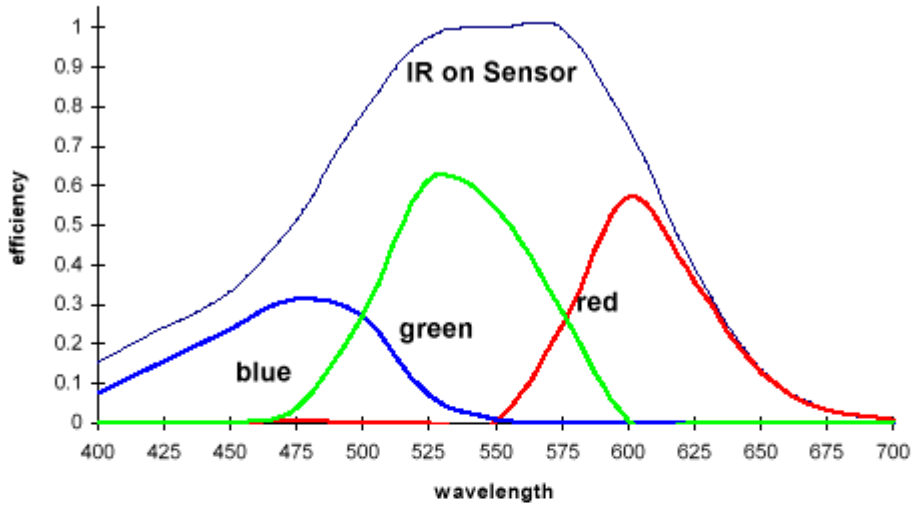
**Figure 6. Slave Mode External Sync Timing**


**Note:**

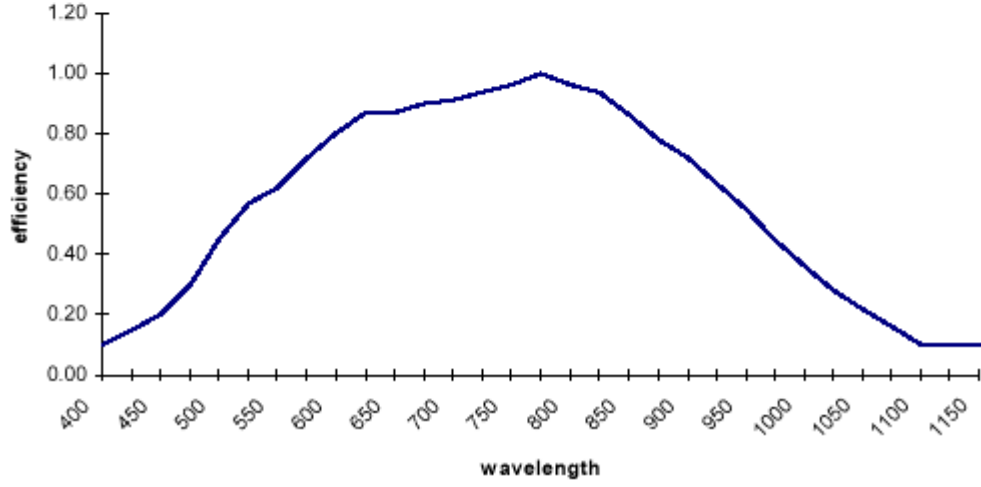
- $T_{PR} = 292 \times 4 \times T_{CLK}$ .  $T_{CLK}$  is internal pixel period.  $T_{CLK} = 112ns$  if the system clock is 17.73MHz.  $T_{CLK}$  will increase with the clock divider CLK[5:0].
- $T_{EX}$  is array exposure time which is decided by external master device.
- $T_{IN}$  is uncertain time due to the using of HSYNC rising edge to synchronize FREX.  $T_{IN} < T_{HS}$ .
- There are 8 lines data output before valid data after FREX=0.  $T_{HD} = 4 T_{HS}$ . Valid data is output when HREF=1.
- $T_{SET} = T_{IN} + T_{PR} + T_{EX}$ .  $T_{SET} > T_{PR} + T_{IN}$ . The exposure time setting resolution is  $T_{HS}$  (one line) due to the uncertainty of  $T_{IN}$ .

**Figure 7. Frame Exposure Timing**

**Normalized Spectrum Response**



**Monochrome Response**



## 2 Electrical Characteristics

**Table 10. DC Characteristics (0°C ≤ TA ≤ 85°C, Voltages referenced to GND)**

| Symbol  | Descriptions   | Max                  | Typ      | Min        | Units |
|---|--|----------------------|----------|------------|-------|
| <b>Supply</b>   |  |                      |          |            |       |
| V <sub>DD1</sub>  | Supply voltage (DEVDD, ADVDD, AVDD, SVDD, DVDD)  | 3.6                  | 3.3      | 2.7        | V     |
| V <sub>DD2</sub>  | Supply voltage (DOVDD)   | 5.5<br>3.6           | 5<br>3.3 | 4.5<br>2.7 | V     |
| I <sub>DD1</sub>  | Supply current (@50Hz frame rate and 3.3V digital I/O with 25pF plus 1TTL loading on 16-bit data bus)                                | 40                   |          |            | mA    |
| I <sub>DD2</sub>  | Supply current (V <sub>DD</sub> =3V, @50Hz frame rate without digital I/O loading, 2 ports output, and without internal charge pump) |                      | 12       |            | mA    |
| I <sub>DD3</sub>  | Standby supply current   | 10                   | 5        |            | μA    |
| <b>Digital Inputs</b>                                       |  |                      |          |            |       |
| V <sub>IL</sub>   | Input voltage LOW  | 0.8                  |          |            | V     |
| V <sub>IH</sub>   | Input voltage HIGH   |                      |          | 2          | V     |
| C <sub>IN</sub>   | Input capacitor  | 10                   |          |            | PF    |
| <b>Digital Outputs</b> (standard loading 25pF, 1.2KΩ to 3V) |  |                      |          |            |       |
| V <sub>OH</sub>   | Output voltage HIGH  |                      |          | 2.4        | V     |
| V <sub>OL</sub>   | Output voltage LOW   | 0.6                  |          |            | V     |
| <b>I<sup>2</sup>C Input</b> (5KΩ pull up + 100pF)           |  |                      |          |            |       |
| V <sub>IL</sub>   | SDA and SCL (V <sub>DD2</sub> =5V)   | 1.5                  |          | -0.5       | V     |
| V <sub>IH</sub>   | SDA and SCL (V <sub>DD2</sub> =5V)   | V <sub>DD</sub> +0.5 | 3.3      | 3.0        | V     |
| V <sub>IL</sub>   | SDA and SCL (V <sub>DD2</sub> =3V)   | 1                    | 0        | -0.5       | V     |
| V <sub>IH</sub>   | SDA and SCL (V <sub>DD2</sub> =3V)   | V <sub>DD</sub> +0.5 | 3        | 2.5        | V     |

**Table 11. AC Characteristics (T<sub>A</sub>=25°C, V<sub>DD</sub>=3V)**

| Symbol                  | Descriptions   | Max | Typ             | Min | Units |
|-------------------------|--|-----|-----------------|-----|-------|
| <b>RGB/YCrCb Output</b> |  |     |                 |     |       |
| I <sub>SO</sub>         | Maximum sourcing current   |     | 15              |     | mA    |
| V <sub>Y</sub>          | DC level at zero signal<br>Y <sub>pp</sub> 100% amplitude (without sync)<br>Sync amplitude |     | 1.2<br>1<br>0.4 |     | V     |
| <b>ADC Parameters</b>   |  |     |                 |     |       |
| B                       | Analog bandwidth   |     |                 |     | MHz   |
| Φ <sub>DIFF</sub>       |  |     |                 |     |       |
| DLE                     | DC differential linearity error  |     | 0.5             |     | LSB   |
| ILE                     | DC integral linearity error  |     | 1               |     | LSB   |

**Table 12. Timing Characteristics**

| Symbol                                   | Descriptions                         | Max | Typ    | Min | Units |
|--|--------------------------------------|-----|--------|-----|-------|
| <b>Oscillator and Clock Input</b>        |                                      |     |        |     |       |
| f <sub>OSC</sub>                         | Frequency (XCLK1, XCLK2)             | 24  | 17.734 | 10  | MHz   |
| t <sub>r</sub> , t <sub>f</sub>          | Clock input rise/fall time           | 5   |        |     | ns    |
|  | Clock input duty cycle               | 55  | 50     | 45  | %     |
| <b>I<sup>2</sup>C Timing</b> (400Kbit/s) |                                      |     |        |     |       |
| t <sub>BUF</sub>                         | Bus free time between STOP and START |     |        | 1.3 | ms    |
| t <sub>HD:SAT</sub>                      | SCL change after START status        |     |        | 0.6 | μs    |
| t <sub>LOW</sub>                         | SCL low period                       |     |        | 1.3 | μs    |
| t <sub>HIGH</sub>                        | SCL high period                      |     |        | 0.6 | μs    |
| t <sub>HD:DAT</sub>                      | Data hold time                       |     |        | 0   | μs    |

|                       |  |    |    |           |         |
|-----------------------|--|----|----|-----------|---------|
| $t_{SU:DAT}$          | Data setup time  |    |    | 0.1       | $\mu s$ |
| $t_{SU:STP}$          | Setup time for STOP status                             |    |    | 0.6       | $\mu s$ |
| <b>Digital Timing</b> |  |    |    |           |         |
| $t_{PCLK}$            | PCLK cycle time<br>16-bit operation<br>8-bit operation |    |    | 112<br>56 | ns      |
| $t_r, t_f$            | PCLK rise/fall time                                    | 15 |    |           | ns      |
| $t_{PDD}$             | PCLK to data valid                                     | 15 |    |           | ns      |
| $t_{PHD}$             | PCLK to HREF delay                                     | 20 | 10 | 5         | ns      |

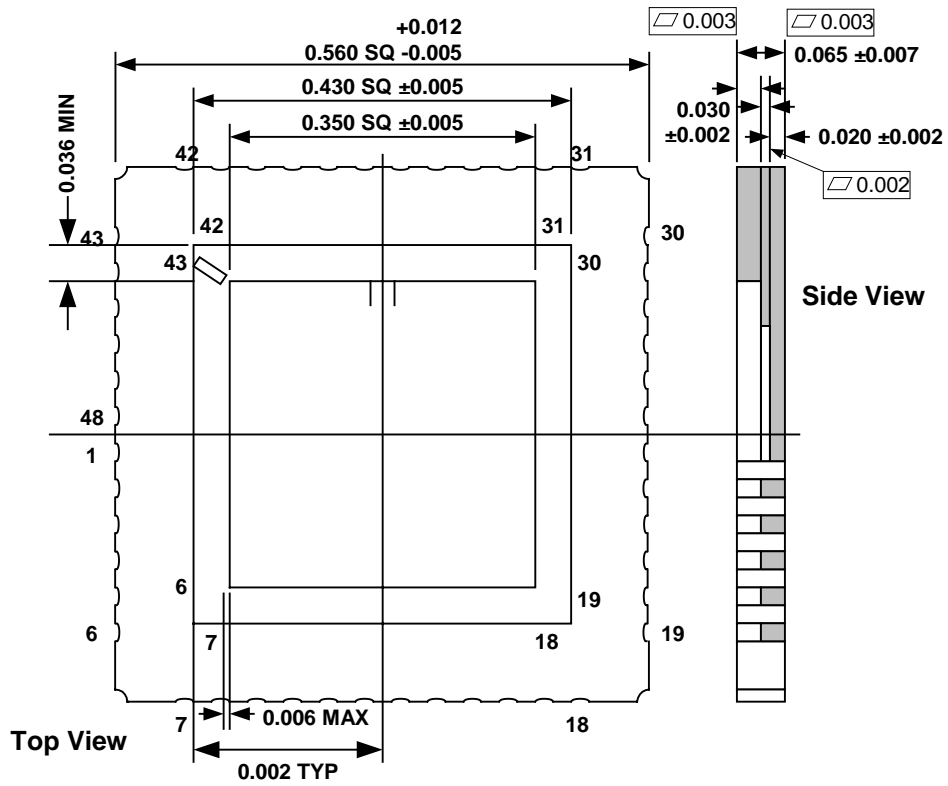
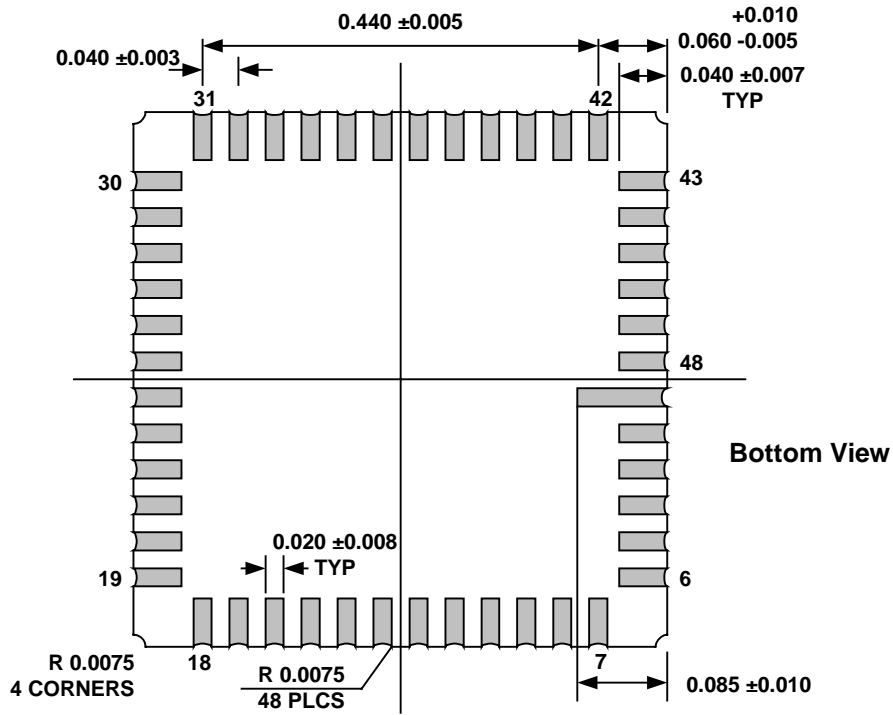
**Table 13. Zoom Video Port AC Parameters**

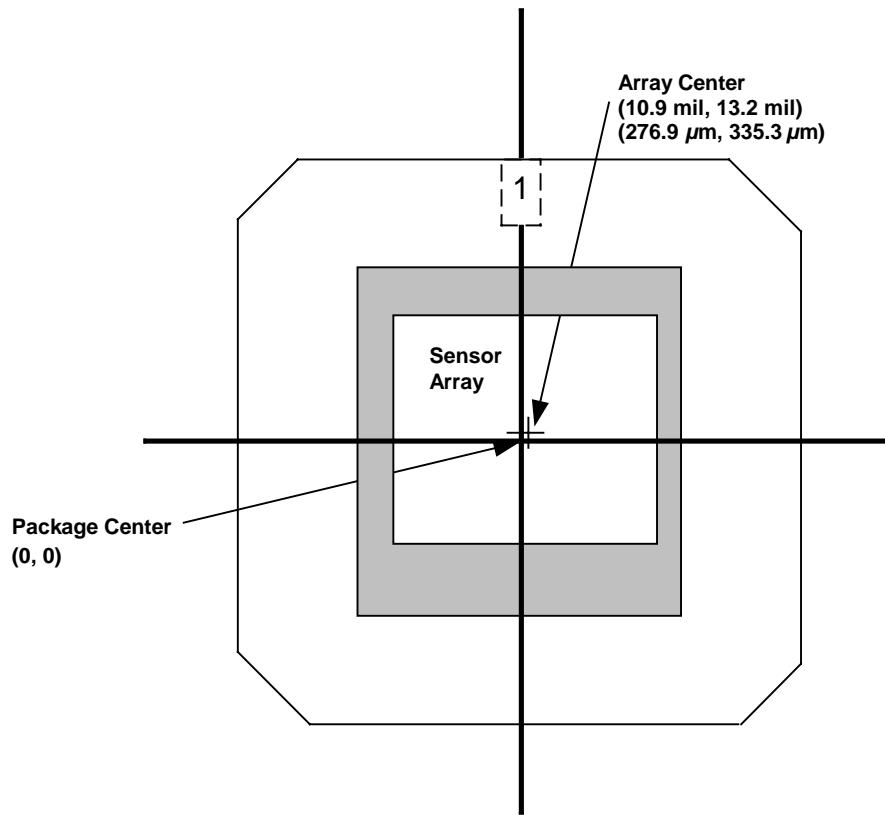
| Symbol | Parameter                     | Min       | Max |
|--------|-------------------------------|-----------|-----|
| t1     | PCLK fall time                | 4ns       | 8ns |
| t2     | PCLK low time                 | 50ns      |     |
| t3     | PCLK rise time                | 4ns       | 8ns |
| t4     | PCLK high time                | 50ns      |     |
| t5     | PCLK period                   | 106ns     |     |
| t6     | Y/UV/HREF setup time          | 10ns      |     |
| t7     | Y/UV/HREF hold time           | 20ns      |     |
| t8     | VSYNC setup/hold time to HREF | 1 $\mu s$ |     |

**Notes:**

1. In Interlaced Mode, there are even/odd field different (t8). When In Progressive Scan Mode, only frame timing same as Even field(t8).
2. After VSYNC falling edge, OV6630 will output black reference level, the line number is  $T_{VS}$ , which is the line number between the 1st HREF rising edge after VSYNC falling edge and 1st valid data CHSYNC rising edge. Then valid data, then black reference, line number is  $T_{VE}$ , which is the line number between last valid data CHSYNC rising edge and 1st CHSYNC rising edge after VSYNC rising edge. The black reference output line number is dependent on vertical window setting.
3. When in default setting,  $T_{VE} = 14 \times T_{LINE}$ , which is changed with register VS[7:0]. VS[7:0] step equal to 1 line.
4. When in default setting,  $T_{VE} = 4 \times T_{LINE}$  for Odd Field,  $T_{VE} = 3 \times T_{LINE}$  for Even Field, which is changed with register VE[7:0]. VE[7:0] step equal to 1 line.







**Table 14. Ordering Information**

| Part Number | Description  | Package    |
|-------------|--|------------|
| OV6630      | COLOR Image Sensor, CIF, Digital, I <sup>2</sup> C Bus Control | 48 pin LCC |
| OV6130      | B/W Image Sensor, CIF, Digital, I <sup>2</sup> C Bus Control   | 48 pin LCC |

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### 3 I<sup>2</sup>C Bus

Many of the functions and configuration registers in the OV6630/OV6130 image sensors are available through the I<sup>2</sup>C interface. The I<sup>2</sup>C port is enabled by asserting the I2CB line (pin 12) through a 10KΩ resistor to V<sub>DD</sub>. When the I<sup>2</sup>C capability is enabled (I2CB = 1), the OV6630/OV6130 imager operates as a slave device

that supports up to 400 Kbps serial transfer rate using a 7-bit address/data transfer protocol.

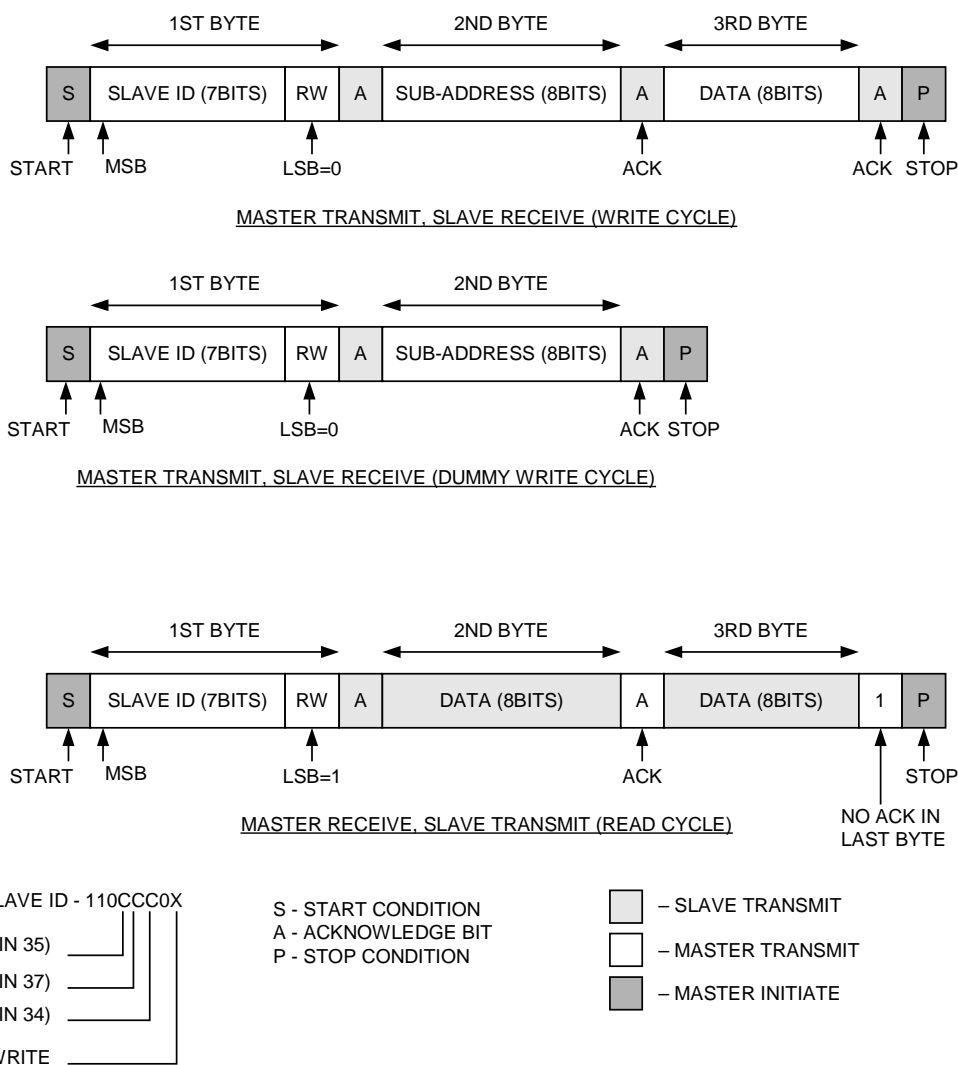


Figure 8. I<sup>2</sup>C Bus Protocol Format

#### 3.1 I<sup>2</sup>C Bus Protocol Format

In I<sup>2</sup>C operation, the master must perform the following operations:

- Generate the start/stop condition
- Provide the serial clock on SCL

- Place the 7-bit slave address, the RW bit, and the 8-bit sub-address on SDA

The receiver must pull down SDA during the acknowledge period. During the write cycle, OV6630/OV6130 returns acknowledge and,

during read cycle, the master returns acknowledge except the read data is the last byte. The master does not perform acknowledge if the read data is the last byte, indicates that the slave can terminate the read cycle. Note that the restart feature is not supported here.

Within each byte, MSB is always transferred first. Read/write control bit is the LSB of the first byte.

Standard I<sup>2</sup>C communications require only two pins: SCL and SDA. SDA is configured as open drain for bi-directional purpose. A HIGH to LOW transition on the SDA while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA while

SCL is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions.

Except for these two special conditions, the protocol that SDA remain stable during the HIGH period of the clock, SCL. Each bit is allowed to change state only when SCL is LOW (See Figure \* and Figure 10 below).

The OV6630/OV6130 I<sup>2</sup>C supports multi-byte write and multi-byte read. The master must supply the sub-address. in the write cycle, but not in the read cycle.

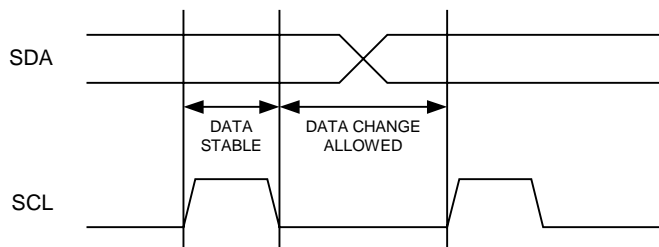


Figure 9. Bit Transfer on the I<sup>2</sup>C Bus

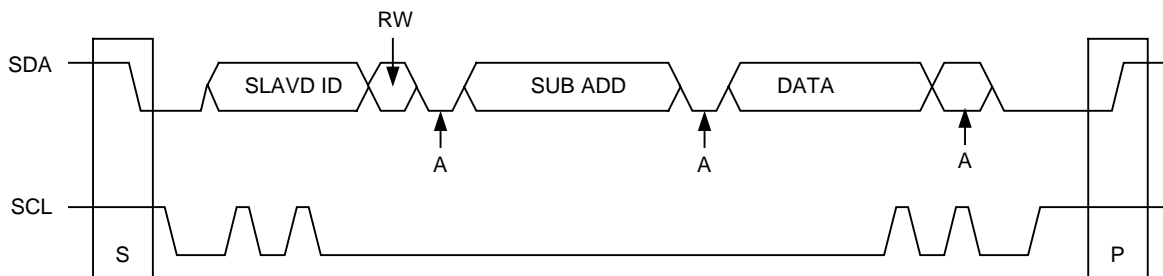


Figure 10. Data Transfer on the I<sup>2</sup>C Bus

Therefore, OV6630/OV6130 takes the read sub-address from the previous write cycle. In multi-byte write or multi-byte read cycles, the sub-address is automatically increment after the first data byte so that continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original sub-address; therefore, if a read cycle

immediately follows a multi-byte cycle, you must insert a single byte write cycle that provides a new sub-address.

OV6630/OV6130 can be power up pin programmed to one-of-eight slave ID addresses through function pins CS[2:0] (pins 35, 37, 34, respectively).

Table 15. Slave ID Addresses

| CS[2:0]        | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|----------------|-----|-----|-----|-----|-----|-----|-----|-----|
| WRITE ID (hex) | C0  | C4  | C8  | CC  | D0  | D4  | D8  | DC  |
| READ ID (hex)  | C1  | C5  | C9  | CD  | D1  | D5  | D9  | DD  |

OV6630/OV6130 supports both single chip and multiple chip configurations. By asserting MULT (pin 47) to high, the sensor can be programmed for up to 8 slave ID addresses. Asserting MULT low

configures OV6630/OV6130 for single ID slave address with address C0 for writes and address C1 for reads. MULT is internally defaulted to a low condition.

In the write cycle, the second byte in I<sup>2</sup>C bus is the sub-address for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to unimplemented sub-address is ignored. In the read cycle, the second byte is the data associated with the previous stored sub-address. Reading of unimplemented sub-address returns unknown.

### **3.2 Register Set**

The table below provides a list and description of available I<sup>2</sup>C registers contained in the OV6630/OV6130 image sensor.

Table 16 I<sup>2</sup>C Registers

| Sub-address (hex) | Register   | Default (hex) | Read/Write | Descriptions  |
|-------------------|------------|---------------|------------|---|
| 00                | GAIN       | 00            | RW         | AGC gain control<br>GC[7:6] – Unimplemented.<br>GC[5:0] – The current gain setting.<br><br><i>This register is updated automatically if AGC is enabled. The internal controller stores the optimal gain value in this register. The current value is stored in this register if AGC is not enabled.</i> |
| 01                | BLUE       | 80            | RW         | Blue gain control<br>BLU[7] – “0” decrease gain, “1” increase gain.<br>BLU[6:0] – blue channel gain balance value.<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>   |
| 02                | RED        | 80            | RW         | Red gain control<br>RED[7] – “0” decrease gain, “1” increase gain.<br>RED[6:0] – red channel balance value.<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>  |
| 03                | SAT        | 80            | RW         | Color saturation control<br>SAT[7:3] – Saturation adjustment. “F8h” is highest and “00h” is lowest.<br>SAT[2:0] – Unimplemented.<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>   |
| 04                | Rsvd 04    | xx            | –          | Reserved  |
| 05                | CTR        | 48            | RW         | Contrast control<br>CTR[7] – selects gain at the dark area. “0” – gain=0.5 and “1” – gain=1.<br>CTR[6:4] – reserved.<br>CTR[3:0] – Contrast adjustment. “FFh” is highest and “00h” is lowest.   |
| 06                | BRT        | 80            | RW         | Brightness control<br>BRT[7:0] – Brightness adjustment. “FFh” is highest and “00h” is lowest.   |
| 07                | SHP        | C6            | RW         | Sharpness control<br>SHP[7:4] – Coring adjustment. Range: 0~80mV with step 5mV.<br>SHP[3:0] – Strength adjustment. Range: 0~8x with step 0.5x.  |
| 08-0B             | Rsvd 08-0B | xx            | –          | Reserved  |
| 0C                | ABLU       | 20            | RW         | White balance background: Blue channel<br>ABLU[7:6] – rsvd<br>ABLU[5] – “0” decrease background blue component, “1” increase background blue component<br>ABLU[4:0] - White balance blue ratio adjustment<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>                |
| 0D                | ARED       | 20            | RW         | White balance background: Red channel<br>ARED[7:6] – rsvd<br>ARED[5] – “0” decrease background red component, “1” increase background red component<br>ARED[4:0] - White balance red ratio adjustment<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>                    |
| 0E                | COMR       | 0D            | RW         | Common control R<br>COMR[7] – Analog signal 2x gain control bit. “1” - Additional 2x gain, “0” - normal.<br>COMR[6:0] – Reserved.   |
| 0F                | COMS       | 05            | RW         | Common control S<br>COMS[7:6] – Reserved<br>COMS[5:4] – select the lowest signal used in automatic black level expanding (or automatic brightness). “00” – lowest, “11” – highest and image is brighter.<br>COMS[3:2] – select highest luminance level to be available in AWB control. “00” –           |

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|    |       |    |    | lowest, "11" – highest.<br>COMS[1:0] – select lowest luminance level to be available in AWB control. "00" – lowest, "11" – highest.  |
| 10 | AEC   | 9A | RW | Automatic exposure control<br>AEC[7:0] - Set exposure time<br>$T_{EX} = 2 \times T_{LINE} \times AEC[7:0]$   |
| 11 | CLKRC | 00 | RW | Clock rate control<br>CLKRC[7:6] – Sync output polarity selection<br>"00" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Pos<br>"01" – HSYNC=Neg, CHSYNC=Neg, VSYNC=Neg<br>"10" – HSYNC=Pos, CHSYNC=Neg, VSYNC=Pos<br>"11" – HSYNC=Pos, CHSYNC=Pos, VSYNC=Pos<br>CLKRC[5:0] – Clock pre-scaler<br>$CLK = (MAIN\_CLOCK / ((CLKRC[5:0] + 1) \times 2)) / n$<br><br>Where n=1 if register [3E], COMO<7> is set to "1" and n=2 otherwise.  |
| 12 | COMA  | 24 | RW | Common control A<br>COMA[7] – SRST, "1" initiates soft reset. All registers are set to default values and chip is reset to known state and resumes normal operation. This bit is automatically cleared after reset.<br>COMA[6] – MIRR, "1" selects mirror image<br>COMA[5] – AGCEN, "1" enables AGC,<br>COMA[4] – Digital output format, "1" selects 8-bit: Y U Y V Y U Y V<br>COMA[3] – Select video data output: "1" - select RGB, "0" - select YCrCb<br>COMA[2] – Auto white balance "1" - Enable AWB, "0" - Disable AWB<br>COMA[1] – Color bar test pattern: "1" - Enable color bar test pattern<br>COMA[0] – reserved<br><br><i>Note: COMA[3] is not programmable on the OV6130 image sensor.</i> |
| 13 | COMB  | 01 | RW | Common control B<br>COMB[7:6] – reserved<br>COMB[5] - Select data format. "1" - select 8-bit format, Y/CrCb and RGB is multiplexed to 8-bit Y bus, UV bus is tri-stated, "0" - select 16-bit format<br>COMB[4] – "1" - enable digital output in ITU-656 format<br>COMB[3] – CHSYNC output. "1" - horizontal sync, "0" - composite sync<br>COMB[2] – "1" – Tri-state Y and UV busses. "0" - enable both busses<br>COMB[1] – "1" - Initiate single frame transfer.<br>COMB[0] – "1" - Enable auto adjust mode.<br><br><i>Note: COMB[5] is not programmable on the OV6130 image sensor.</i>   |
| 14 | COMC  | 00 | RW | Common control C<br>COMC[7:6] – reserved<br>COMC[5] – QCIF digital output format selection. 1 - 176x144; 0 - 352x288.<br>COMC[4] – Field/Frame vertical sync output in VSYNC port selection: 1 - frame sync, only ODD field vertical sync; 0 - field vertical sync, effect in Interlaced mode<br>COMC[3] – HREF polarity selection: 0 - HREF positive effective, 1 - HREF negative.<br>COMC[2] – gamma selection: 1 - RGB Gamma on ; 0 - RGB gamma is 1.<br>COMC[1:0] – reserved   |
| 15 | COMD  | 01 | RW | Common Control D<br>COMD[7:2] – reserved bit.<br>COMD[1] – PCLK polarity selection. "0" - OV6630/OV6130 output data at PCLK falling edge and data bus will be stable at PCLK rising edge; "1" - rising edge output data and stable at PCLK falling edge. This bit is disable and should use PCLK rising edge latch data bus in ITU-656 format (COMB[4]=1).<br>COMD[0] – U V digital output sequence exchange control. 1 - UV UV . . . for 16-bit, U Y V Y . . . for 8-bit; 0 - V U V U . . . for 16-bit and V Y U Y . . . for 8-bit.<br><br><i>Note: COMD[0] is not programmable on the OV6130 image sensor.</i>   |
| 16 | FSD   | 03 | RW | Field slot division<br>FSD[7:2] – Field interval selection. It has functional in EVEN and ODD mode defined   |

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|       |            |    |    | <p>by FSD[1:0]. It is disabled in OFF and FRAME mode. The purpose of FSD[7:2] is to divide the video signal into programmed number of time slots, and allows HREF to be active only one field in every FSD[7:2] fields. It does not affect the video data or pixel rate. FSD[7:2] disables digital data output, there is only black reference level at the output. FSD[7:2]=1 outputs every field. FSD[7:2]=2 outputs one field and disables one field, etc.</p> <p>FSD[1:0] – field mode selection. Each frame consists of two fields: Odd and Even, FSD[1:0] define the assertion of HREF in relation to the two fields.</p> <p>“00” – OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register 13)</p> <p>“01” – ODD mode; HREF is asserted in odd field only.</p> <p>“10” – EVEN mode; HREF is asserted in even field only.</p> <p>“11” – FRAME mode; HREF is asserted in both odd field and even field. FSD[7:2] disabled.</p> |
| 17    | HREFST     | 38 | RW | <p>Horizontal HREF start</p> <p>HS[7:0] – selects the starting point of HREF window, each LSB represents two pixels for CIF resolution mode, one pixels for QCIF resolution mode, this value is set based on an internal column counter, the default value corresponds to 352 horizontal window. Maximum window size is 356. See window description below. HS[7:0] programmable range is [38] - [EB], and should less than HE[7:0]. HS[7:0] should be programmable to value larger than or equal to [38]. Value larger than [EC] is invalid. See window description below.</p>   |
| 18    | HREFEND    | EA | RW | <p>Horizontal HREF end</p> <p>HE[7:0] – selects the ending point of HREF window, each LSB represents two pixels for full resolution and one pixels for QCIF resolution, this value is set based on an internal column counter, the default value corresponds to the last available pixel. The HE[7:0] programmable range is [39] - [EC]. HE[7:0] should be larger than HS[7:0] and less than or equal to [EC]. Value larger than [EC] is invalid. See window description below.</p>  |
| 19    | VSTRT      | 03 | RW | <p>Vertical line start</p> <p>VS[7:0] – selects the starting row of vertical window, in full resolution mode, each LSB represents 1 scan line in one frame. See window description below. Min. is [03], max. is [93] and should less than VE[7:0].</p>   |
| 1A    | VEND       | 92 | RW | <p>Vertical line end</p> <p>VE[7:0] – selects the ending row of vertical window, in full resolution mode, each LSB represents 1 scan line in one frame, see window description below. Min. is [04], max. is [94] and should larger than VS[7:0].</p>   |
| 1B    | PSHFT      | 00 | RW | <p>Pixel shift</p> <p>PS[7:0] – to provide a way to fine tune the output timing of the pixel data relative to that of HREF, it physically shifts the video data output time late in unit of pixel clock as shown in the figure below. This function is different from changing the size of the window as defined by HS[7:0] and HE[7:0] in registers 17 and 18. Higher than default number delay the pixel output relative to HREF. The highest number is “FF” and the maximum shift number is delay 256 pixels.</p>   |
| 1C    | MIDH       | 7F | R  | <p>Manufacture ID byte: High</p> <p>MIDH[7:0] – read only, always returns “7F” as manufacturer’s ID no.</p>  |
| 1D    | MIDL       | A2 | R  | <p>Manufacture ID byte: Low</p> <p>MIDL[7:0] – read only, always returns “A2” as manufacturer’s ID no.</p>   |
| 1E-1F | Rsvd 1E-1F | xx | RW | Reserved   |
| 20    | COME       | 00 | RW | <p>Common control E</p> <p>COME[7] – HREF pixel number selection. “1” - HREF include 704 PCLK, every data output twice.</p> <p>COME[6] – reserved.</p> <p>COME[5] – “1” First stage aperture correction enable. Correction strength will be decided by register [07]. “0” disable first stage aperture correction.</p> <p>COME[4] – “1” Second stage aperture correction enable. Correction strength and threshold value will be decided by COMF[7] ~ COMF[4].</p> <p>COME[3] – AWB smart mode enable. 1 – do not count pixels that their luminance level are not in the range defined in register [0F]. 0 - count all pixels to get AWB result. Valid only when COMB[0]=1 and COMA[2]=1</p>   |



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|    |      |    |    | <p>COME[2] – reserved.<br/>                 COME[1] – AWB fast/slow mode selection. “1” - AWB is always fast mode, that is register [01] and [02] is changed every field. “0” AWB is slow mode, [01] and [02] change every 16/ 64 field decided by COMK[1]. When AWB enable, COMA[2]=1, AWB is working as fast mode until it reaches stable, than as slow mode.<br/>                 COME[0] – Digital output driver capability increase selection: “1” Double digital output driver current; “0” low output driver current status.</p> <p><i>Note: COME[3] (AWB smart mode), COME[2] (AWB stop), and COME[1] (AWB fast/slow) are not programmable on the OV6130 image sensor.</i></p>  |
| 21 | YOFF | 80 | RW | <p>Y channel offset adjustment<br/>                 YOFF[7] – Offset adjustment direction 0 - Add Y[6:0]; 1 -Subtract Y[6:0].<br/>                 YOFF[6:0] –Y channel digital output offset adjustment. Range: +127 ~ -127. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through I<sup>2</sup>C has no effect. COMG[2]=1, Y channel offset adjustment will use the stored value which can be changed through I<sup>2</sup>C. This register has no effect to A/D output data if COMF[1]=0. If output RGB raw data, this register will adjust R/G/B data.</p>  |
| 22 | UOFF | 80 | RW | <p>U Channel offset adjustment<br/>                 UOFF[7] – Offset adjustment direction: 0 - Add U[6:0]; 1 - Subtract U[6:0].<br/>                 UOFF[6:0] – U channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write a value to this register through I<sup>2</sup>C has no effect. COMG[2]=1, U channel offset adjustment will use the stored value which can be changed through I<sup>2</sup>C. This register has no effect to A/D output data if COMF[1]=1. If output RGB raw data, this register will adjust R/G/B data.</p> <p><i>Note: This function is not available on the OV6130 image sensor.</i></p>  |
| 23 | CLKC | 04 | RW | <p>Oscillator circuit control<br/>                 CLKC[7:6] – Select different crystal circuit power level (“11” = minimum).<br/>                 CLKC[5:0] – reserved</p>   |
| 24 | AEW  | 33 | RW | <p>Automatic exposure control: Bright pixel ratio adjustment<br/>                 AEW[7:0] – Used as calculate bright pixel ratio. OV6630/OV6130 AEC algorithm is count whole field bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is same as the ratio defined by register [25] and [26], image stable. This register is used to define bright pixel ratio, default is 25%, each LSB represent step: 0.5% Change range is: [01] ~ [CA]; Increase AEW[7:0] will increase bright pixel ratio. For same light condition, the image brightness will increase if AEW[7:0] increase.</p> <p><i>Note: AEW[7:0] must combine with register [26] AEB[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] &gt; [CA].</i></p> |
| 25 | AEB  | 97 | RW | <p>Automatic Exposure Control: Black pixel ratio adjustment<br/>                 AEB[7:0] – used as calculate black pixel ratio. OV6630 AEC algorithm is count whole field/ frame bright pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When bright/black pixel ratio is same as the ratio defined by register [25] and [26], image stable. This register is used to define black pixel ratio, default is 80%, each LSB represent step: 0.5%; Change range is: [01] ~ [CA]; Increase AEB[7:0] will increase black pixel ratio. For same light condition, the image brightness will decrease if AEB[7:0] increase.</p> <p><i>Note: AEB[7:0] must e combined with register [25] AEW[7:0]. The relation must be as follows: AEW[7:0] + AEB[7:0] &gt; [CA].</i></p> |
| 26 | COMF | B0 | RW | <p>Common control F<br/>                 COMF[7:4] – reserved.<br/>                 COMF[3] – UV offset difference. “1” use separate offsets for U and V; “0” use one offset for both U and V.<br/>                 COMF[2] – Digital data MSB/LSB swap. “1” LSB→bit7, MSB→bit0; “0” normal.</p>  |

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|    |       |    |    | COMF[1] – “1” digital offset adjustment enable. “0” disable.<br>COMF[0] – “1” Output first 4 line black level before valid data output. HREF number will increase 4 relatively. “0” no black level output.   |
| 27 | COMG  | A0 | RW | Common control G<br>COMG[7:6] – reserved<br>COMG[5] - Select CKOUT pin output V flag. “1” - CKOUT output V flag signal. CKOUT=1 if UV channel output V or Red. CKOUT=0 if UV channel output U or BLUE. “0” - CKOUT output buffered XCLK2<br>COMG[4:3] – reserved.<br>COMG[2] – “1” digital offset adjustment manually mode enable. Digital data will be add/subtract a value defined by register [21] and [22], the contents are programmed through I <sup>2</sup> C. “0” - digital data will be added/subtract a value defined by register [21] and [22], which are updated by internal circuit.<br>COMG[1] – Digital output full range selection. OV6630/OV6130 default output data range is [10] - [F0]. The output range changes to [01] - [FE] with signal overshoot and undershoot level if COMG[1]=1.<br>COMG[0] – reserved.  |
| 28 | COMH  | 01 | RW | Common control H<br>COMH[7] – “1” selects one-line RGB raw data output format, “0” selects normal two-line RGB raw data output.<br>COMH[6] – “1” enable black/white mode. The vertical resolution will be higher than color mode when the imager works as BW mode. OV6630/OV6130 can’t work at 8-bit output in this mode. OV6630/OV6130 outputs data from Y port. UV port will be tri-state. COMB[5] and COMB[4] will be set to “0”. “0” normal color mode.<br>COMH[5] – reserved.<br>COMH[4] – Freeze AEC/AGC value, effective only at COMB[0]=1. “1” - register [00] and [10] will not be updated and hold latest value. “0” - AEC/AGC normal working status.<br>COMH[3] – AGC disable. “1” - when COMB[0]=1 and COMA[5]=1, internal circuit will not update register [00], register [00] will kept latest updated value before COMH[3]=1. “0” - when COMB0=1 and COMA[5]=1, register [00] will be updated by internal algorithm.<br>COMH[2] – RGB raw data output YG format: “1” - Y channel G, UV channel B R; “0” - Y channel: G R G R . . . , UV channel B G B G . . .<br>COMH[1] – Gain control bit. “1” channel gain increases 6dB. “0” no change to the channel gain.<br>COMH[0] – reserved.<br><br><i>Note: COMH[2] (RGB Raw Data) is not programmable on the OV6130 image sensor.</i> |
| 29 | COMI  | 00 | RW | Common control I<br>COMI[7] – AEC disable. “1” If COMB[0]=1, AEC stop and register [10] value will be held at last AEC value and not be updated by internal circuit. “0” - if COMB[0]=1, register [10] value will be updated by internal circuit<br>COMI[6] – Slave mode selection. “1” slave mode, use external SYNC and VSYNC; “0” master mode.<br>COMI[5:4] – reserved<br>COMI[3] – Central 1/4 image area rather whole image used to calculate AEC/AGC. “0” use whole image area to calculate AEC/AGC.<br>COMI[2] – reserved<br>COMI[1:0] – Version flag. For version A, value is [00], these two bits are read only.  |
| 2A | FRARH | 84 | RW | Frame rate adjust high<br>FRARH[7] – Frame Rate adjustment enable bit. “1” Enable.<br>FRARH[6] – reserved<br>FRARH[5] – Highest 1bit of frame rate adjust control byte. See explanation below.<br>FRARH[4] – reserved<br>FRARH[3] – Y channel brightness adjustment enable. When COMF[2]=1 active.<br>FRARH[2] – reserved<br>FRARH[1] – “1” When in Frame exposure mode, only One frame data output.<br>FRARH[0] – reserved  |
| 2B | FRARL | 5E | RW | Frame rate adjust low<br>FRARL[7:0] – Lowest 8 bit of frame rate adjust control byte. Frame rate adjustment  |

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|         |            |    |    | resolution is 0.21%. Control byte is 10 bit. Every LSB equal decrease frame rate 0.21%. Range is 0.21% - 109%. IF frame rate adjustment enable, COME[7] must set to "0".   |
| 2C      | Rsvd 2C    | 88 | RW | Reserved   |
| 2D      | COMJ       | 03 | RW | Common control J<br>COMJ[7:5] – reserved<br>COMJ[4] – Enable auto black expanding mode.<br>COMJ[3] – "1" update white balance update only if AGC/AEC is stable. "0" update white balance independent with AEC/AGC.<br>COMJ[2] – Band filter enable. After adjust frame rate to match indoor light frequency, this bit enable a different exposure algorithm to cut light band induced by fluorescent light.<br>COMJ[1] – reserved<br>COMJ[0] –U and V offset separate mode. "1" U and V use separate offsets. "0" U and V use same offset defined by register [2E].  |
| 2E      | VCOFF      | 80 | RW | V channel offset adjustment<br>VCOFF[7] – Offset adjustment direction: "0" = Add V[6:0]; "1" = Subtract V[6:0].<br>VCOFF[6:0] – V channel digital output offset adjustment. Range: +128 ~ -128. If COMG[2]=0, this register will be updated by internal circuit. Write to this register through I <sup>2</sup> C has no effect. If COMG[2]=1, V channel offset adjustment will use the stored value which can be changed through I <sup>2</sup> C. If COMF[1]=1, this register has no effect to digital output data. If output RGB raw data, this register will adjust R/G/B data.<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>  |
| 2F – 32 | Rsvd 2F–32 | xx | –  | Reserved   |
| 33      | CPP        | 00 | RW | Color processing parameter control<br>CPP[7:6] – reserved<br>CPP[5] – Luminance gamma on/off. "1" - luminance gamma on; "0" - luminance gamma is 1.<br>CPP[4:0] – reserved   |
| 34      | BIAS       | A2 | RW | Bias adjustment<br>BIAS[7:6] – A/D reference level adjustment. "00" - 110% internal full signal range; "01" - 120%, "10" - 130%, "11" - 140%.<br>BIAS[5:0] – reserved  |
| 35-37   | Rsvd 35-37 | 80 | RW | Reserved   |
| 38      | COMK       | 81 | RW | Common control K<br>COMK[7] – HREF edge latched by PCLK falling edge. "0" HREF edge is 10 ns after PCLK rising edge.<br>COMK[6] – Output port drive current additional 2x control bit.<br>COMK[5] – reserved.<br>COMK[4] – ZV port Vertical timing selection. "1" VSYNC output ZV port vertical sync signal. "0" = normal TV vertical sync signal.<br>COMK[3] – Quick stable mode when camera mode change. After relative control bit set, the first VS will be the stable image with suitable AEC/AWB setting. "0" - slow mode, after mode change need more field/frame to get stable AEC/AWB setting image.<br>COMK[2] – reserved<br>COMK[1] – AWB stable time selection when in slow mode. "1" - 4 times less time needed to get stable AWB setting when in slow AWB mode.<br>COMK[0] – reserved.<br><br><i>Note: COMK[1] (AWB stable Time) is not programmable on the OV6130 image sensor.</i> |
| 39      | COML       | 00 | RW | Common control L<br>COML[7] – reserved<br>COML[6] – PCLK output timing selection. "1" - PCLK valid only when HREF is high; "0" - PCLK is free running.<br>COML[5] – reserved.<br>COML[4] – "1" select CHSYNC output from HREF port. "0" normal<br>COML[3] – "1" select HREF output from CHSYNC port. "0" normal  |

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|       |            |    |    | COML[2] – Tristate all control signal output (FODD, CHSYNC, HREF, PCLK)<br>COML[1] – Highest 1 bit of horizontal sync starting position, combined with register [3A]<br>COML[0] – Highest 1 bit of horizontal sync ending position, combined with register [3B]  |
| 3A    | HSST       | 0F | RW | Horizontal sync start position<br>HSST[7:0] – lower 8 bit of horizontal sync starting position, combined with register bit of COML[1], total 9 bit control. range: [00] -- [FF]. HSEND[8:0] must be less than HSST[8:0]  |
| 3B    | HSEND      | 3C | RW | Horizontal sync end position<br>HEND[7:0] – lower 8 bit of horizontal sync ending position, combined with register bit of COML[0], total 9 bit control. range: [00] - [FF]. HSEND[8:0] must be larger than HSST[8:0]   |
| 3C    | COMM       | 21 | RW | Common control M<br>COMM[7:5] – reserved.<br>COMM[4] – AEC/AGC change mode selection<br>COMM[3] – AEC/AGC change mode selection<br>COMM[2] – AEC/AGC change fastest mode<br>COMM[1] – AEC/AGC change fast mode<br>COMM[0] – AEC/AGC change slowest mode  |
| 3D    | COMN       | 08 | RW | Common Control N<br>COMN[7] – Enable one frame drop when AEC change to keep data valid when Banding filter mode enable.<br>COMN[6:4] – reserved<br>COMN[3] – Enable 50 Hz PAL video timing, VTO analog signal can be displayed on TV<br>COMN[2] – reserved<br>COMN[1] – Tri-state Y and UV digital video ports in power down mode.<br>COMN[0] – reserved |
| 3E    | COMO       | 80 | RW | Common control O<br>COMO[7] – Input main clock divided by 2 or 4 selection. “1” -- 2; “0” -- 4<br>COMO[6:5] – reserved<br>COMO[4] – Select 4-bit nibble mode output<br>COMO[3] – reserved<br>COMO[2] – Enable Minimum exposure time is 4 line. Default is 1 line<br>COMO[1:0] – reserved   |
| 3F    | COMP       | 02 | RW | Common control P<br>COMP[7] – reserved<br>COMP[6] – Output main clock output from FODD port<br>COMP[5] – reserved<br>COMP[4] – Soft chip power down enable, can be waked up by disable this bit<br>COMP[3:2] – reserved<br>COMP[1] – ITU-656 output control<br>COMP[0] – Reset internal timing circuit without reset AEC/AGC/AWB value                   |
| 40-4C | Rsvd 40-4C | xx | –  | Reserved   |
| 4D    | YMXA       | 02 | RW | YUV matrix control (Main)<br>YMXA[7:5] – reserved<br>YMXA[4:3] – YUV/YCrCb selection:<br>“00” U = u, V = v<br>“01” U = 0.938u, V = 0.838v<br>“10” U = 0.563u, V = 0.714v<br>“11” U = 0.5u, V = 0.877v<br>YMXA[2:0] – Reserved<br><br><i>Note: This function is not available on the OV6130 image sensor.</i>   |
| 4E    | ARL        | A0 | RW | AEC/AGC reference level<br>ARL[7:5] – Voltage reference selection (Higher voltage = brighter final stable image)<br>“000” = Lowest reference level<br>“111” = Highest reference level<br>ARL[4:0] – Reserved   |

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| 4F    | YMXB       | 00 | RW | <p>YUV matrix control (Secondary)</p> <p>YMXB[7:6] – Y channel delay selection: 0 ~ 3tp</p> <p>YMXB[5] – reserved.</p> <p>YMXB[4] – UV 2tp delay selection</p> <p>YMXB[3] – reserved.</p> <p>YMXB[2] – Enable UV average mode.</p> <p>YMXB[1:0] – Color killer control. “00” no color kill, “11” strongest.</p> <p><i>Note: This function is not available on the OV6130 image sensor.</i></p>   |
| 50-53 | Rsvd 50-53 | xx | –  | Reserved   |
| 54    | COMQ       | 09 | RW | <p>Common control Q</p> <p>COMQ[7] – reserved.</p> <p>COMQ[6] – Central 1/4 image area rather whole image used to calculate AWB. “0” uses whole image area to calculate AWB.</p> <p>COMQ[5] – reserved.</p> <p>COMQ[4] - Select smart AWB. AWB algorithm will not count pixels with strong color.</p> <p>COMQ[3] – Enable AWB using manual input AWB registers when AWB is switched from manual to automatic control.</p> <p>COMQ[2] – reserved.</p> <p>COMQ[1:0] – Select the maximum AGC.</p> <p>“00” maximum gain=6dB, step 1/16</p> <p>“01” maximum gain=12dB, step 1/16</p> <p>“10” maximum gain=6dB, step 1/16</p> <p>“11” maximum gain=18dB, step 1/8</p> |
| 55-56 | Rsvd 55-56 | xx | RW | Reserved   |
| 57    | DBL        | 81 | RW | <p>Internal charge pump control</p> <p>DBL[7] – “0” disables internal charge pump. “1” enables internal charge pump.</p> <p>DBL[6:4] – selects the driving capability of internal charge pump. “000” is the smallest and “111” is the strongest.</p> <p>DBL[3] – “1” no VSYNC in the field that is dropped.</p> <p>DBL[2:0] – reserved.</p>  |
| 58    | Rsvd 58    | F5 | RW | Reserved   |
| 59    | OFC        | 00 | RW | <p>Dark current compensation</p> <p>OFC[7] – reserved</p> <p>OFC[6] – sign bit of the offset. “0” positive offset and “1” negative offset.</p> <p>OFC[5:0] – add an offset before AGC to compensate the dark current.</p>  |
| 5A    | SC         | 28 | RW | <p>Smart color control</p> <p>SC[7] – reserved</p> <p>SC[6] – select smart color. “1” indicates the color saturation will decrease with the increase of AGC.</p> <p>SC[5] – select the minimum color saturation in smart color option. “0” the minimum saturation is 40% of normal value. “1” the minimum saturation is 50% of normal value.</p> <p>SC[4:0] – reserved.</p>  |
| 5B    | SAWB       | 00 | RW | <p>Smart AWB control</p> <p>SAWB[7:4] – reserved</p> <p>SAWB[3:2] – Lowest chrominance level to be available for AWB control.</p> <p>SAWB[1:0] – highest chrominance level to be available for AWB control.</p>  |
| 5C    | Rsvd 5C    | 13 | RW | Reserved.  |