Advanced Information
Preliminary Datasheet

OV7680 Color CMOS VGA (640x480) CAMERACHIP™ Sensor with OmniPixel2™ Technology

General Description

The OV7680 CAMERACHIP™ image sensor is a low voltage CMOS device that provides the full functionality of a single-chip VGA camera and image processor in a small footprint package. The OV7680 provides full-frame, sub-sampled or windowed 8-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 30 frames per second (fps) in VGA with complete user control over image quality, formatting and output data transfer. Enabling 640x480 pixels to be output allows the user to perform image stabilization functions with post processing. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control and more, are also programmable through the SCCB interface. In addition, OmniVision sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise (FPN), smearing, blooming, etc., to produce a clean, fully stable color image.

Note: The OV7680 uses a lead-free package.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable apps
- Standard SCCB interface compatible with I2C interface
- Output support for Raw RGB, RGB565/444, ITU656 and YCbCr (4:2:2) formats
- Supports image sizes: VGA, CIF, and any size scaling down to CIF and QVGA from VGA
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB) and Automatic Black Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement) and anti-blooming
- ISP includes noise reduction and defect correction
- Lens shading correction
- Saturation level auto adjust
- Black level auto adjust
- Edge enhancement level auto adjust
- Output stream OFF mode

Ordering Information

Product	Package
OV07680-VL2A (Color, lead-free)	24-pin CSP2

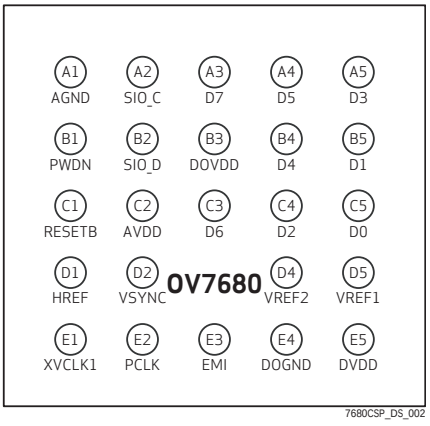
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Active Array Size		640 x 480
Power Supply	**Digital Core**	1.2VDC ±10%
	Analog	2.45V to 3.0V
	I/O	1.7V to 3.0V
Power Requirements	**Active**	80 mW typical (30fps VGA YCbCr format)
	Standby	< 20 µA
Temperature Range	**Operation**	-20°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • RGB565/444 • ITU656 • Raw RGB Data
Lens Size		TBD
Chief Ray Angle		TBD
Maximum Image Transfer Rate		30 fps for VGA
Sensitivity		560 mV/(Lux • sec)
S/N Ratio	**With De-noise**	TBD
	Without De-noise	TBD
Dynamic Range		TBD
Scan Mode		Progressive
Electronics Exposure		Up to 511:1 (for selected fps)
Pixel Size		2.2 µm x 2.2 µm
Dark Current		TBD
Well Capacity		TBD
Image Area		1443.2 µm x 1082.4 µm
Package Dimensions		3285 µm x 3485 µm

Figure 1 OV7680 Pin Diagram (Top View)



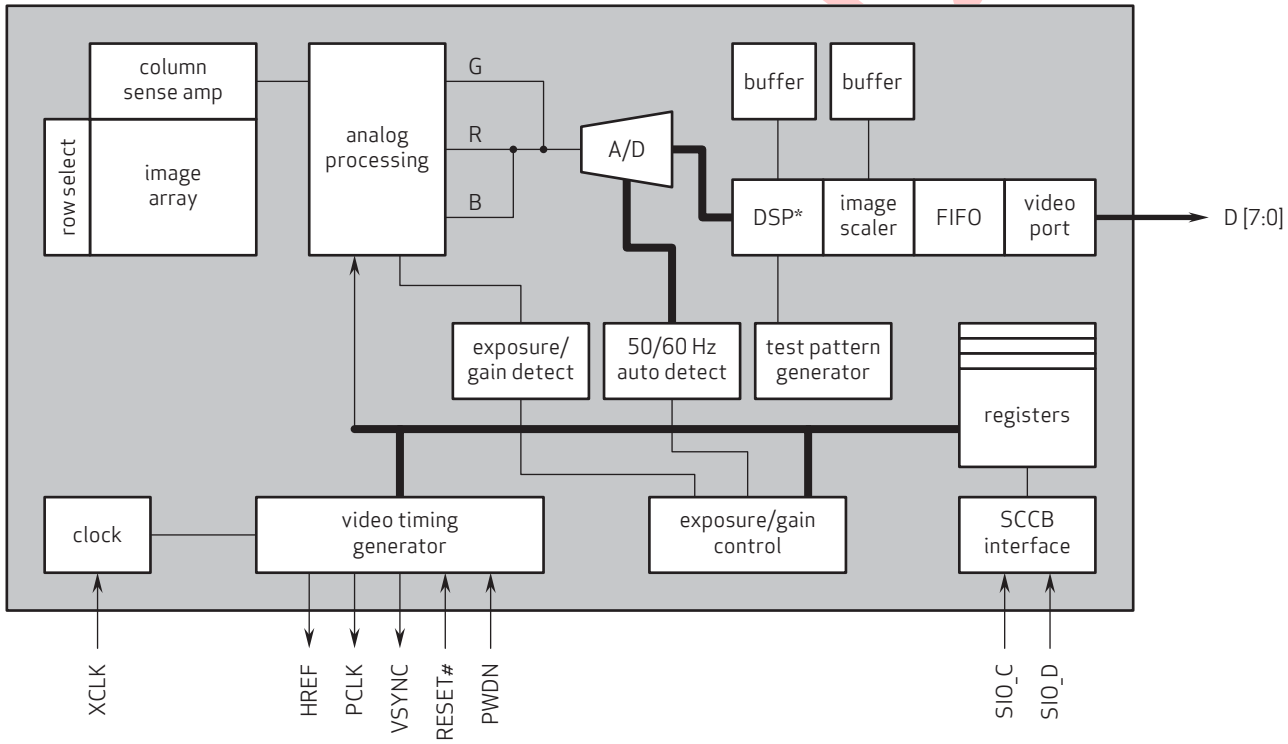
Version 1.0, December 22, 2006

Functional Description

Figure 2 shows the functional block diagram of the OV7680 image sensor. The OV7680 includes:

- Image Sensor Array (total array of 656 x 488 pixels, with active pixels 640 x 480 in YUV mode)
- Analog Signal Processor
- A/D Converter
- Test Pattern Generator
- Digital Signal Processor (DSP)
- Image Scaler
- Timing Generator
- Digital Video Port
- SCCB Interface

Figure 2 Functional Block Diagram



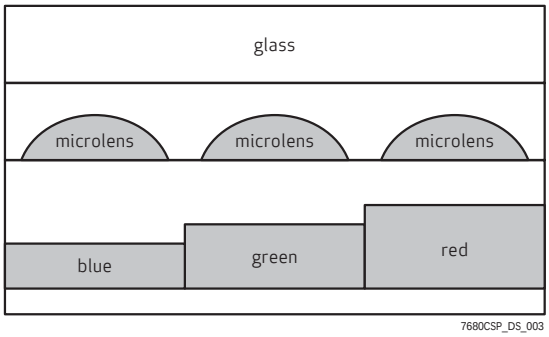
note 1 DSP* (lens shading correction, de-noise, white/black pixel correction, auto white balance, etc.)

7680CSP_DS_002

Image Sensor Array

The OV7680 sensor has an image array of 656 x 492 pixels for a total of 322,752 pixels, of which 640 x 480 pixels are active (307,200 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)

A/D Converter

After the Analog Processing block, the bayer pattern Raw signal is fed to a 10-bit analog-to-digital (A/D) converter shared by RGB channels. This A/D converter operates at speeds up to 13 MHz and is fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Black-Level Calibration (BLC)
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Test Pattern Generator

The Test Pattern Generator features the following:

- 8-bar color bar pattern
- Bit shift pattern

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Automatic White Balance (AWB)
- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- White/black pixel correction
- De-noise
- Lens shading correction
- Programmable gamma control
- Transfer 10-bit data to 8-bit

Image Scaler

This block controls all output and data formatting required prior to sending the image out. This block scales YCbCr/RGB output from VGA to CIF and QVGA.

Digital Video Port

Register bits REG0E[1:0] (0x0E) increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP sensor operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Function/Description
A1	AGND	Power	Analog ground
A2	SIO_C	Input	SCCB serial interface clock input
A3	D7	Output	YCbCr/RGB video component output bit[7]
A4	D5	Output	YCbCr/RGB video component output bit[5]
A5	D3	Output	YCbCr/RGB video component output bit[3]
B1	PWDN	Input (0)[a]	Power Down Mode Selection 0: Normal mode (default) 1: Power down mode
B2	SIO_D	I/O	SCCB serial interface data I/O
B3	DOVDD	Power	Digital power supply for I/O (1.7V ~ 3.0V)
B4	D4	Output	YCbCr/RGB video component output bit[4]
B5	D1[b]	Output	YCbCr/RGB video component output bit[1]
C1	RESETB	Input (1)[c]	Clears all registers and resets them to their default values. 0: Reset mode 1: Normal mode (default)
C2	AVDD	Power	Analog power supply
C3	D6	Output	YCbCr/RGB video component output bit[6]
C4	D2	Output	YCbCr/RGB video component output bit[2]
C5	D0	Output	YCbCr/RGB video component output bit[0]
D1	HREF	Output	HREF output
D2	VSYNC	Output	Vertical sync output
D4	VREF2	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
D5	VREF1	Reference	Reference voltage - connect to ground using a 0.1 µF capacitor
E1	XVCLK1	Input	System clock input
E2	PCLK	Output	Pixel clock output
E3	EMI		
E4	DOGND	Power	I/O ground
E5	DVDD	Power	Power supply (+1.2 VDC) for digital logic core

a. Input (0) represents an internal pull-down resistor.
b. D[7:0] for 8-bit YUV or RGB (D[7] MSB, D[0] LSB)
c. Input (1) represents an internal pull-up resistor.

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+0.5V
Lead-free Temperature, Surface-mount process		245ºC

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	2.45	2.75	3.0	V
V_{DD-C}	DC supply voltage – Core	–	1.08	1.2	1.32	V
V_{DD-IO}	DC supply voltage – I/O	–	1.7	–	3.0	V
I_{DDA}	Active (Operating) current	See Note [a]		14 + 15[b]		mA
$I_{DDS-SCCB}$	Standby current	See Note [c]		1		mA
$I_{DDS-PWDN}$	Standby current			10	20	µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [d]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 2.5V, V_{DD-C} = 1.2V, V_{DD-IO} = 2.5V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 30 fps YCbCr output, no I/O loading

b. I_{DD-IO} = 15mA, I_{DD-A} = 14mA, without loading

c. V_{DD-A} = 2.5V, V_{DD-C} = 1.2V, V_{DD-IO} = 2.5V
$I_{DDS-SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS-PWDN}$ refers to a PWDN pin-initiated Standby

d. Standard Output Loading = 25pF, 1.2KΩ

Table 4 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential non-linearity		± 1/2		LSB
	A/D Integral non-linearity		± 1		LSB
	AGC Range			24	dB
	Red/Blue adjustment range			12	dB
Inputs (PWDN, CLK, RESET#)					
f_{CLK}	Input clock frequency	6	13	24	MHz
t_{CLK}	Input clock period	TBD	TBD	TBD	ns
$t_{CLK:DC}$	Clock duty cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SIO_C}	Clock frequency			400	KHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_{AA}	SIO_C low to data out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	Data in hold time	0			µs
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
t_R, t_F	SCCB rise/fall times			300	ns
t_{DH}	Data out hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[7:0] (see Figure 5 and Figure 6)					
t_{PDV}	PCLK[↓] to data out valid			5	ns
t_{SU}	D[7:0] setup time	15			ns
t_{HD}	D[7:0] hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.2V, V_{DD-A} = 2.5V, V_{DD-IO} = 2.5V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 2.5V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

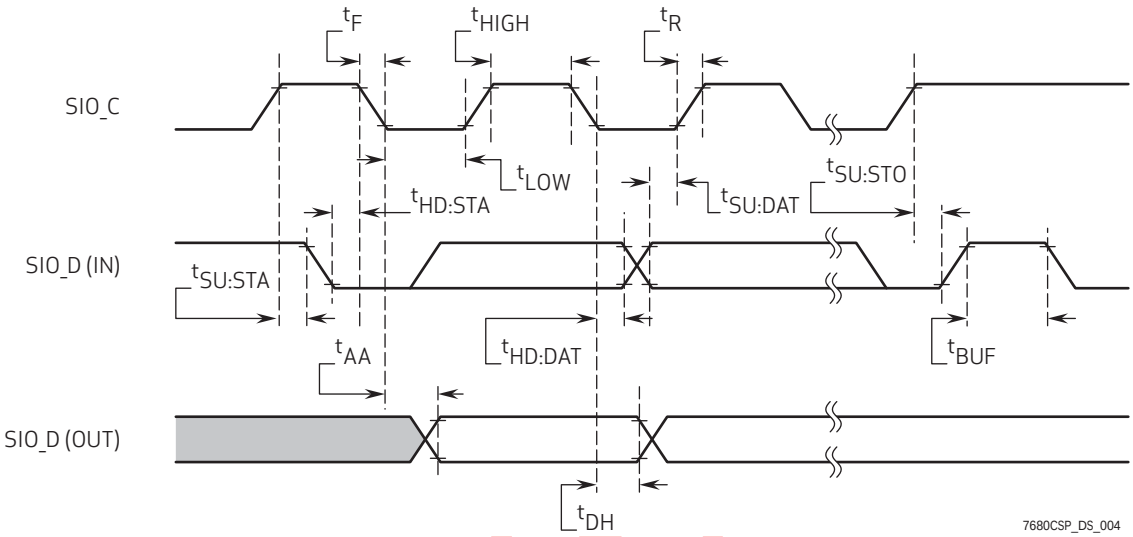


Figure 5 VGA Frame Timing (No Fixed)

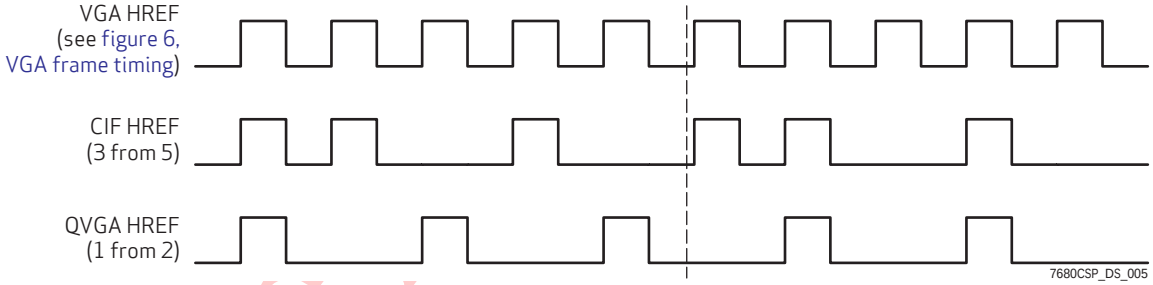
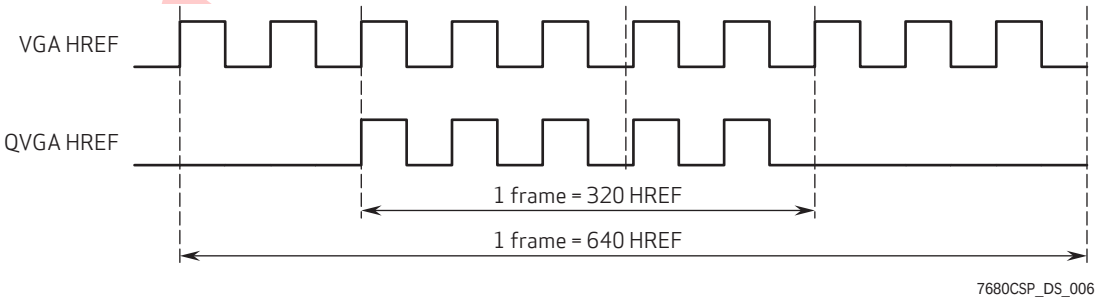


Figure 6 QVGA Frame Timing (No Fixed)



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV7680. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 42 for write and 43 for read.

Table 5 Device Control Register List (Sheet 1 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC – Gain Control 8 bits • Range: 1x to 32x Gain = (Bit[7]+1) × (Bit[6]+1) × (Bit[5]+1) × (Bit[4]+1) × (1+Bit[3:0]/16)
01	BGAIN	40	RW	AWB – Blue Gain Control • Range: 0 to 4x ([00] to [FF])
02	RGAIN	40	RW	AWB – Red Gain Control • Range: 0 to 4x ([00] to [FF])
03	GGAIN	40	RW	AWB – Green Gain Control • Range: 0 to 4x ([00] to [FF])
04	YAVG	00	R	Frame Average Level Automatically updated based on chip output format
05	BAVG	00	R	B Pixel Average Automatically updated based on chip output format
06	RAVG	00	R	R Pixel Average Automatically updated based on chip output format
07	GAVG	00	R	G Pixel Average Automatically updated based on chip output format
08-09	RSVD	XX	–	Reserved
0A	PIDH	76	R	Product ID Number MSB (Read only)
0B	PIDL	80	R	Product ID Number LSB (Read only)
0C	REG0C	00	RW	Register 0C Bit[7]: Vertical flip Bit[6]: Horizontal mirror Bit[5]: B and R swap when in RGB format Bit[4]: YU/YV swap when in YUV format Bit[3]: Reverse order of data bus Bit[2]: Clock output power down pin status 0: Tri-state data output pin at power down 1: Data output pin hold at last status before power down Bit[1]: Data output pin status selection at power down 0: Tri-state VSYNC, PCLK, HREF and CHSYNC pins upon power down 1: VSYNC, PCLK, HREF and CHSYNC pins hold at last status before power down Bit[0]: Enable color bar

Table 5 Device Control Register List (Sheet 2 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0D	REG0D	44	RW	Register 0D Bit[7]: Reserved Bit[6:4]: VS start point Bit[3]: Reserved Bit[2:0]: VS width
0E	REG0E	00	RW	Register 0E Bit[7:4]: Reserved Bit[3]: Sleep mode enable 0: Normal mode 1: Sleep mode Bit[2]: Output data range selection 0: Full range 1: Data from [10] to [F0] (8 MSBs) Bit[1:0]: Output drive current select 00: 1x 01: 2x 10: 3x 11: 4x
0F	AECH	00	RW	Automatic Exposure Control MSBs (see register AECL (0x10) for LSBs)
10	AECL	00	RW	Automatic Exposure Control LSBs AEC[15:0]: Exposure time TEX = $t_{LINE} \times$ AEC[15:0] ***Note:*** *The maximum exposure time is 1 frame period even if TEX is longer than 1 frame period.*
11	CLKRC	00	RW	Internal Clock Bit[7]: Internal frequency doublers ON/OFF switch 0: OFF 1: ON Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(PLL clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]

Table 5 Device Control Register List (Sheet 3 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	REG12	11	RW	Register 12 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: VarioPixel enable Bit[5]: IT656 protocol ON/OFF selection Bit[4]: Sensor original raw data output selection Bit[3:2]: RGB output format control 00: GBR 4:2:2 01: RGB565 10: RGB555 11: RGB444 Bit[1:0]: Output format control 00: YUV 01: Bayer RAW 10: RGB 11:Bayer RAW
13	REG13	00	RW	Register 13 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: Reserved Bit[5]: Banding filter ON/OFF Bit[4]: Enable AEC below banding value Bit[3]: Reserved Bit[2]: AGC auto/manual control selection Bit[1]: AWB auto/manual control selection Bit[0]: Exposure auto/manual control selection
14	REG14	32	RW	Register 14 Bit[7]: Reserved Bit[6:4]: Automatic gain ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101 Not allowed 110: Not allowed 111: Not allowed Bit[3]: Histogram/Average-based algorithm selection 0: Average-based 1: Histogram-based Bit[2]: Drop VSYNC output of corrupt frame Bit[1]: Auto set banding Bit[0]: Manually set banding 0: 60 Hz 1: 50 Hz

Table 5 Device Control Register List (Sheet 4 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	REG15	00	RW	Register 15 Bit[7]: Auto frame rate control ON/OFF selection Bit[6:4]: Auto frame rate max rate control 000: No reduction of frame rate 001: Max reduction to 2/3 frame rate 010: Max reduction to 1/2 frame rate 011: Max reduction to 1/3 frame rate 100: Max reduction to 1/4 frame rate 101 Max reduction to 1/6 frame rate 110: Max reduction to 1/8 frame rate 111: Max reduction to 1/12 frame rate Bit[3:0]: Reserved
16	REG16	08	RW	Register 16 Bit[7:4]: Reserved Bit[3:2]: Vertical window start line control 2 LSBs (8 MSBs are at register VSTART[7:0]) Bit[1:0]: Horizontal window start line control 2 LSBs (8 MSBs are at HSTART[7:0])
17	HSTART	1A	RW	Horizontal Window Start Point Control 8 MSBs (2 LSBs are at register REG16[1:0] (0x16))
18	HSize	A4	RW	Horizontal Sensor Size bit[8:1] Actual horizontal size = 2 × {HSize[7:0]. REG16[6]}
19	VSTART	03	RW	Vertical Window Start Point Control 8 MSBs (2 LSBs are at register REG16[3:2] (0x16))
1A	VSTOP	F2	RW	Vertical Sensor Size 8 bits Actual vertical size = 2 × VSize[7:0]
1B	RSVD	XX	–	Reserved
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E-1F	RSVD	XX	–	Reserved
20	REG20	00	RW	Register 20 Bit[7]: MSB for banding filter maximum step for 50 Hz light source (4 LSBs are in register AECGM[7:4]) Bit[6]: MSB for banding filter maximum step for 60 Hz light source (4 LSBs are in register AECGM[3:0]) Bit[5:0]: Manual banding counter
21	AECGM	44	RW	Bit[7:4]: Banding filter maximum step for 50 Hz light source Bit[3:0]: Banding filter maximum step for 60 Hz light source
22	REG22	00	RW	Register 22 Bit[7]: Optical black output selection 0: Disable 1: Enable Bit[6:0]: Reserved

Table 5 Device Control Register List (Sheet 5 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
23	RSVD	XX	–	Reserved
24	WPT	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	BPT	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: High nibble of upper limit of fast mode control zone Bit[3:0]: High nibble of lower limit of fast mode control zone
27	REG27	00	RW	Register 27 Bit[7]: Black sun enable (digital part) Bit[6:4]: Vertical window position adjustment (when center average is used) Bit[3]: Reserved Bit[2:0]: Horizontal window position adjustment (when center average is used)
28	REG28	00	RW	Register 28 Bit[7]: Output negative data Bit[7]: HREF changes to HSYNC Bit[7]: HSYNC reverse Bit[7]: HREF reverse Bit[7]: Reserved Bit[2]: VSYNC option 0: VSYNC changes on falling edge of PCLK 1: VSYNC changes on rising edge of PCLK Bit[1]: VSYNC negative Bit[0]: Reserved
29	PLL	A2	RW	PLL Control Bit[7:6]: PLL input control 00: 1x 01: 2x 10: 3x 11: 4x Bit[5:4]: PLL output control 00: Bypass PLL 01: 4x 10: 6x 11: 8x Bit[3]: Reset PLL Bit[2:0]: Reserved
2A	EXHCL	B0	RW	Bit[7]: Contrast center auto adjustment 0: Manual mode by setting YOFFSET[7:0] 1: Auto mode Bit[6:4]: 3 MSBs for dummy pixel insert in horizontal direction Bit[3:0]: Dummy line 4 MSBs
2B	EXHCH	0B	RW	8 LSBs for Dummy Pixel Insert in Horizontal Direction
2C	DM_LN	00	RW	Dummy Line 8 LSBs

Table 5 Device Control Register List (Sheet 6 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2D	ADVFL	00	RW	LSB for Dummy Line Insert in Vertical Direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB for Dummy Line Insert in Vertical Direction
2F	LC_TH1	04	RW	Lens Correction Lower Threshold Auto disable lens correction when luminance is less than LC_TH1[7:0]
30	LC_TH2	08	RW	Lens Correction Higher Threshold Auto enable lens correction when luminance is larger than LC_TH2[7:0]
31	LCC0	09	RW	Lens Correction Control 0 Bit[7:4]: Reserved Bit[3]: BLC offset cancellation enable Bit[2:1]: Reserved Bit[0]: Lens correction enable
32	LCC1	00	RW	X Coordinate of Lens Correction Center Relative to Array Center
33	LCC2	00	RW	Y Coordinate of Lens Correction Center Relative to Array Center
34	LCC3	80	RW	G Channel Compensation Coefficient
35	LCC4	60	RW	Radius of the Circular Section where no compensation applies
36	LCC5	80	RW	B Channel Compensation Coefficient
37	LCC6	80	RW	R Channel Compensation Coefficient
38	REG38	14	RW	Register 38 Bit[7]: Enable lens correction auto OFF when in low light 0: Disable 1: Enable Bit[6:4]: Stream off control VSYNC / Y / HREF / PCLK 3'b0xx: f f f f 3'b100: k k k f 3'b101: k k k k 3'b11x: hz hz hz hz *NOTE: "f" stands for "free running", 'k" stands for "keep last condition", and "hz" stands for "high impedence"* Bit[3:0]: Reserved
39-3D	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 7 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3E	REG3E	20	RW	Register 3E Bit[7]: Reserved Bit[6]: PCLK output gated 0: PCLK always output 1: PCLK output qualified by HREF Bit[5]: Reserved Bit[4]: PCLK output selection 0: When in RAW format 1: When in YUV format, PCLK will be double that of PCLK in RAW format Bit[3:0]: Reserved
3F	REG3F	44	RW	Register 3F Bit[7]: Reserved Bit[6]: HREF trigger option 0: HREF goes high on rising edge of PCLK 1: HREF goes high on falling edge of PCLK Bit[5:0]: Reserved
40	ARRAY0	00	RW	Bit[7:1]: Reserved Bit[0]: Black sun enable
41-42	RSVD	XX	–	Reserved
43	ARRAY3	41	RW	Bit[7:6]: Reserved Bit[5]: Reg sleep Bit[4:0]: Reserved
44-49	RSVD	XX	–	Reserved
4A	ANA1	00	RW	Bit[7:2]: Reserved Bit[1:0]: Pre-gain control 00: 1x 01: 1.1x 10: 1.3x 11: 1.5x
4B-4D	RSVD	XX	–	Reserved
4E	PWC3	5D	RW	Bit[7]: Bypass regulator 0: Do not bypass regulator 1: Bypass regulator Bit[6:0]: Reserved
4F	BD50st	9A	RW	50 Hz Banding AEC 8 bits
50	BD60st	80	RW	60 Hz Banding AEC 8 bits
51-59	RSVD	XX	–	Reserved
5A	UV_CTR0	01	RW	Slope of UV Curve
5B	UV_CTR1	FF	RW	Bit[7:6]: UV adjustment gain high threshold control 2 LSBs (3 MSBs are in register UV_CTR2[7:5] (0x5C)) Bit[5:0]: Y intercept point of UV curve

Table 5 Device Control Register List (Sheet 8 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
5C	UV_CTR2	1F	RW	Bit[7:5]: UV adjustment gain high threshold control 3 MSBs (2 MSBs are in register UV_CTR1[7:6] (0x5B)) Bit[4:0]: Manual UV adjustment
5D	UV_CTR3	00	RW	Bit[7:4]: UV adjustment gain low threshold control Bit[3:2]: Reserved Bit[1]: Center average selection 0: Choose whole image average value to system 1: Choose center-quarter average value to system Bit[0]: Reserved
5E-5F	RSVD	XX	–	Reserved
60	HSTG_L	60	RW	Low Luminance Threshold Value for Histogram-based Algorithm
61	HSTG_H	80	RW	High Luminance Threshold Value for Histogram-based Algorithm
62	REG62	00	RW	Bit[7]: Bit shift test pattern output enable Bit[6]: Reserved Bit[5:4]: Output select 00: Normal output 10: Bit shift test pattern output x1: Reserved Bit[3:0]: Reserved
63	EV_CTL	08	RW	Bit[7]: Sleep control option Bit[6:2]: Reserved Bit[1:0]: Digital gain select 00: Choose AGC[5:4] as digital gain 01: Choose AGC[6:5] as digital gain 1x: Choose AGC[7:6] as digital gain
64-65	RSVD	XX	–	Reserved
66	BLC6	02	RW	Bit[7:3]: Reserved Bit[2:0]: BLC Targ[2:0]
67-6E	RSVD	XX	–	Reserved
6F	REG6F	40	RW	Register 6F Bit[7]: Reset enable/disable when sensor 's working mode changes 0: Sensor timing does not reset when mode changes 1: Sensor timing resets when mode changes Bit[6:0]: Reserved
70-7F	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Sheet 9 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
80	REG80	7E	RW	Register 80 Bit[7]: VarioPixel enable 0: Disable 1: Enable Bit[6]: Color interpolation enable 0: Disable 1: Enable Bit[5]: Black pixel correction enable 0: Disable 1: Enable Bit[4]: White pixel correction enable 0: Disable 1: Enable Bit[3]: Gamma control enable 0: Disable 1: Enable Bit[2]: AW gain apply enable 0: Disable 1: Enable Bit[1]: AWB control enable 0: Disable 1: Enable Bit[0]: Black level auto adjust enable 0: Disable 1: Enable
81	REG81	0C	RW	Register 81 Bit[7]: Vertical zoom out enable 0: Disable 1: Enable Bit[6]: Down-sampling vertical enable 0: Disable 1: Enable Bit[5]: Horizontal zoom out enable 0: Disable 1: Enable Bit[4]: Down-sampling horizontal enable 0: Disable 1: Enable Bit[3]: Reserved Bit[2]: Color matrix enable 0: Disable 1: Enable Bit[1]: Special digital effects (SDE) enable 0: Disable 1: Enable Bit[0]: UV auto adjust enable 0: Disable 1: Enable

Table 5 Device Control Register List (Sheet 10 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
82	REG82	18	RW	Register 82 Bit[7:4]: Reserved Bit[3]: DSP YUV422 enable 0: Disable 1: Enable Bit[2]: UV auto average enable 0: Disable 1: Enable Bit[1:0]: DSP output format select 0x: YUV422 10: RAW8 11: RAW10
83	REG83	08	RW	Register 83 Bit[7:1]: Reserved Bit[0]: Color bar enable
84-8A	RSVD	XX	–	Reserved
8B	REG8B	12	RW	Register 8B Bit[7]: AWB_SIMPLE Bit[6:0]: Reserved
8C-9F	RSVD	XX	–	Reserved
A0	GAM1	10	RW	Gamma Curve 1st Segment Input End Point 0x04 Output Value
A1	GAM2	12	RW	Gamma Curve 2nd Segment Input End Point 0x08 Output Value
A2	GAM3	35	RW	Gamma Curve 3rd Segment Input End Point 0x10 Output Value
A3	GAM4	5A	RW	Gamma Curve 4th Segment Input End Point 0x20 Output Value
A4	GAM5	69	RW	Gamma Curve 5th Segment Input End Point 0x28 Output Value
A5	GAM6	76	RW	Gamma Curve 6th Segment Input End Point 0x30 Output Value
A6	GAM7	80	RW	Gamma Curve 7th Segment Input End Point 0x38 Output Value
A7	GAM8	88	RW	Gamma Curve 8th Segment Input End Point 0x40 Output Value
A8	GAM9	8F	RW	Gamma Curve 9th Segment Input End Point 0x48 Output Value
A9	GAM10	96	RW	Gamma Curve 10th Segment Input End Point 0x50 Output Value
AA	GAM11	A3	RW	Gamma Curve 11th Segment Input End Point 0x60 Output Value
AB	GAM12	AF	RW	Gamma Curve 12th Segment Input End Point 0x70 Output Value
AC	GAM13	C4	RW	Gamma Curve 13th Segment Input End Point 0x90 Output Value
AD	GAM14	D7	RW	Gamma Curve 14th Segment Input End Point 0xB0 Output Value
AE	GAM15	E8	RW	Gamma Curve 15th Segment Input End Point 0xD0 Output Value
AF	SLOPE	20	RW	Gamma Curve Highest Segment Slope – calculated as follows: SLOPE[7:0] = (0x100 – GAM15[7:0]) × 4/3

Table 5 Device Control Register List (Sheet 11 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
B0	RSVD	XX	–	Reserved
B1	REGB1	00	RW	Register B1 Bit[7:5]: Reserved Bit[4:0]: Bad pixel correction control
B2	REGB2	08	RW	De-noise Control Magnitude
B3	REGB3	04	RW	Register B3 Bit[7]: Reserved Bit[6]: Sharpness auto control upper limit 1 LSB (see REGB6[7:4] for 4 MSBs) Bit[5]: Sharpness auto control lower limit 1 LSB (see REGB6[3:0] for 4 MSBs) Bit[4:0]: Sharpness magnitude
B4	REGB4	06	RW	Register B4 Bit[7]: Reserved Bit[6]: Sharpness control 0: Auto 1: Manual Bit[5]: De-noise control 0: Auto 1: Manual Bit[4]: Reserved Bit[3:0]: Sharpness threshold
B5	REGB5	10	RW	De-noise Auto Control Lower Limit
B6	REGB6	1F	RW	Register B6 Bit[7:4]: Sharpness auto control upper limit 4 MSBs (see REGB3[6] for LSB) Bit[3:0]: Sharpness auto control lower limit 4 MSBs see REGB3[5] for LSB)
B7	MX1	2C	RW	Matrix Coefficient 1
B8	MX2	24	RW	Matrix Coefficient 2
B9	MX3	08	RW	Matrix Coefficient 3
BA	MX4	14	RW	Matrix Coefficient 4
BB	MX5	24	RW	Matrix Coefficient 5
BC	MX6	38	RW	Matrix Coefficient 6

Table 5 Device Control Register List (Sheet 12 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
BD	REGBD	1E	RW	Register BD Bit[76]: Matrix double ON/OFF selection 0: OFF 1: ON Bit[6]: Select color matrix 1 0: Selected 1: Not selected Bit[5]: Sign bit for MX6 (0xBC) Bit[4]: Sign bit for MX5 (0xBB) Bit[3]: Sign bit for MX4 (0xBA) Bit[2]: Sign bit for MX3 (0xB9) Bit[1]: Sign bit for MX2 (0xB8) Bit[0]: Sign bit for MX1 (0xB7)
BE-CF	RSVD	XX	–	Reserved
D0	REGD0	A4	RW	Image Scaler Horizontal Input Size 8 MSBs - IH[9:2]
D1	REGD1	78	RW	Image Scaler Vertical Input Size 7 MSBs - IV[8:2]
D2	REGD2	A0	RW	Image Scaler Horizontal Output Size 8 MSBs - OH[9:2]
D3	REGD3	78	RW	Image Scaler Vertical Output Size 7 MSBs - OV[8:2]
D4	REGD4	20	RW	Register D4 Bit[7:6]: Image scaler horizontal input size 2 LSBs - IH[1:0] Bit[5:4]: Image scaler vertical input size 2 LSBs - IV[1:0] Bit[3:2]: Image scaler horizontal output size2 LSBs - OH[1:0] Bit[1:0]: Image scaler vertical output size 2 LSBs - OV[1:0]

Table 5 Device Control Register List (Sheet 13 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
D5	SDE	00	RW	Special Digital Effects Bit[7]: Fixed Y value enable - Y is set by register YOFFSET (0xD8) 0: Disabled 1: Enabled Bit[6]: Negative enable 0: Disabled 1: Enabled Bit[5]: Gray enable 0: Disabled 1: Enabled Bit[4]: Fixed V value enable - V is set by register FIXEDV (0xDE) 0: Disabled 1: Enabled Bit[3]: Fixed U value enable - U is set by register FIXEDU (0xDD) 0: Disabled 1: Enabled Bit[2]: Contrast enable - refer to register CNTRS (0xD7) for details 0: Disabled 1: Enabled Bit[1]: Saturation enable - refer to registers USAT (0xDB) and VSAT (0xDC) for details 0: Disabled 1: Enabled Bit[0]: Hue enable - refer to registers HUECOS (0xD9) and HUESIN (0xDA) for details 0: Disabled 1: Enabled
D6	BRIGHTNESS	00	RW	Bit[7:0]: Brightness control for SDE function
D7	CNTRS	20	RW	Contrast Level Control
D8	YOFFSET	00	RW	Bit[7:0]: Y offset for SDE function when SDE[7] (0xD5) is 1; Contrast center when SDE[2] (0xD5) is 1 and SDE[7] (0xD5) is 0 $Y = Y0 + \left(SGNSET[3]YOFFSET \times \left(\frac{CNTRS}{0x20}\right)\right) + SGNSET[2]BRIGHTNESS$
D9	HUECOS	80	RW	DSP Control 10 Bit[7:0]: Hue control parameter (HUECOS), effective when SDE[0] (0xD5) is 1
DA	HUESIN	00	RW	DSP Control 11 Bit[7:0]: Hue control parameter (HUESIN), effective when SDE[0] (0xD5) is 1

Table 5 Device Control Register List (Sheet 14 of 14)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
DB	USAT	40	RW	DSP Control 12 Bit[7:0]: U component saturation control, effective when SDE[1] (0xD5) is 1 $U = \frac{U_0 \times USAT[7:0]}{0x40}$
DC	VSAT	40	RW	DSP Control 13 Bit[7:0]: V component saturation control, effective when SDE[1] (0xD5) is 1 $V = \frac{V_0 \times VSAT[7:0]}{0x40}$
DD	FIXEDU	80	RW	Bit[7:0]: U channel fixed value output, effective when SDE[3] (0xD5) is 1
DE	FIXEDV	80	RW	Bit[7:0]: V channel fixed value output, effective when SDE[4] (0xD5) is 1
DF	SGNSET	01	RW	Register DF Bit[7:6]: Reserved Bit[5:0]: SgnSet Hue: sgn0 = 1, sgn1 = 0, sgn4 = sgn5 = 0 → 0 < θ < π/2 sgn0 = 0, sgn1 = 1, sgn4 = sgn5 = 0 → π/2 < θ < 0 sgn0 = 1, sgn1 = 0, sgn4 = sgn5 = 1 → π/2 < θ < π sgn0 = 0, sgn1 = 1, sgn4 = sgn5 = 1 → π < θ < -π/2 YContrast: sign2: YOFFSET sign3: BRIGHTNESS
E0-E2	RSVD	XX	–	Reserved
E3	REGE3	00	RW	Reg_Addr
E4	REGE4	–	R	Reg_Dout
E5	RSVD	XX	–	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV7680 uses a 24-ball Chip Scale Package 2 (CSP2). Refer to Figure 7 for package information, Table 6 for package dimensions and Figure 8 for the array center on the chip.

Note: For OVT devices that are lead-free, all part marking letters are lower case. Underlining the last digit of the lot number indicates CSP2 is used.

Figure 7 OV7680 Package Specifications

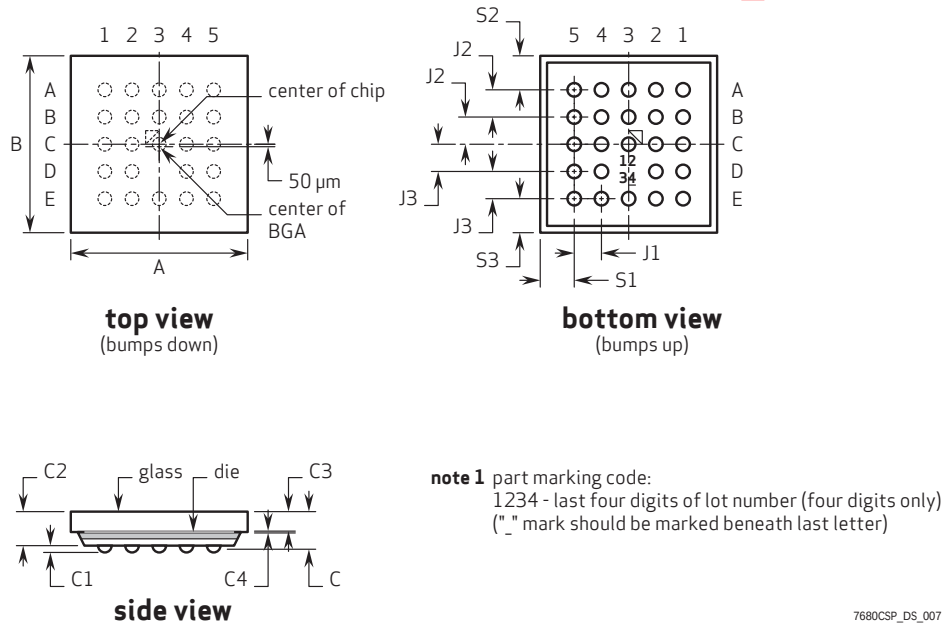
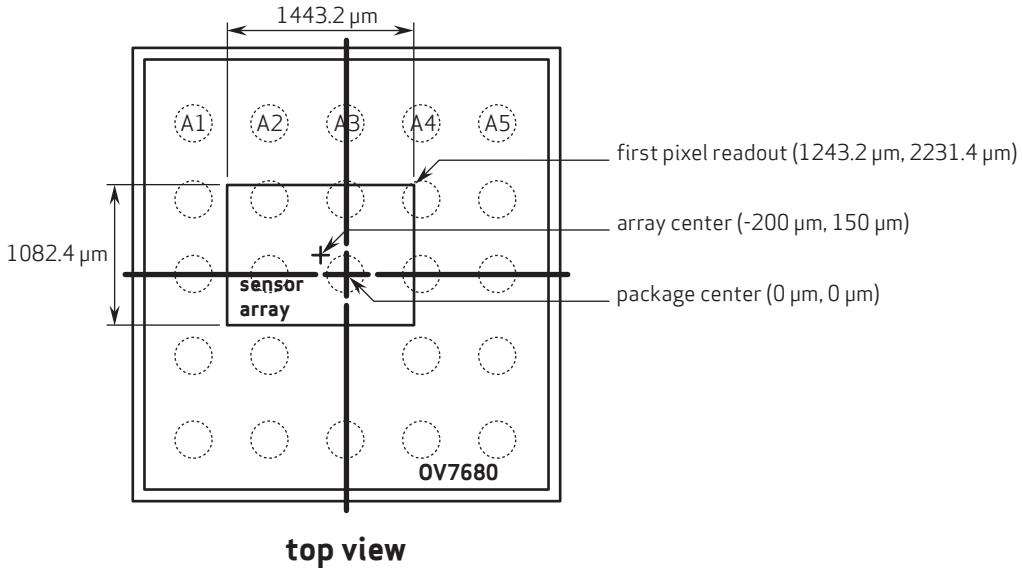


Table 6 OV7680 Package Dimensions

Parameter	Symbol	Minimum	Nominal	Maximum	Unit
Package body dimension X	A	3260	3285	3310	µm
Package body dimension Y	B	3460	3485	3510	µm
Package height	C	825	885	945	µm
Ball height	C1	130	160	190	µm
Package body thickness	C2	680	725	770	µm
Cover glass thickness	C3	375	400	425	µm
Airgap between cover glass and sensor	C4	30	45	60	µm
Ball diameter	D	270	300	330	µm
Total pin count	N		24		
Pin count X-axis	N1		5		
Pin count Y-axis	N2		5		
Pins pitch X-axis	J1		600		µm
Pins pitch Y-axis	J2		600		µm
Pins pitch Y-axis	J3		650		µm
Edge-to-pin center distance analog X	S1	412.5	442.5	472.5	µm
Edge-to-pin center distance analog Y	S2	512.5	542.5	572.5	µm
Edge-to-pin center distance analog Y	S3	412.5	442.5	472.5	µm

Sensor Array Center

Figure 8 OV7680 Sensor Array Center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

7680CSP_DS_008

IR Reflow Ramp Rate Requirements

OV7680 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case.

Figure 9 IR Reflow Ramp Rate Requirements

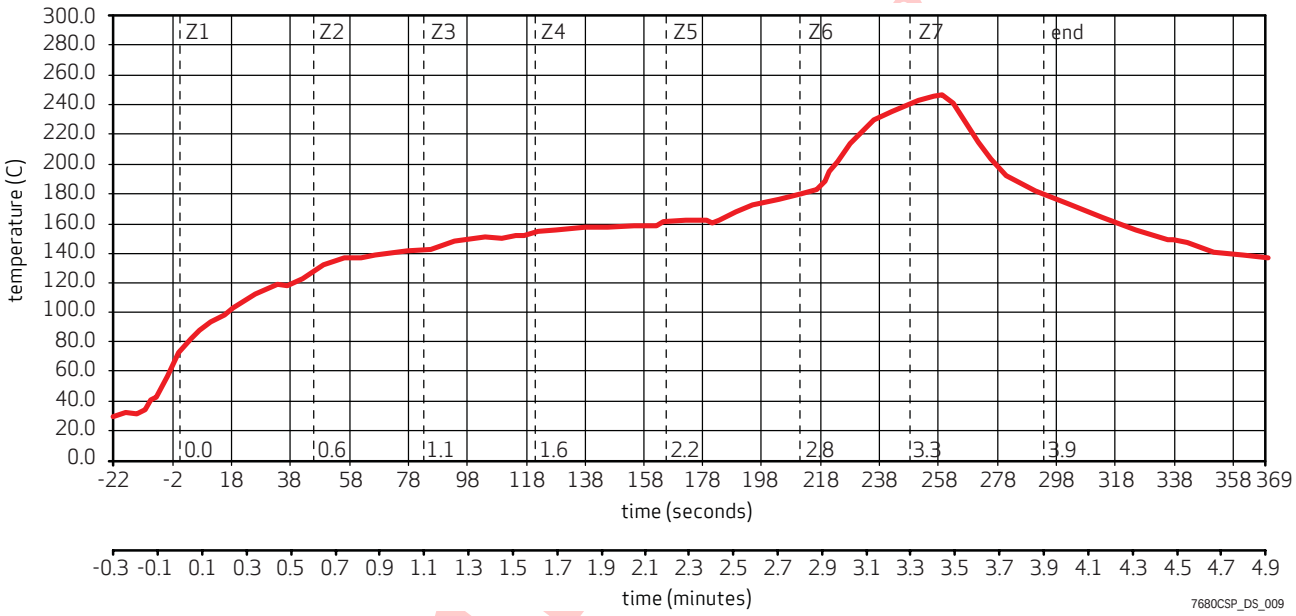


Table 7 Reflow Conditions

Condition	Exposure
Average ramp-up rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak temperature	245°C
Cool-down rate (peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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