OV7930 Color CMOS Analog CAMERACHIP™

General Description

The OV7930 (color) is a high performance quarter-inch CMOS CAMERACHIP™ designed for all applications requiring a small footprint, low voltage, low power consumption and low cost color video camera.

The device supports NTSC composite video output and can directly interface with a VCR TV monitor or other 75 ohm terminated input with 2X standard TV signal range. The OV7930 CAMERACHIPs require only a single 5-volt DC power supply and have been designed for very low power operation.

Features

- Single chip 1/4" lens video camera
- Composite video: NTSC
- Sensitivity boost (+27 dB)/AGC ON/OFF
- Automatic exposure/gain/white balance
- External frame sync capability
- Aperture correction
- SCCB programmable controls:
  - Color saturation
  - Brightness
  - Hue
  - White balance
  - Exposure
  - Gain
  - Gamma curve
  - Aperture correction
- Gamma correction (0.45) ON/OFF
- Low power consumption
- +5 volt only power supply
- Wide dynamic range, anti-blooming, zero smearing

Ordering Information

Product	Packages
OV7930 (Color, VGA, NTSC, CVO)	CLCC-28, PLCC-28

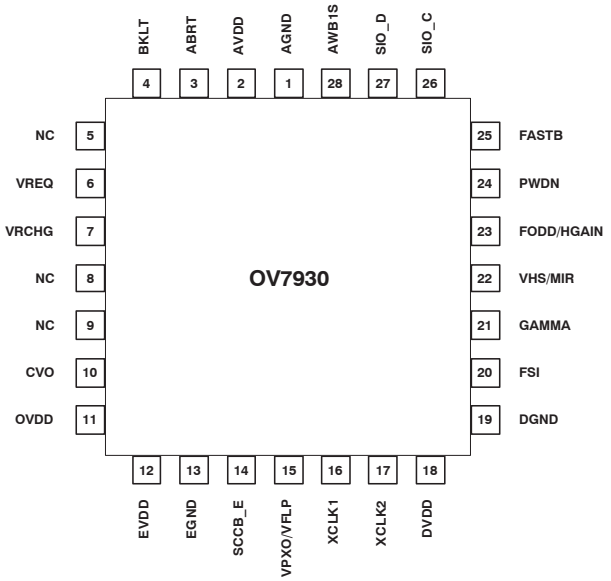
Applications

- Video Conferencing
- Video Phones
- Video E-mail
- PC Multimedia
- Toys
- Security
- Surveillance
- Finger Printing
- Medical and Dental Equipment

Key Specifications

Array Size		510 x 492
Power Supply		5 VDC ± 5%
Power Requirements	**Without Loading**	20 mA
	With 75 ohm Loading	< 35 mA
Image Area		4.00 mm x 3.08 mm
Auto Electronic Exposure Time		1/60s - 6.3µs
Minimum Illumination (3000K)		< 2.0 Lux
S/N Ratio		> 46 dB
Dynamic Range		> 70 dB
Pixel Size		7.86 µm x 6.25 µm
Dark Current		< 100 mV/s
Fixed Pattern Noise		< 0.03% $V_{PEAK-TO-PEAK}$
Package Dimensions		0.45 in. x 0.45 in.

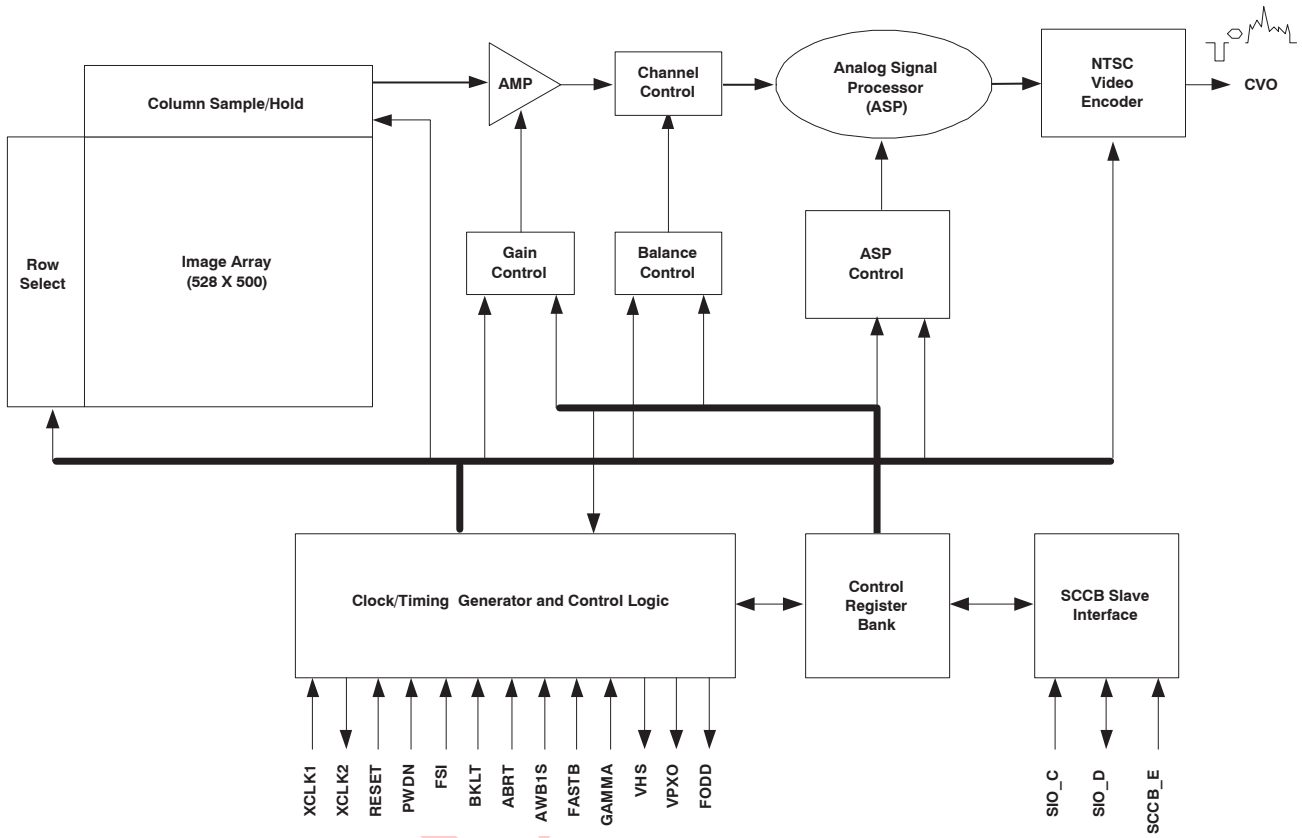
Figure 1 OV7930 Pin Diagram



Functional Description

This section describes the various functions of the OV7930. Refer to Figure 2 for the functional block diagram of the OV7930.

Figure 2 Functional Block Diagram



Video Standards

NTSC TV standards are implemented and available as output in the OV7930 CAMERACHIP. Note that the accuracy and stability of the crystal clock frequency is important to avoid unwanted color shift in the TV video system. A 14.31818 MHz crystal is recommended when using the OV7930 CAMERACHIP.

Video Format

The OV7930 CAMERACHIP supports Composite (CVBS) video format only. Composite signals are generated from the built-in NTSC TV encoder.

Image Sensor Functions

White Balance

The function of white balance in the OV7930 CAMERACHIP is to adjust and calibrate the image device sensitivity on the primary (RGB) colors to match the color cast of the light source. The Auto White Balance (AWB) can be enabled or disabled by SCCB register bit COMD[1] (see "COMD" on page 12).

Mirror and Vertical Flip

The OV7930 has pin control functions:

- Mirror (pin22 - see "VHS/MIR" on page 4)
- VFLIP (pin 15 input - see "VPXO/VFLP" on page 4)

These two functions can be controlled separately using SCCB register bit COME[6] (see "COME" on page 12) for the mirror function and register bit COMJ[0] (see "COMJ" on page 13) for the vertical flip function.

Multi-Chip Synchronize

The OV7930 CAMERACHIP provides the multi-chip Synchronize function where one chip works as the master and all others as slave devices. The master chip provides the frame synchronize signal through the FODD pin (pin 23 - see "FODD/HGAIN" on page 5). All slave devices accept the frame synchronize signal through the FSI pin (pin 20 - see "FSI" on page 4). This mode allows all devices to synchronize together.

Chip Configuration

The OV7930 CAMERACHIP has been designed for ease-of-use in many stand-alone applications. Most of the on-chip functions are configurable by connecting the appropriate pins high (logic "1") or low (logic "0") through a 10 KΩ resistor. The CAMERACHIP reads the input pins at power up which enable user-defined default configurations.

The OV7930 CAMERACHIP also has a SCCB slave interface for programmable access to all registers functions. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

NOTE Once the SCCB interface is enabled (pin 14 - see "SCCB_E" on page 4), the following pin assignment functions will be ignored and functions will be defined by the related SCCB register. These pins are:

- ABRT (pin 3)
- BKLT (pin 4)
- VFLIP (pin 15)
- GAMMA (pin 21)
- MIR (pin 22)
- HGAIN (pin 23)
- FASTB (pin 25)

Additional Picture Controls

The OV7930 CAMERACHIP provides additional picture control functions to enhance image quality and chip performance.

Automatic Gain Control (AGC)

The default gain range is 1x - 8x while the user can set the gain range up to 4x or 16x.

Brightness Control

Brightness can be controlled either by internal automatic algorithms or by the user through the following SCCB register bits:

- BRT[7:0] (see "BRT" on page 11)

Gamma Correction

The OV7930 has luminance and chrominance Gamma correction through the GAMMA pin (pin 21 - see "GAMMA" on page 4).

Backlight Control

The OV7930 manages backlight conditions through register bit COME[4] (see "COME" on page 12).

Color Saturation

Color saturation can be updated manually through the SCCB register bits SAT[7:4] (see "SAT" on page 11).

Hue Adjustment

Image hue can be adjusted through the SCCB register bits HUE[5:0] (see "HUE" on page 11).

Pin Description

Table 1 Pin Description

Pin Number	Name	Pin Type	Default (V)	Function/Description
01	AGND	Power	0	Analog ground
02	AVDD	Power	5	Analog Power (+5 VDC)
03	ABRT	Input	0	Auto brightness control ON/OFF
04	BKLT	Input	0	Backlight selection 0: OFF 1: ON
05	NC	—	—	No connection
06	VREQ	Analog	2.5	Internal reference
07	VRCHG	Analog	3.6	Internal reference
08	NC	—	—	No connection
09	NC	—	—	No connection
10	CVO	Output	—	Composite video output, 2X standard NTSC TV signal
11	OVDD	Power	5	Analog power for video output (+5 VDC)
12	EVDD	Power	5	Analog power (+5 VDC)
13	EGND	Power	0	Analog ground
14	SCCB_E	Input	5	SCCB interface enable signal, active low
15	VPXO/VFLP	I/O	0	Valid pixels detect output. CLK is asserted on this pin during the active image period. Power up initial pin value will be latched as vertical flip ON/OFF control. 0: OFF 1: ON
16	XCLK1	Input	—	Crystal clock input. 14.31818 MHz for NTSC
17	XCLK2	Output	—	Crystal clock output
18	DVDD	Power	5	Digital power (+5 VDC)
19	DGND	Power	0	Digital ground
20	FSI	Input	0	Frame synchronizing signal input
21	GAMMA	Input	5	Gamma function ON/OFF 0: OFF 1: ON
22	VHS/MIR	I/O	0	Vertical/Horizontal SYNC output. Power up initial pin value will be latched as mirror function ON/OFF control. 0: OFF 1: ON

Table 1 Pin Description

Pin Number	Name	Pin Type	Default (V)	Function/Description
23	FODD/HGAIN	I/O	0	Even/odd field flag and frame synchronize signal output. Power up initial pin value will be latched as AGC gain range control. 0: AGC gain 1x - 4x 1: AGC gain 1x - 8x
24	PWDN	Input	0	Power down mode selection 0: OFF 1: ON
25	FASTB	Input	0	AEC/AGC mode selection 0: Fast mode 1: Normal mode
26	SIO_C	Input	—	SCCB serial interface clock
27	SIO_D	I/O	—	SCCB serial interface data I/O
28	AWB1S	Input	0	After power up, first high pulse edge will trigger one shot AWB. System performs fast AWB only when this pin is high at this mode.

Electrical Characteristics

Table 2 Operating Conditions

Parameter	Min	Max	Unit
Operating temperature	0	40	°C
Storage temperature	-40	125	°C
Operating humidity	TBD	TBD	
Storage humidity	TBD	TBD	

Table 3 DC Electrical Characteristics (0°C ≤ T_A ≤ 85°C)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
V_{DD}	Supply voltage (AVDD, DVDD, OVDD, EVDD)	4.75	5	5.25	V
I_{DD}	Supply current in VDDs (without loading)	—	20	—	mA
Digital Inputs					
V_{IL}	Input voltage LOW			1.0	V
V_{IH}	Input voltage HIGH	3.5			V
C_{IN}	Input capacitor			10	pF
Digital Outputs					
V_{OH}	Output voltage HIGH	4			V
V_{OL}	Output voltage LOW			0.6	V
SCCB (SIO_C and SIO_D)					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	3.5	5	V_{DD} ± 0.5	V

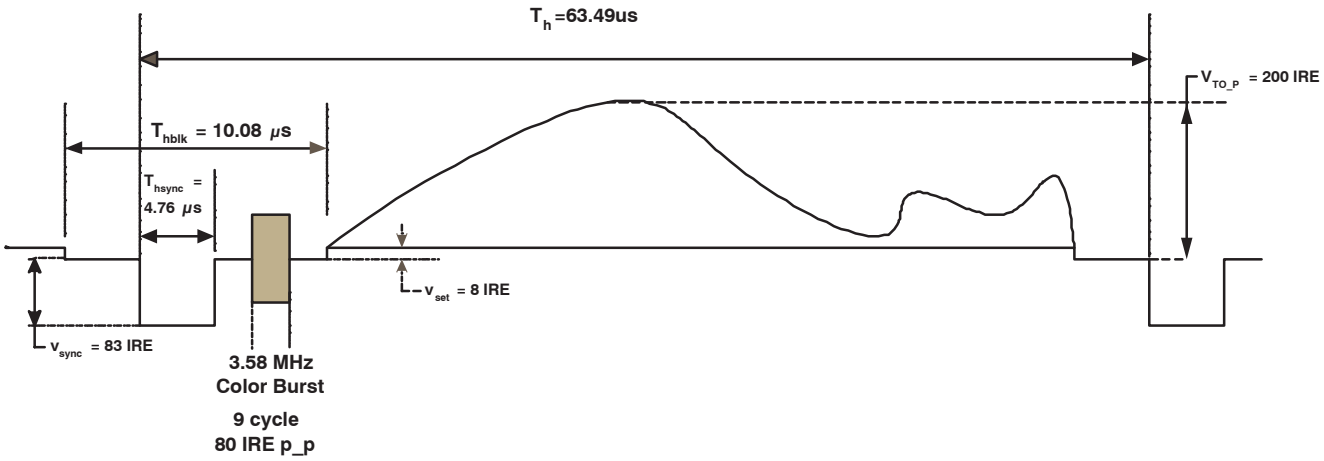
Table 4 AC Characteristics (T_A = 25°C, V_{DD} = 5V)

Symbol	Parameter	Min	Typ	Max	Unit
Clock Input/Crystal Oscillator					
f_{OSC}	Resonator frequency	—	14.31818	—	MHz
	Load capacitor		33		pF
	Parallel resistance		1		MΩ
	Rise/fall time for external clock input	—	5	—	ns
	Duty cycle for external clock input	40	50	60	%
CVO Analog Video Output Parameters					
V_{TO_P}	Video peak signal level	—	2.0	—	V
V_{TO_B}	Video black signal level	—	0.58	—	V
V_{SYNC}	Video sync pulse amplitude	—	0.58	—	V
Ro	Video output load	—	75	—	Ω
I/O Pin					
I_{source}	Output pin source current (Output = 1.5v)	8	10	12	mA
I_{sink}	Output pin sink current (Output = 3v)	8	10	12	mA
Miscellaneous Timing					
t_{SYNC}	External FSI cycle time	—	2	—	field
t_{PU}	Chip power up time	—	—	100	µs
t_{PD}	Power up delay time	—	10	—	µs
t_{PZ}	Power up low-z delay	—	1000	—	µs

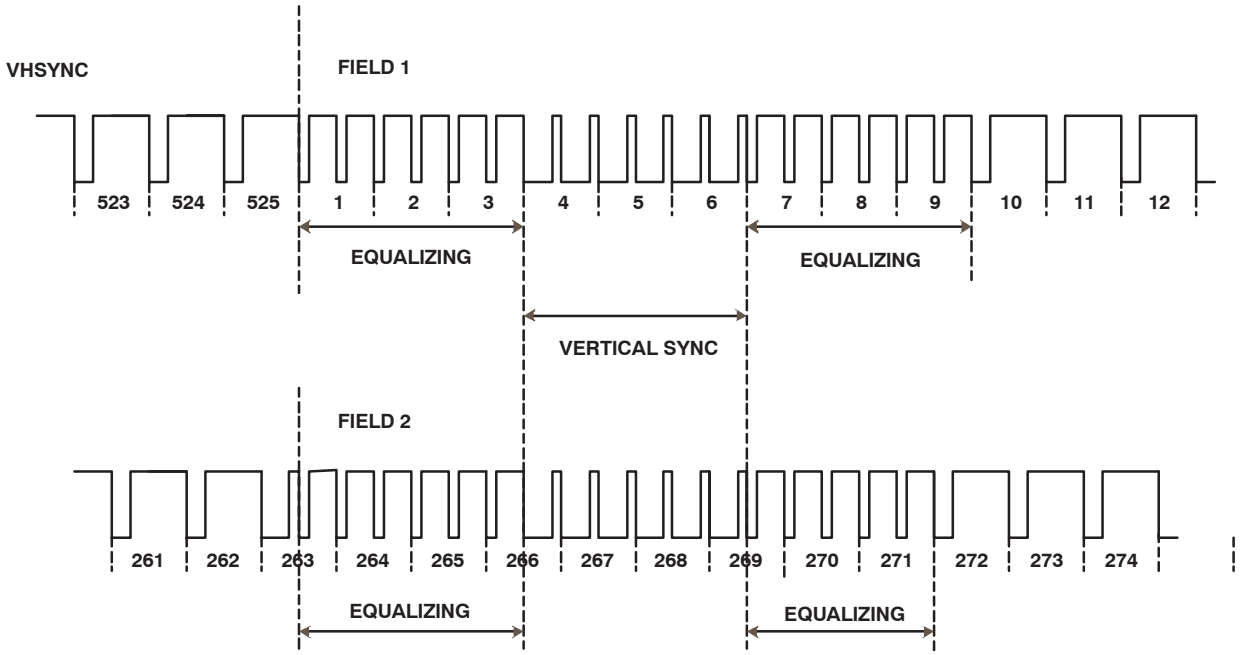
Timing Specifications

The OV7930 timing is standard NTSC TV timing. Figure 3 shows the NTSC timing and signal range. The OV7930 outputs 2X standard TV signals.

Figure 3 NTSC Timing and Signal Range



(A) HORIZONTAL TIMING FOR NTSC



(B) VERTICAL TIMING FOR NTSC

Figure 4 SCCB Timing Diagram

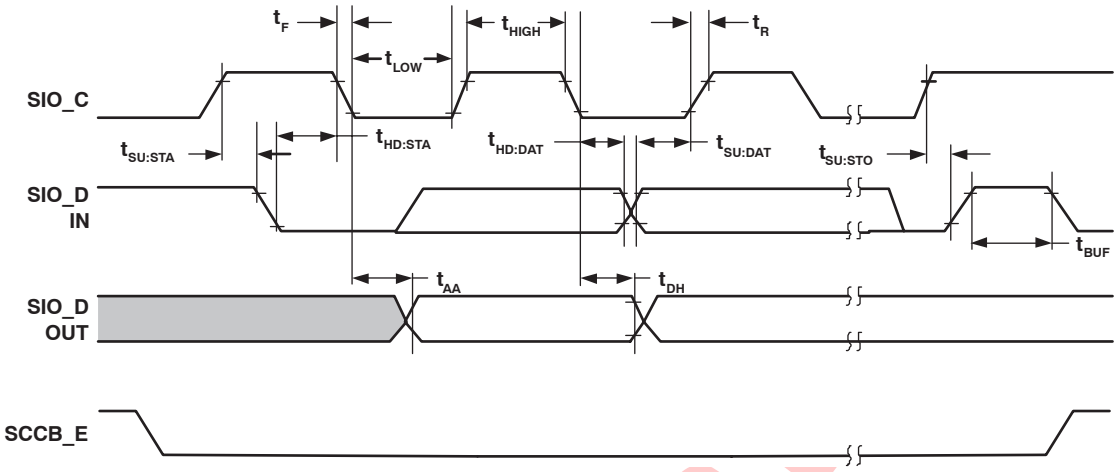
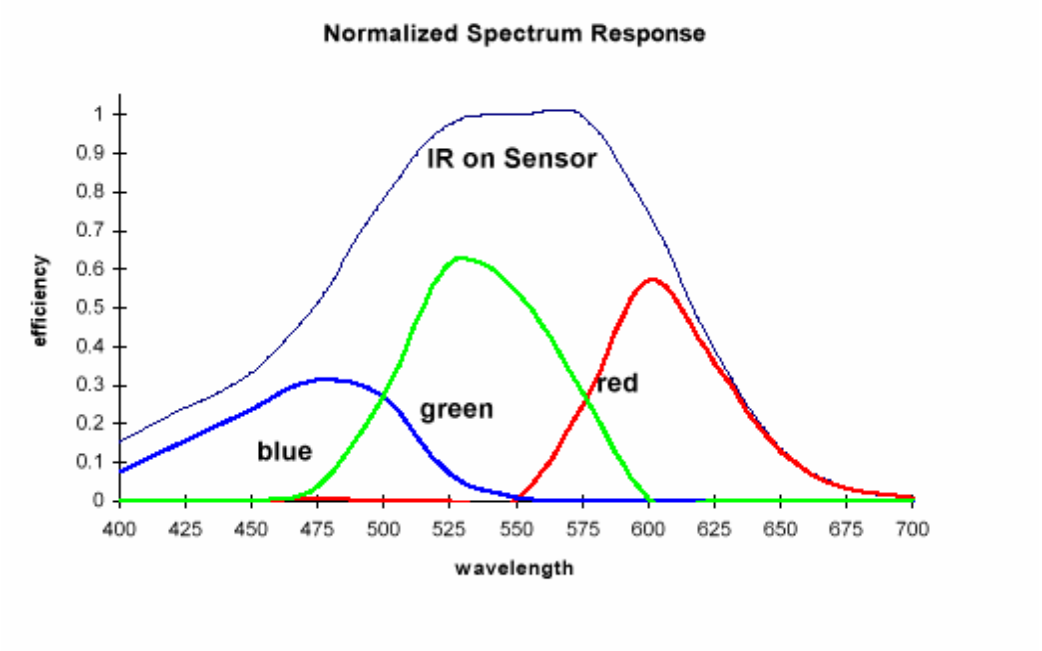


Table 5 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
$t_{R,}$ t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns

OV7930 Light Response

Figure 5 OV7930 Light Response



Register Set

Table 6 provides a list and description of the Device Control registers contained in the OV7930. The device slave addresses are 80 for write and 81 for read.

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control
01	BLUE	80	RW	Blue Channel Gain Control MSB, 8 bits (LSB 2 bits in register BRLOW[1:0] (see "BRLOW" on page 11).
02	RED	80	RW	Red Channel Gain Control MSB, 8 bits (LSB 2 bits in register BRLOW[5:4] (see "BRLOW" on page 11).
03	SAT	80	RW	Saturation Control Bit[7:4]: Saturation adjustment 0000: Lowest 1111: Highest Bit[3:0]: Reserved
04	HUE	10	RW	Hue Adjustment Control Bit[7:6]: Reserved Bit[5]: Hue control ON/OFF 0: OFF 1: ON Bit[4:0]: Hue control setting • Range: -20° to +20° (10000 in the middle)
05	RSVD	XX	–	Reserved
06	BRT	80	RW	Brightness Adjustment Control • Range: [00] to [FF] ***Note:*** *If auto brightness is enabled, this register will be automatically updated by internal control. If auto brightness is disabled, the user can update brightness value.*
07	SHP	D4	RW	Sharpness Adjustment Bit[7:4]: Sharpness ON/OFF threshold Bit[3:0]: Sharpness adjustment
08-09	RSVD	XX	–	Reserved
0A	BRLOW	00	RW	Blue/Red Channel Gain LSBs Bit[7:6]: Reserved Bit[5:4]: Red channel AWB gain two lower bits Bit[3:2]: Reserved Bit[1:0]: Blue channel AWB gain two lower bits
0B-0D	RSVD	XX	–	Reserved
0E	COMB	96	RW	Common Control B Bit[7]: Edge enhancement ON/OFF 0: OFF 1: ON Bit[6:0]: Reserved

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0F	RSVD	XX	–	Reserved
10	VER	01	R	Version number
11	MIDH	7F	R	Manufacturer ID Byte -- High (Read only = 0x7F)
12	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
13	AEC	82	RW	Exposure Control Value • Range: [00] to [82] Tex = (2 x AEC[7:0] + 1) x 63.5 µs
14	COMD	1F	RW	Common Control D Bit[7:6]: AEC/AGC algorithm analyze image area selection 00: Whole image 01: Lower two-thirds image 10: Lower one-half image 11: Lower one-third image Bit[5:3]: Reserved Bit[2]: AGC ON/OFF 0: OFF 1: ON Bit[1]: AWB ON/OFF 0: OFF 1: ON Bit[0]: AEC ON/OFF 0: OFF 1: ON
15	COME	04	RW	Common Control E Bit[7]: SRST 1: Initiates soft reset. All registers are set to default values after which the chip resumes normal operation. Bit[6]: Mirror image selection 0: Normal 1: Output mirror image Bit[5]: Vertical sync option (see "COMG" on page 13 for details) Bit[4]: Backlight exposure mode ON/OFF 0: OFF 1: ON Bit[3]: Reserved Bit[2]: AGC gain ceiling selection - combined with COMJ[3] (see "COMJ" on page 13) as follows: 0: 1x to 4x 1: 1x to 8x/16x Bit[1:0]: Reserved
16	COMF	44	RW	Common Control F Bit[7:3]: Reserved Bit[2]: Banding filter ON/OFF 0: OFF 1: ON Bit[1:0]: Reserved

Table 6 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
17	COMG	95	RW	Common Control G Bit[7]: Fast AGC/AEC algorithm ON/OFF 0: OFF 1: ON Bit[6:5]: Reserved Bit[4]: FODD pin (pin 23 - see "FODD/HGAIN" on page 5) output signal selection - combined with COME[5] (see "COME" on page 12) as follows: COMG[4] COME[5] FODD (pin 23) 0 0 VSYNC every field 0 1 VSYNC every two fields 1 X FODD (odd field flagged) Bit[3:0]: Reserved
18	AECPT	A5	RW	AEC/AGC Luminance Level Control Bit[7:4]: Low level luminance percentage Bit[3:0]: High level luminance percentage ***Note:*** *Stable condition is AECPT[7:4] + AECPT[3:0] > 0x0E.*
19	BKPT	59	RW	AEC/AGC Luminance Level Control in Backlight Mode Bit[7:4]: Low level luminance percentage in backlight mode Bit[3:0]: High level luminance percentage in backlight mode ***Note:*** *Stable condition is BKPT[7:4] + BKPTT[3:0] > 0x0E.*
1A-1C	RSVD	XX	–	Reserved
1D	COMJ	30	RW	Common Control J Bit[7]: Pixel clock polarity selection 0: Normal 1: Revised pixel clock output Bit[6:4]: Reserved Bit[3]: AGC gain ceiling - in effect only if COME[2] = "1" (see "COME" on page 12) 0: 8X 1: 16X Bit[2]: Reserved Bit[1]: NTSC with 50 Hz light compensation. In effect only when COMD[0] = "1" (see "COMD" on page 12) and COMF[2] = "1" (see "COMF" on page 12) Bit[0]: Vertical flip selection 0: Normal 1: Vertical flip output image
1E-20	RSVD	XX	–	Reserved
21	VPT	A4	RW	AEC/AGC Fast mode threshold Bit[7:4]: Fast AEC/AGC low level percentage threshold Bit[3:0]: Fast AEC/AGC high level percentage threshold
22-33	RSVD	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV7930 uses either a 28-pin ceramic package or 28-pin plastic package. Refer to Figure 6 for ceramic package information, Figure 7 for plastic package information, and Figure 8 for the array center on the chip.

Figure 6 OV7930 Ceramic Package Specifications

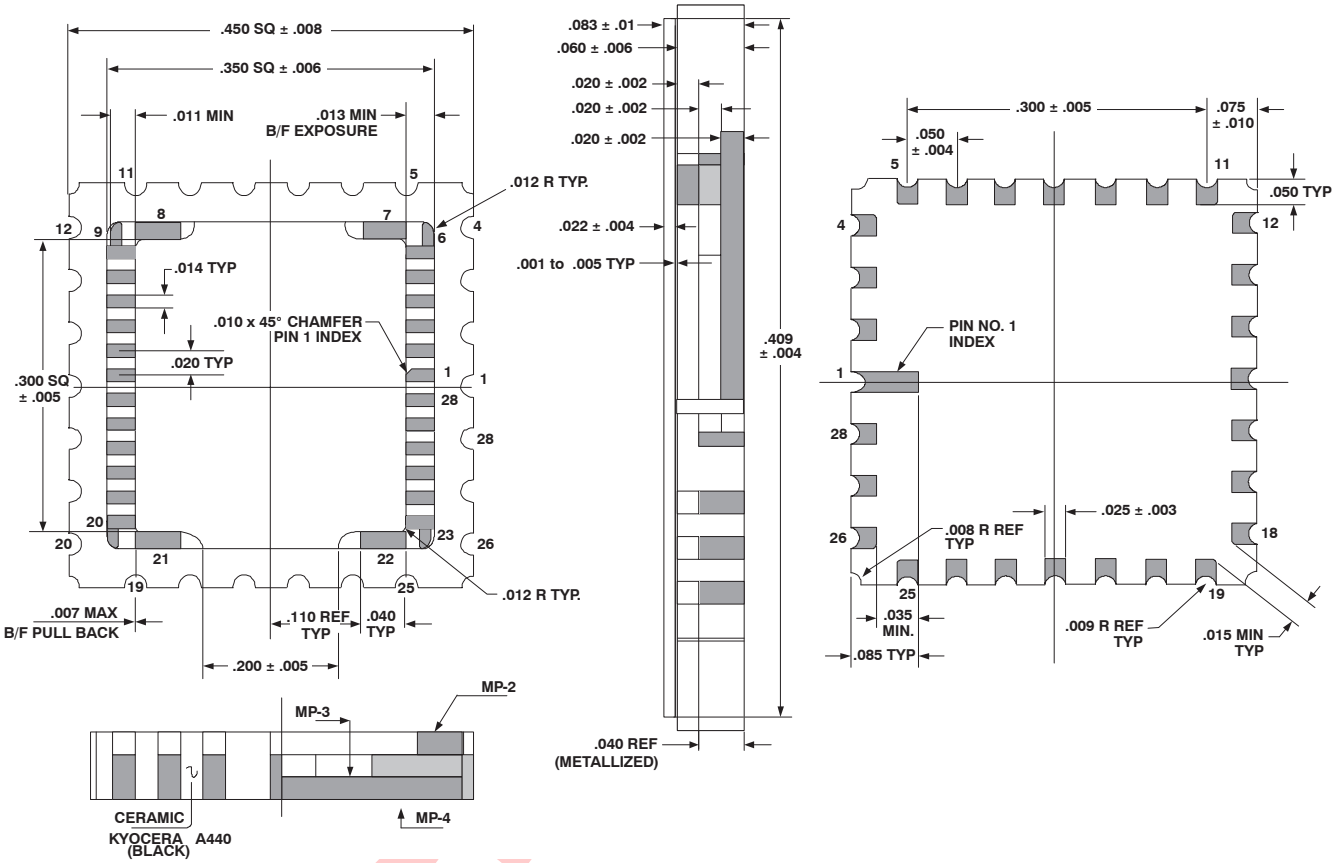


Table 7 OV7930 Ceramic Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	11.43 ± 0.20 SQ	.450 ± .008 SQ
Package Height	2.11 ± 0.25	.083 ± .01
Substrate Height	0.51 ± 0.05	.020 ± .002
Cavity Size	7.62 ± 0.13 SQ	.300 ± .005 SQ
Castellation Height	1.02 ± 0.1	.040 ± .004
Pin #1 Pad Size	0.64 x 2.16	.025 x .085
Pad Size	0.64 x 1.27	.025 x .050
Pad Pitch	1.27 ± 0.10	.050 ± .004
Package Edge to First Lead Center	1.91 ± 0.25	.075 ± .010
End-to-End Pad Center-Center	7.62 ± 0.13	.300 ± .005
Glass Size	10.41 ± 0.10 SQ	.409 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Figure 7 OV7930 Plastic Package Specifications

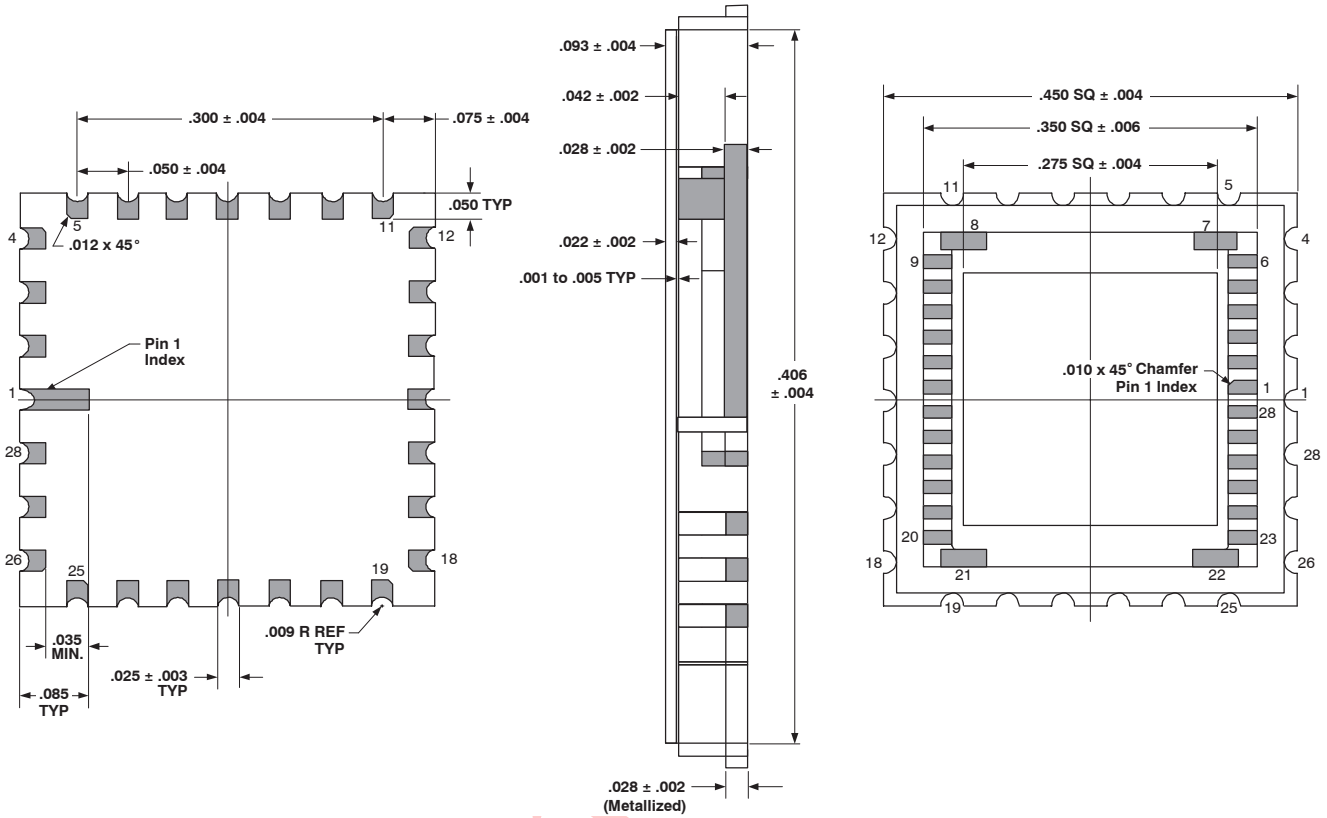
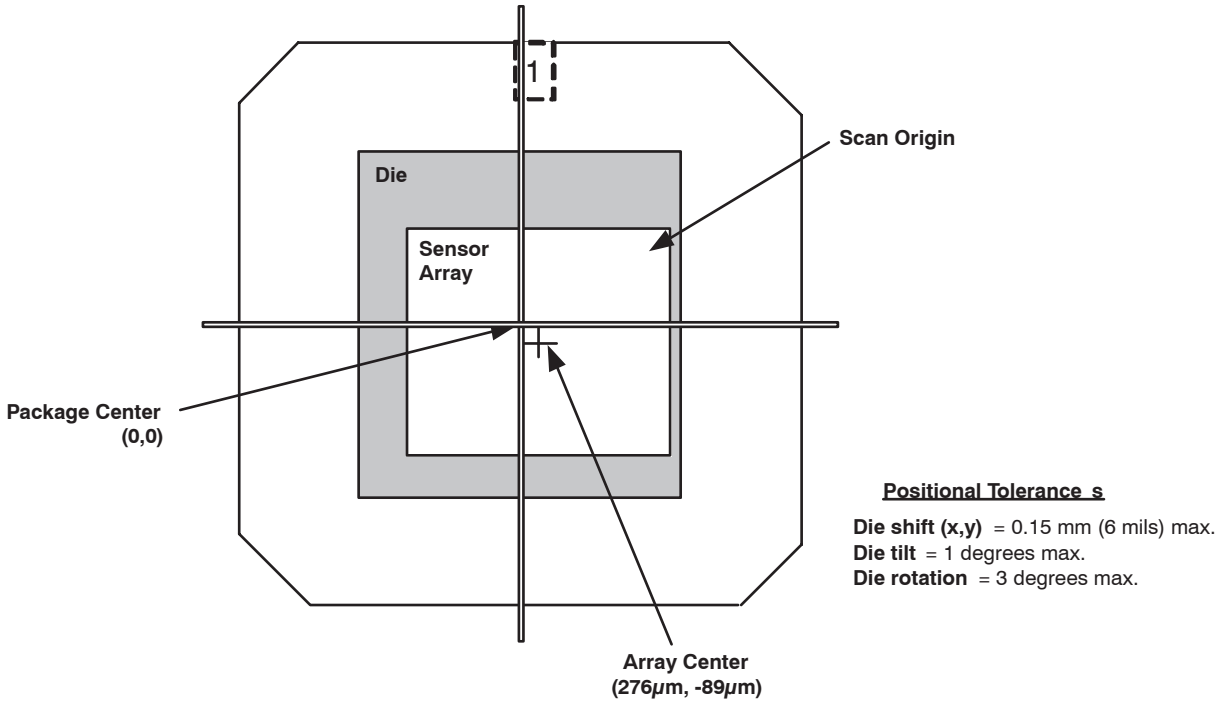


Table 8 OV7930 Plastic Package Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	11.43 ± 0.10 SQ	.450 ± .004 SQ
Package Height	2.35 ± 0.1	.093 ± .004
Substrate Height	0.70 ± 0.05	.028 ± .002
Cavity Size	7.00 ± 0.10 SQ	.275 ± .004 SQ
Castellation Height	1.07 ± 0.05	.042 ± .002
Pin #1 Pad Size	0.64 x 2.16	.025 x .085
Pad Size	0.64 x 1.27	.025 x .050
Pad Pitch	1.27 ± 0.10	.050 ± .004
Package Edge to First Lead Center	1.90 ± 0.10	.075 ± .004
End-to-End Pad Center-Center	7.62 ± 0.10	.300 ± .004
Glass Size	10.30 ± 0.10 SQ	.406 ± .004 SQ
Glass Height	0.55 ± 0.05	.022 ± .002

Sensor Array Center

Figure 8 OV7930 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pin one oriented down on the PCB.

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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