OV7949/OV7449 CMOS NTSC/PAL CAMERACHIP™ Sensor with OmniPixel® Technology for Automotive Applications

General Description

The OV7949 (color) and OV7449 (B&W) single chip CMOS CAMERACHIP™ image sensors are designed to provide a high level of functionality for applications requiring a small footprint, low voltage, low power consumption and high performance color video camera.

The OV7949 supports NTSC/PAL composite video output and can directly interface with a VCR TV monitor or other device with 75 ohm loading.

Note: The OV7949 is available in a lead-free package.

Features

- Single chip 1/3" format video camera
- Composite video (NTSC/PAL) differential output drive
- Sensitivity boost (+42 dB)
- Automatic exposure/gain with 16 zone control
- Auto white balance control
- Aperture/Gamma correction
- 50/60 Hz flicker cancellation
- External frame sync capability
- SPI/EEPROM used to control overlay and set other customer variables
- I2C compatible Serial Camera Control Bus (SCCB) control interface for register programming
- Low power consumption
- Extremely low dark current for high temperature applications
- Defective pixel correction
- Genlock
- QFP parts qualified to AEC-Q100 standard

Ordering Information

Product	Package
OV07949-Q10V (Color, NTSC)	QFP-48
OV07449-Q10V (B&W, NTSC)	QFP-48
OV07949-Q20V (Color, PAL)	QFP-48
OV07449-Q20V (B&W, PAL)	QFP-48

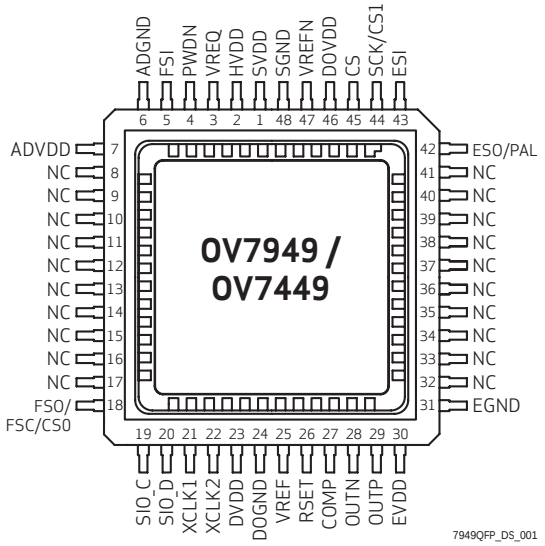
Applications

- Automobile applications
  - Occupant sensor
  - Adaptive cruise control
  - Rear view / backup camera
  - Lane departure warning
  - Blind spot detection
  - Night vision

Key Specifications

Array Size	**PAL**	628 x 586
	NTSC	510 x 496
Power Supply	**Analog/ADC/IO**	3.3 VDC ± 5%
	Digital Core	1.8 VDC ± 5%
Power Consumption		168 mW (DVDD=1.8V, all other voltages=3.3V, 75Ω loading)
Image Area		5.961 mm x 4.276 mm
Exposure Time Range		1/60s - 12 µs (NTSC) 1/50s - 12.5 µs (PAL)
Sensitivity		4.7 V/Lux-sec @ 5600K
S/N Ratio		48 dB
Dynamic Range		50 dB
Pixel Size		9.2 µm x 7.2 µm
Dark Current		10 mW/s @ 60°C
Fixed Pattern Noise		0.079% of $V_{PEAK-TO-PEAK}$
Package Dimensions		14.22 mm x 14.22 mm

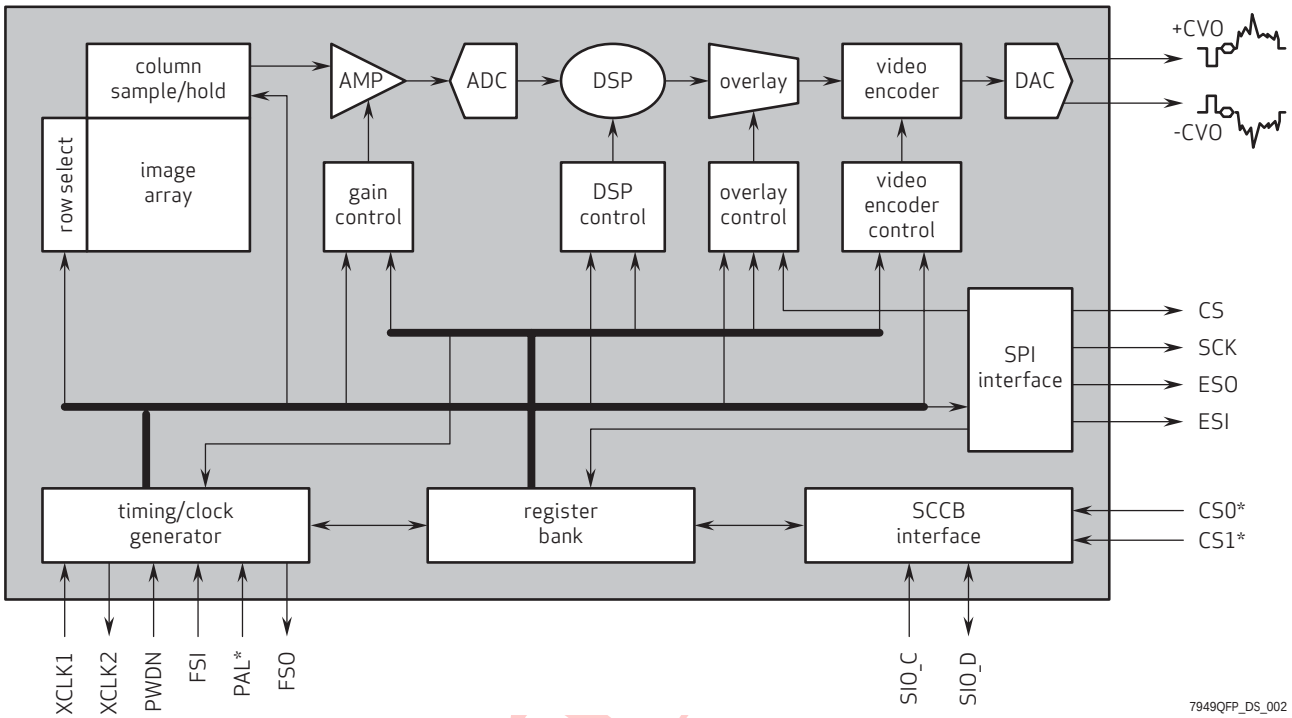
Figure 1 OV7949/OV7449 Pin Diagram (Top View)



Functional Description

This section describes the various functions of the OV7949. Refer to Figure 2 for the functional block diagram of the OV7949.

Figure 2 Functional Block Diagram



Video Standards

PAL/NTSC TV standards are implemented and available as output in the OV7949/OV7449 CAMERACHIP sensor. Note that the accuracy and stability of the crystal clock frequency is important to avoid unwanted color shift in the TV video system. OmniVision recommends using a 17.73448MHz (for PAL) or 14.31818MHz (for NTSC) crystal when utilizing the OV7949/OV7449 CAMERACHIP sensor.

Video Format

The OV7949/OV7449 CAMERACHIP sensor supports Composite (CVBS) video format only. Composite signals are generated from the built-in TV encoder.

Image Sensor Functions

White Balance

The function of white balance in the OV7949/OV7449 CAMERACHIP sensor is to adjust and calibrate the image device sensitivity on the primary (RGB) colors to match the color cast of the light source. The Auto White Balance (AWB) can be enabled or disabled by register control. If the AWB is enabled, the image sensors continuously perform white balancing.

Mirror and Vertical Flip

The OV7949/OV7449 provides horizontal mirror and vertical flip functions. These functions can be turned ON or OFF via register settings.

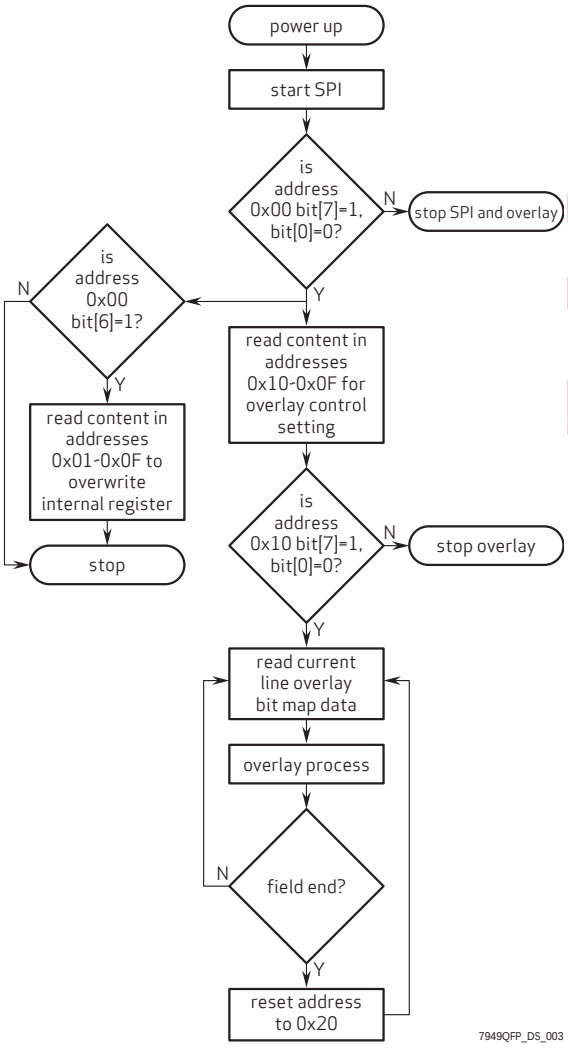
Overlay Control

The OV7949/OV7449 CAMERACHIP sensor has an overlay capability where the user can store an overlay bit map image in an external storage device with an SPI interface.

At power up, OV7949/OV7449 will start the SPI interface automatically. A “0” in the first address bit 7 indicates that there is no SPI slave device attached, causing the SPI interface to stop. Otherwise, the OV7949/OV7449 will check bit 6 of first byte for overwrite control. The user can define up to 15 bytes in the control register to overwrite the internal default value (further detail defining this register is not available at this time). These 15 bytes are only read one time after power up.

If the first byte bit[7] is “1” and bit[0] is “0”, OV7949/OV7449 will read the content in address 0x10 to 0x1F for the overlay setting.

Figure 3 SPI Overlay Process Sequence



Data formats are defined as follows:

EEPROM Address	Description
0x00	SPI Enable Bit[7], [0]: SPI enable 00: No SPI 01: No SPI 10: SPI enabled 11: No SPI Bit[6]: Register settings replacement enable 0: Register replacement disabled (0x01 to 0x0F not used) 1: Addresses 0x01 to 0x0F are used to replace certain register settings. Settings from these addresses are fixed and no longer accessible by SCCB.
0x01 - 0x0F	Used for register replacement settings (see Table 1 for corresponding SCCB register addresses.
0x10	Overlay Common Setting Bit[7], [0]: Overlay ON/OFF selection 0x: OFF 10: ON 11: OFF Bit[6:5]: Overlay opacity setting 00: 25% 01: 50% 10: 75% 11: 100% Bit[4:3]: Resolution selection 00: 2x2 01: 3x3 10: 4x4 11: 5x5 Bit[2]: Overwrite option 0: $Y = r\% \times Y_{ovly} + (1 - r\%)Y_{ori}$ $U = r\% \times U_{ovly} + (1 - r\%)U_{ori}$ $V = r\% \times V_{ovly} + (1 - r\%)V_{ori}$ 1: $Y = r\% \times Y_{ovly} + (1 - r\%)Y_{ori}$ $U = U_{ovly}$ $V = V_{ovly}$
	Note: *r% = Overlay opacity (register bits[6:5] shown above)* *Y_{ovly} = Y Overlay Value (0x11)* *U_{ovly} = Y Overlay Value (0x12)* *V_{ovly} = Y Overlay Value (0x13)* *Y_{ori} = Original Y data* *U_{ori} = Original U data* *V_{ori} = Original V data*
0x11	Y Overlay Value
0x12	U Overlay Value
0x13	V Overlay Value
0x14	Overlay Start Line Address MSBs
0x15	Overlay End Line Address MSBs
0x16	Overlay Start Column Address MSBs
0x17	Overlay End Column Address MSBs
0x18	Overlay Window LSBs Bit[7:6]: Start line LSB Bit[5:4]: End line LSB Bit[3:2]: Start column LSBs Bit[1:0]: End column LSBs
0x19	MemLine - this register determines how many bytes of the Bit Map file in EEPROM are required to draw a line
0x1A - 0x1F	Reserved

Note: Bit map file starts from address 0x20

Table 1 EEPROM Registers and Corresponding Sensor Device Registers

Address (Hex)	Function/Description	Address (Hex)	Function/Description	Address (Hex)	Function/Description
0x01	Bit[7]: COMA[7] (0x04) Bit[6]: COMA[6] (0x04) Bit[5]: COMA[4] (0x04) Bit[4]: COMA[3] (0x04) Bit[3]: COMB[0] (0x0E) Bit[2]: COMI[7] (0x31) Bit[1]: COMI[6] (0x31) Bit[0]: ENC6[0] (0xAB)	0x06	Bit[7]: AEW[7] (0x24) Bit[6]: AEW[6] (0x24) Bit[5]: AEW[5] (0x24) Bit[4]: AEW[4] (0x24) Bit[3]: AEW[3] (0x24) Bit[2]: AEW[2] (0x24) Bit[1]: AEW[1] (0x24) Bit[0]: AEW[0] (0x24)	0x0B	Bit[7]: COMJ[3] (0x3C) Bit[6]: COMJ[2] (0x3C) Bit[5]: COMJ[1] (0x3C) Bit[4]: COMJ[0] (0x3C) Bit[3]: SHP2[7] (0x8D) Bit[2]: SHP2[6] (0x8D) Bit[1]: SHP2[5] (0x8D) Bit[0]: SHP2[4] (0x8D)
0x02	Bit[7]: SYSC[7] (0x12) Bit[6]: SYSC[6] (0x12) Bit[5]: SYSC[1] (0x12) Bit[4]: SYSC[0] (0x12) Bit[3]: COME[1] (0x15) Bit[2]: COMG[6] (0x2C) Bit[1]: COMG[1] (0x2C) Bit[0]: COMG[0] (0x2C)	0x07	Bit[7]: AEB[7] (0x25) Bit[6]: AEB[6] (0x25) Bit[5]: AEB[5] (0x25) Bit[4]: AEB[4] (0x25) Bit[3]: AEB[3] (0x25) Bit[2]: AEB[2] (0x25) Bit[1]: AEB[1] (0x25) Bit[0]: AEB[0] (0x25)	0x0C	Bit[7]: SHP1[7] (0x8C) Bit[6]: SHP1[6] (0x8C) Bit[5]: SHP3[7] (0x8E) Bit[4]: SHP3[6] (0x8E) Bit[3]: SHP3[5] (0x8E) Bit[2]: SHP3[4] (0x8E) Bit[1]: SHP3[3] (0x8E) Bit[0]: SHP3[2] (0x8E)
0x03	Bit[7]: AUTO[7] (0x13) Bit[6]: AUTO[6] (0x13) Bit[5]: AUTO[5] (0x13) Bit[4]: AUTO[3] (0x13) Bit[3]: AUTO[2] (0x13) Bit[2]: AUTO[1] (0x13) Bit[1]: AUTO[0] (0x13) Bit[0]: COMF[7] (0x16)	0x08	Bit[7]: VV[7] (0x26) Bit[6]: VV[6] (0x26) Bit[5]: VV[5] (0x26) Bit[4]: VV[4] (0x26) Bit[3]: VV[3] (0x26) Bit[2]: VV[2] (0x26) Bit[1]: VV[1] (0x26) Bit[0]: VV[0] (0x26)	0x0D	Bit[7]: BRT[7] (0x97) Bit[6]: BRT[6] (0x97) Bit[5]: BRT[5] (0x97) Bit[4]: BRT[4] (0x97) Bit[3]: BRT[3] (0x97) Bit[2]: BRT[2] (0x97) Bit[1]: BRT[1] (0x97) Bit[0]: BRT[0] (0x97)
0x04	Bit[7]: COMD[7] (0x14) Bit[6]: COMD[6] (0x14) Bit[5]: COMD[5] (0x14) Bit[4]: COMD[4] (0x14) Bit[3]: Not used Bit[2]: Not used Bit[1]: Not used Bit[0]: Not used	0x09	Bit[7]: AVGSL[7] (0x2D) Bit[6]: AVGSL[6] (0x2D) Bit[5]: AVGSL[5] (0x2D) Bit[4]: AVGSL[4] (0x2D) Bit[3]: AVGSL[3] (0x2D) Bit[2]: AVGSL[2] (0x2D) Bit[1]: AVGSL[1] (0x2D) Bit[0]: AVGSL[0] (0x2D)	0x0E	Bit[7]: CNTR1[7] (0x98) Bit[6]: CNTR1[6] (0x98) Bit[5]: CNTR1[5] (0x98) Bit[4]: CNTR1[4] (0x98) Bit[3]: CNTR1[3] (0x98) Bit[2]: CNTR1[2] (0x98) Bit[1]: CNTR1[1] (0x98) Bit[0]: CNTR1[0] (0x98)
0x05	Bit[7]: VWSFT[7] (0x19) Bit[6]: VWSFT[6] (0x19) Bit[5]: VWSFT[5] (0x19) Bit[4]: VWSFT[4] (0x19) Bit[3]: VWSFT[3] (0x19) Bit[2]: VWSFT[2] (0x19) Bit[1]: VWSFT[1] (0x19) Bit[0]: VWSFT[0] (0x19)	0x0A	Bit[7]: AVGSH[7] (0x2E) Bit[6]: AVGSH[6] (0x2E) Bit[5]: AVGSH[5] (0x2E) Bit[4]: AVGSH[4] (0x2E) Bit[3]: AVGSH[3] (0x2E) Bit[2]: AVGSH[2] (0x2E) Bit[1]: AVGSH[1] (0x2E) Bit[0]: AVGSH[0] (0x2E)	0x0F	Bit[7]: OHSFT[7] (0xBC) Bit[6]: OHSFT[6] (0xBC) Bit[5]: OHSFT[5] (0xBC) Bit[4]: OHSFT[4] (0xBC) Bit[3]: OHSFT[3] (0xBC) Bit[2]: OHSFT[2] (0xBC) Bit[1]: OHSFT[1] (0xBC) Bit[0]: OHSFT[0] (0xBC)

Bit Map File

The bit map file starts from address 0x20 where each bit that equals '0' indicates no overlay bit marked and each bit that equals '1' indicates an overlay bit is marked.

Byte[19]

Every time a new line is started, we need to go to a new address for memory reading. For example, if the user specifies 500 pixels per line, which is not an exact multiple of 8, they need at least 63 bytes (63 x 8 = 504) to save the information. So, they can only specify MemLine[7:0] to be a number greater than or equal to [3F].

For example, if you want 500 pixels per line and if MemLine = [40], use hex address [20] to [5E].

Line 1 start address = [20], and the reading sequence as follows:

Byte[20]bit7, bit6, bit5, bit4, bit3, bit2, bit1, bit0,
Byte[21]bit7, bit6, bit5, bit4, bit3, bit2, bit1, bit0,
Byte[22]bit7, bit6, ...
Byte[5E]bit7, bit6, bit5, bit4 END

Line 2 start address = [60] and it reads through address [9E], the reading sequence as follows:

Reading sequence:

Byte[60]bit7, bit6, bit5, bit4, bit3, bit2, bit1, bit0,
Byte[61]bit7, bit6, bit5, bit4, bit3, bit2, bit1, bit0,
Byte[62]bit7, bit6, ...
Byte[9E]bit7, bit6, bit5, bit4 END

So, in each line, 500 bits are read.

Byte[18:14]

The user can specify the vertical and horizontal dimensions of the overlay bitmap. If the desired figure is very small compared to the dimensions of the whole screen, the user can save a lot of memory.

Byte[13:11]

Y, U, V specifies overlay color.

Byte[10]

When choosing 3x3 or 5x5 resolution, be aware that because the YUV sampling format is 4:2:2, there may be strong color aliasing around overlay edge.

Multi-Chip Synchronize

The OV7949/OV7449 CAMERACHIP sensor provides the multi-chip Synchronize function where one chip works as the master and all others as slave devices. The master chip provides the frame synchronize signal through pin FSO. All slave devices then accept the frame synchronize signal through pin FSI. This mode allows all devices to synchronize together.

Chip Configuration

The OV7949/OV7449 CAMERACHIP sensor has been designed for ease-of-use in many stand-alone applications. Some functions like serial interface slave address (pins CS0 and CS1) and PAL/NTSC (pin ESO/PAL) selection can be set by connecting appropriate pins high (logic "1") or low (logic "0") through a 10 KΩ resistor. The OV7949/OV7449 CAMERACHIP sensor also has a serial slave interface for programmable access to all register functions.

Additional Picture Controls

The OV7949/OV7449 CAMERACHIP sensor provides additional picture control functions to enhance image quality and chip performance. These functions are listed as follows:

- AGC gain range control
- Gamma correction
- Brightness
- Contrast
- Full color bar test pattern

Serial Camera Control Bus (SCCB)

Many of the functions and configuration registers in the OV7949/OV7449 image sensors are available through the SCCB interface. The OV7949/OV7449 image sensor operates as a slave device that supports up to 400 kbps serial transfer rate using a 7-bit address/data transfer protocol.

SCCB Protocol Format

In SCCB operation (see Figure 6), the master must perform the following operations:

- Generate the Start/Stop condition
- Provide the serial clock on SIO_C
- Place the 7-bit slave address (RW bit) and the 8-bit sub-address on SIO_D

The receiver must pull down SIO_D during the acknowledgement bit time. During the write cycle, the OV7949/OV7449 device returns the acknowledgement and, during the read cycle, the master returns the acknowledgement, indicating to the slave that the read cycle can be terminated. Note that the restart feature is not supported here.

Within each byte, the MSB is transferred first. The read/write control bit is the LSB of the first byte. Standard SCCB communications require only two pins, SIO_C and SIO_D. SIO_D is configured as an open drain for bidirectional purposes. A HIGH to LOW transition on the SIO_D while SIO_C is HIGH indicates a START condition. A LOW to HIGH transition on the SIO_D while SIO_C is HIGH indicates a STOP condition. Only a master can generate START/STOP conditions.

Except for these two special conditions, the protocol that SIO_D remain stable during the HIGH period of the clock, SIO_C. Each bit is allowed to change state only when SIO_C is LOW (see Figure 4 and Figure 5).

The OV7949/OV7449 SCCB interface supports multi-byte write and multi-byte read. The master must supply the sub-address in the write cycle, but not in the read cycle. Therefore, the OV7949/OV7449 takes the read sub-address from the previous write cycle. In multi-byte write or multi-byte read cycles, the sub-address automatically increments after the first data byte so that continuous locations can be accessed in one bus cycle. A multi-byte cycle overwrites its original sub-address; therefore, if a read cycle immediately follows a multi-byte cycle, a single byte write cycle that provides a new address must be inserted.

The OV7949/OV7449 supports a single slave ID. The ID is preset to 60 for write and 61 for read.

In the write cycle, the second byte in the SCCB is the sub-address for selecting the individual on-chip registers, and the third byte is the data associated with this register. Writing to the unimplemented sub-address is ignored.

In the read cycle, the second byte is the data associated with the previously stored sub-address. Reading of an unimplemented sub-address returns unknown.

Figure 4 Bit Transfer on the SCCB

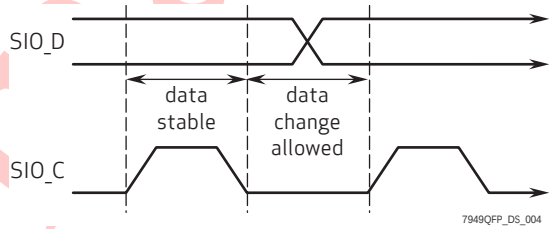


Figure 5 Data Transfer on the SCCB

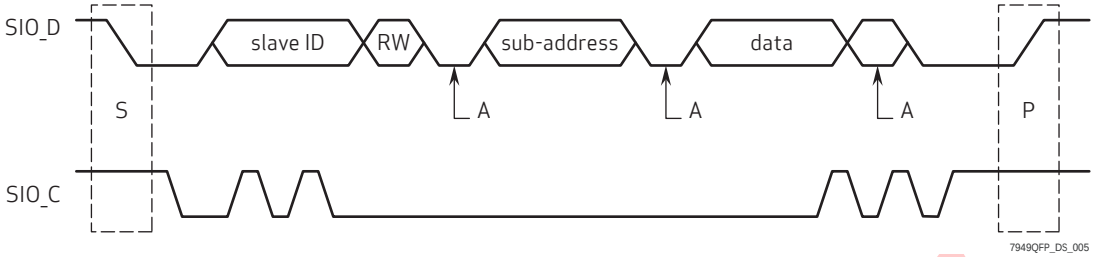
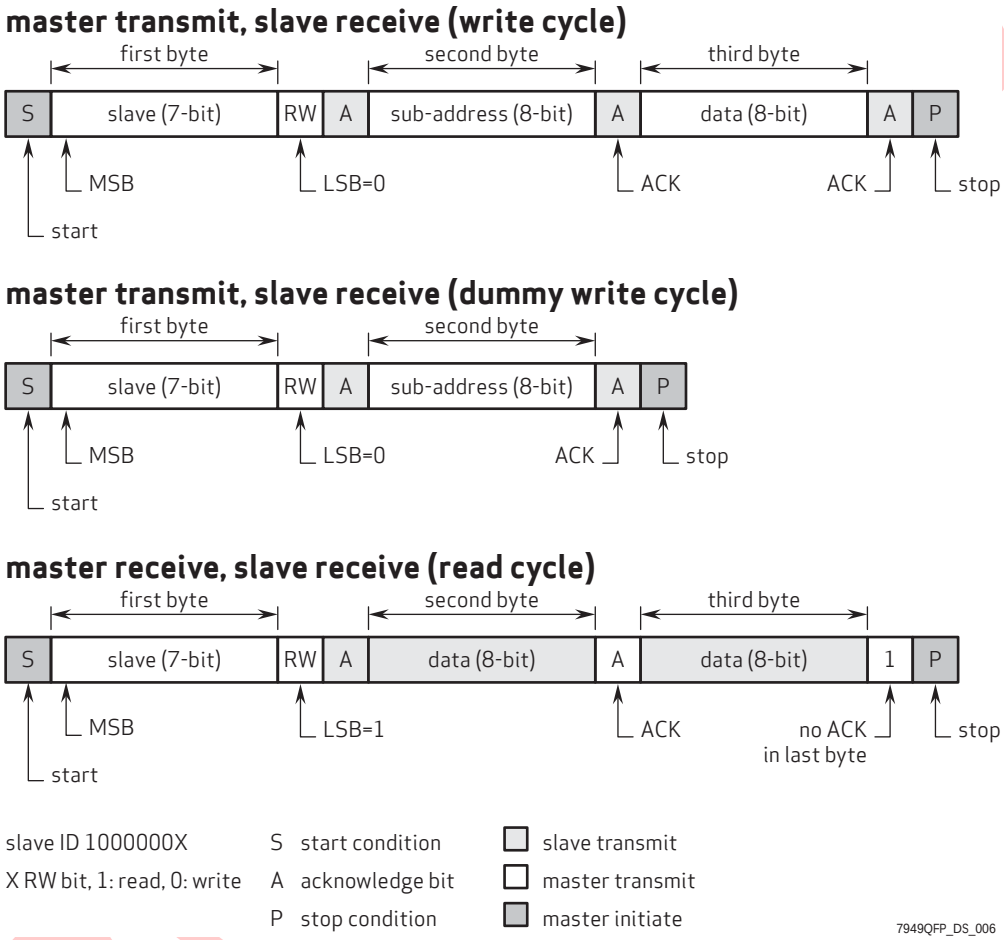


Figure 6 SCCB Protocol Format



Pin Description

Table 2 Pin Description

Pin Location	Name	Pin Type	Default (V)	Function/Description
01	SVDD	Power	3.3	Sensor power supply - connect to VREQ using a 0.1 µF capacitor
02	HVDD	Analog	—	Internal reference - connect to SGND using a 1 µF capacitor
03	VREQ	Analog	—	Internal reference - connect to ground using a 0.1 µF capacitor
04	PWDN	Input	0	Power Down Mode ON/OFF Selection 0: OFF 1: ON
05	FSI	Input	0	Frame sync signal input
06	ADGND	Power	0	ADC ground
07	ADVDD	Power	3.3	ADC power supply
08-17	NC	—	—	No connection
18	FSO/FSC/ CS0	I/O	0	Frame synchronizing signal or sub carrier clock output. Also can be programmed to output sub carrier clock. Also can be power on latch as serial interface slave address bit 0.
19	SIO_C	Input	—	Serial interface clock input
20	SIO_D	I/O	—	Serial interface data I/O
21	XCLK1	Input	—	Crystal input
22	XCLK2	Output	—	Crystal output
23	DVDD	Power	1.8	Digital core power supply
24	DOGND	Power	0	Digital I/O interface ground
25	VREF	Analog	—	Internal reference - connect to ground using a 0.01 µF (MLCC) capacitor
26	RSET	Analog	—	DAC reference - connect to ground using a 330Ω resistor
27	COMP	Analog	—	Internal reference - connect to SVDD using a 0.01 µF (MLCC) capacitor and 10 µF (TRAM) capacitor in parallel
28	OUTN	Output	—	Differential negative output
29	OUTP	Output	—	Differential positive output
30	EVDD	Power	3.3	DAC power supply
31	EGND	Power	0	DAC ground
32-41	NC	—	—	No connection
42	ESO/PAL	I/O	0	SPI interface data output. Power on latch as PAL/NTSC select. 0: NTSC 1: PAL
43	ESI	Input	0	SPI interface data input
44	SCK/CS1	I/O	0	SPI interface clock output. Also can be power on latch as Serial interface slave address bit 1.
45	CS	Output	—	SPI interface chip select signal
46	DOVDD	Power	3.3	Digital I/O interface power supply
47	VREFN	Analog	—	Internal reference - connect to ground using a 1 µF capacitor
48	SGND	Power	0	Sensor array ground

Electrical Characteristics

Table 3 Operating Conditions

Parameter	Min	Max
Operating temperature	-40°C	+85°C
Storage temperature[a]	-40°C	+125°C

a. Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.

Table 4 DC Characteristics (-20°C < T_A < 85°C, Voltages Referenced to GND)

Symbol	Parameter	Min	Typ	Max	Unit
Supply					
VDD1	Supply voltage (SVDD, DOVDD, EVDD)	3.15	3.3	3.45	V
VDD2	Supply voltage (DVDD)	1.70	1.8	1.90	V
IDD	Supply current	–	50	–	mA
Digital Inputs					
V_{IL}	Input voltage LOW			0.2 x DOVDD	V
V_{IH}	Input voltage HIGH	0.8 x DOVDD			V
C_{IN}	Input capacitor			10	pF
Digital Outputs (standard loading 25 pF, 1.2 KΩ to 3V					
V_{OH}	Output voltage HIGH	2			V
V_{OL}	Output voltage LOW			0.6	V
Serial Input					
V_{IL}	SIO_C and SIO_D	-0.5	0	1	V
V_{IH}	SIO_C and SIO_D	2.5	3.3	V_{DOVDD} + 0.5	V

Table 5 AC Characteristics (T_A = 25°C, VDD = 5V)

Symbol	Parameter	Min	Typ	Max	Unit
Clock Input / Crystal Oscillator					
f_{OSC}	Resonator frequency (NTSC)	–	14.31818	–	MHz
	Resonator frequency (PAL)	–	17.73448	–	MHz
	Load capacitor		33		pF
	Parallel resistance		1		MΩ
	Rise/fall time for external clock input	–	5	–	ns
	Duty cycle for external clock input	40	50	60	%
CVO Analog Video Output Parameters					
V_{TO_P}	Video peak signal level	0.969	1.020	1.071	V
V_{TO_B}	Video black signal level	0.339	0.357	0.375	V
V_{VSYNC}	Video sync pulse amplitude	0.291	0.306	0.321	V
$V_{SYNCLEVEL}$	Sync level	0.017	0.022	0.027	V
I_{VTO}	Video output drive current	–		30	mA
I/O Pin					
I_{SOURCE}	Output pin source current (output = 1.5V)	8	10	12	mA
I_{SINK}	Output pin sink current (output = 3V)	8	10	12	mA
Miscellaneous Timing					
t_{SYNC}	External FSI cycle time	–	2	–	field
t_{PU}	Chip power-up time	–	–	100	µs

Timing Specifications

NTSC Timing

Figure 7 NTSC Standard Video Timing Diagram

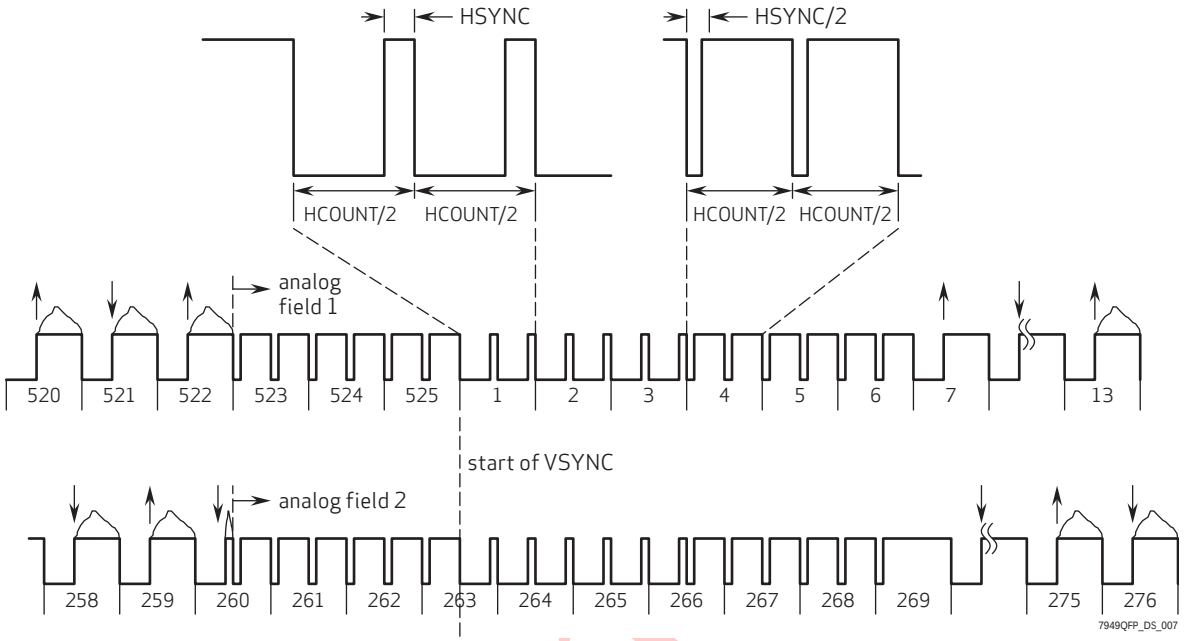
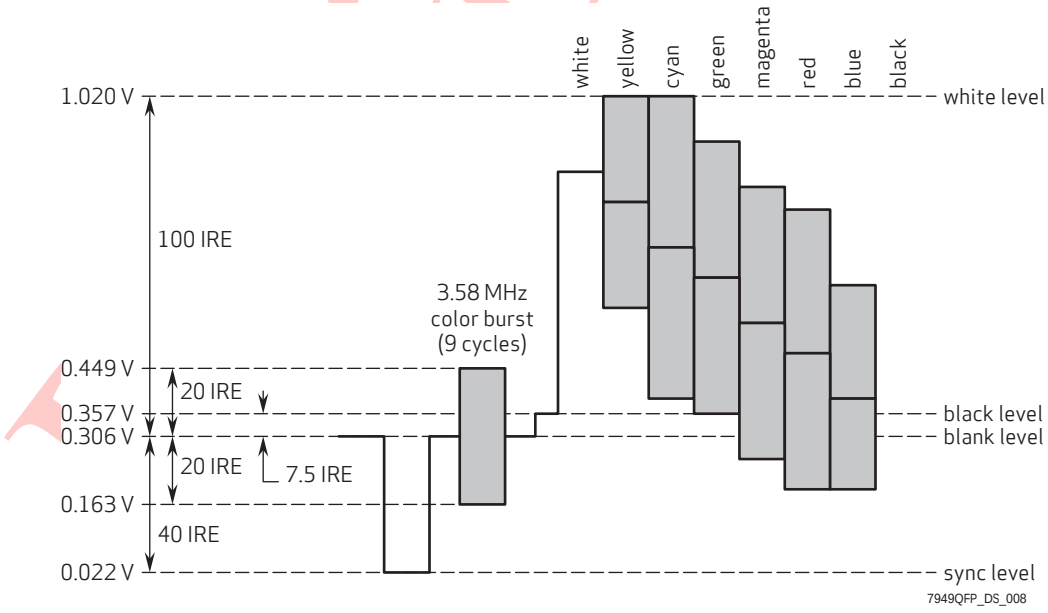


Figure 8 NTSC Composite Video Signal



PAL Timing

Figure 9 PAL Standard Video Timing Diagram

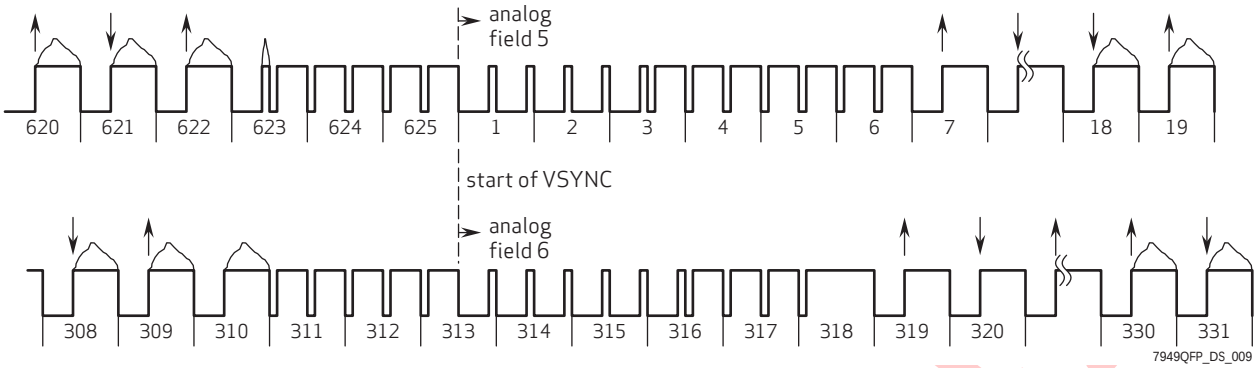
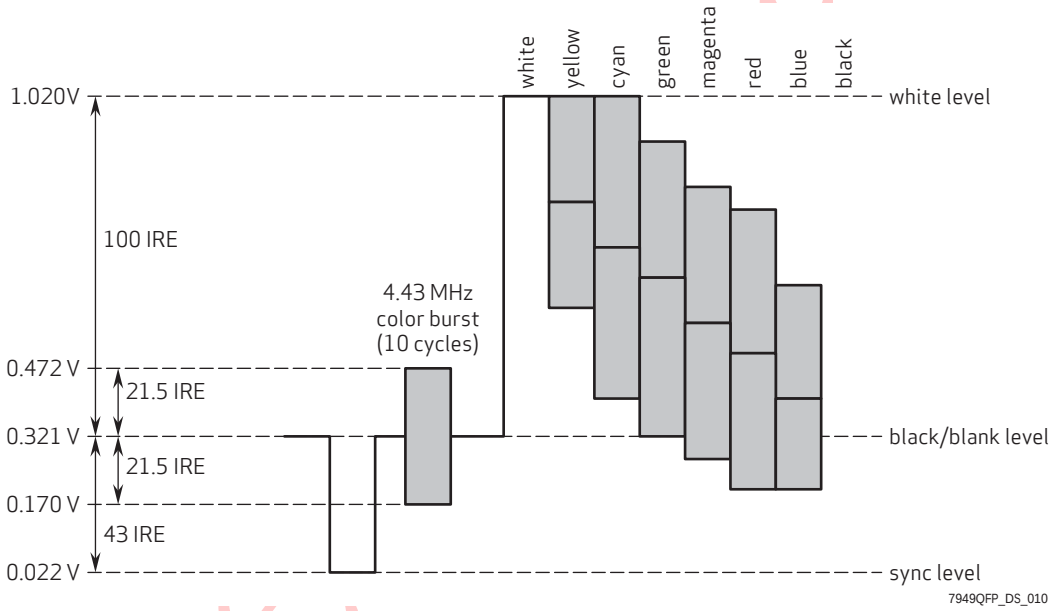


Figure 10 PAL Composite Video Signal



Overlay Timing

Figure 11 Vertical Timing Diagram

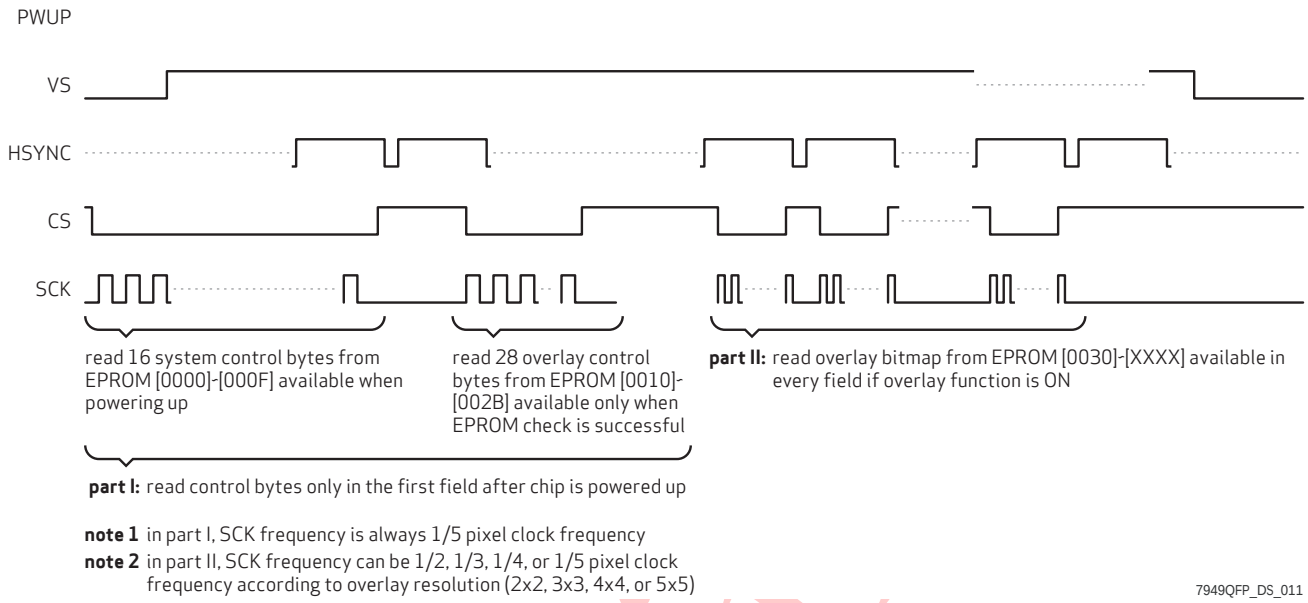
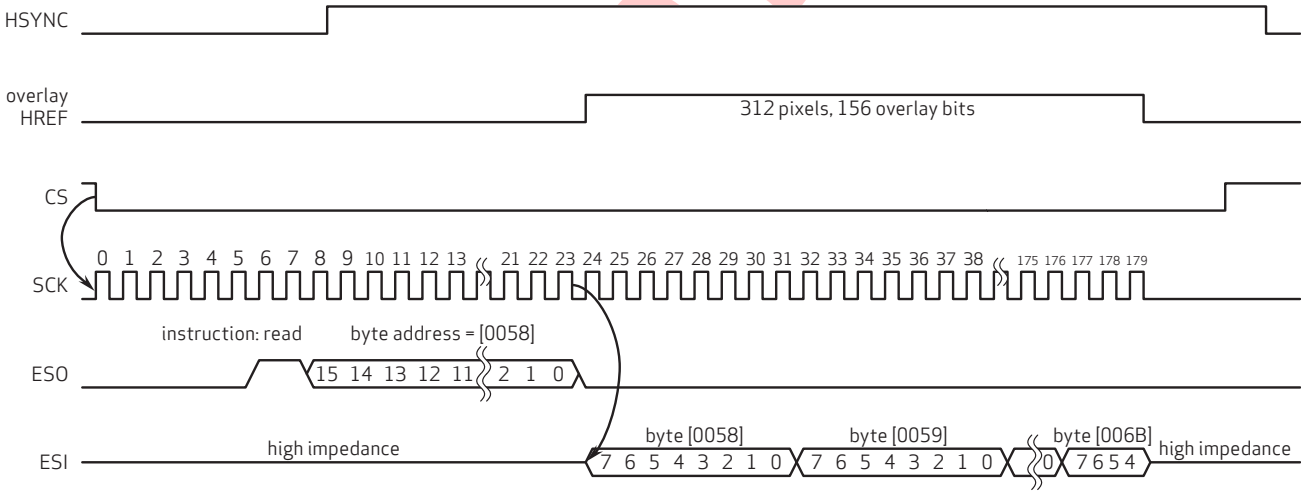


Figure 12 Horizontal Timing Diagram



Interface Timing

Figure 13 SCCB Timing Diagram

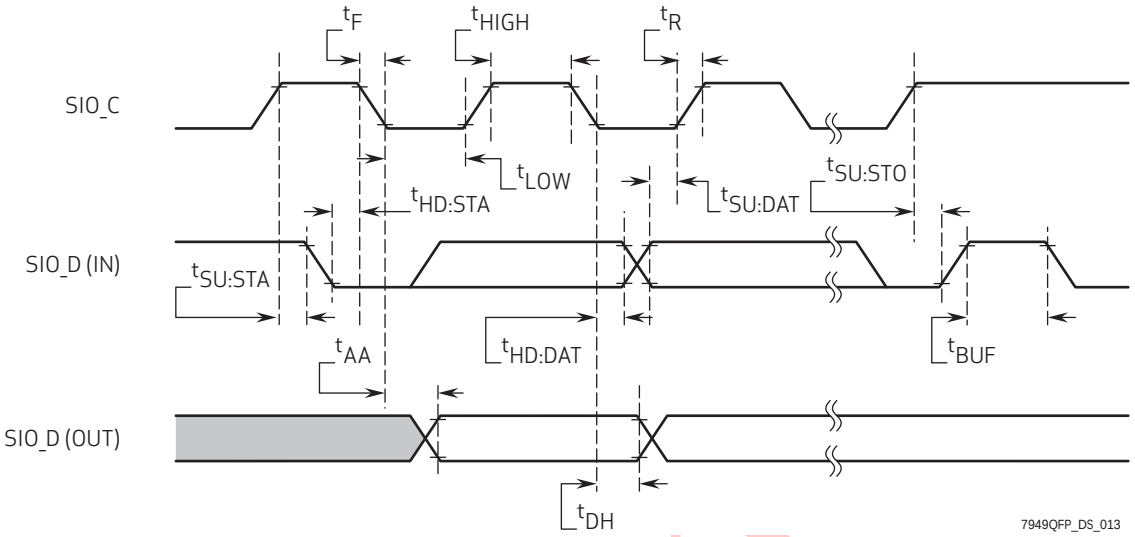


Table 6 SCCB Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
f_{SIO_C}	Clock frequency			400	KHz
t_{LOW}	Clock low period	1.3			µs
t_{HIGH}	Clock high period	600			ns
t_{AA}	SIO_C low to data out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition hold time	600			ns
$t_{SU:STA}$	START condition setup time	600			ns
$t_{HD:DAT}$	Data in hold time	0			µs
$t_{SU:DAT}$	Data in setup time	100			ns
$t_{SU:STO}$	STOP condition setup time	600			ns
$t_{R,}$ t_F	SCCB rise/fall times			300	ns
t_{DH}	Data out hold time	50			ns

Figure 14 SPI Timing Diagram

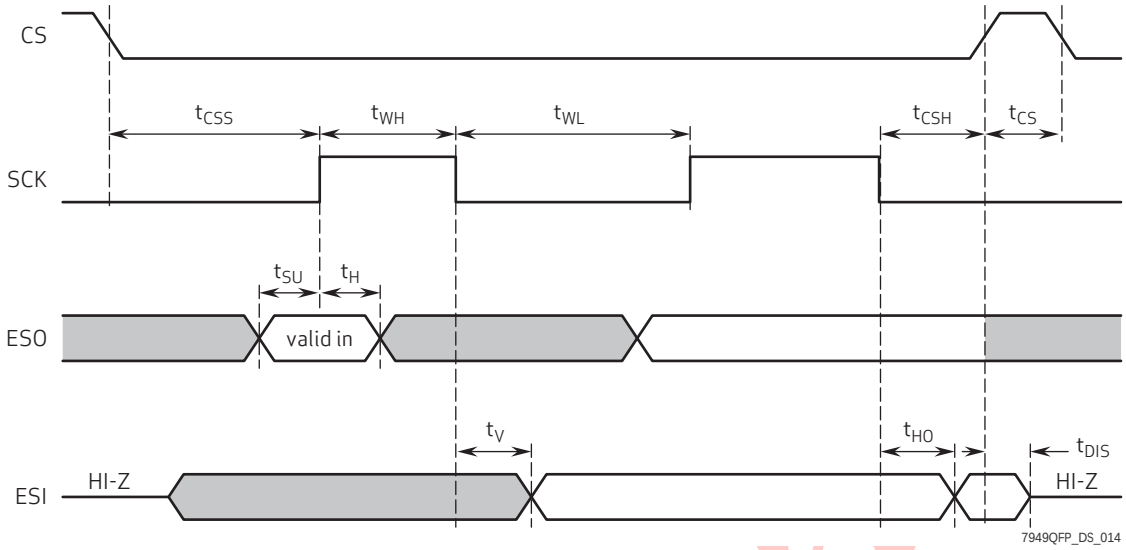
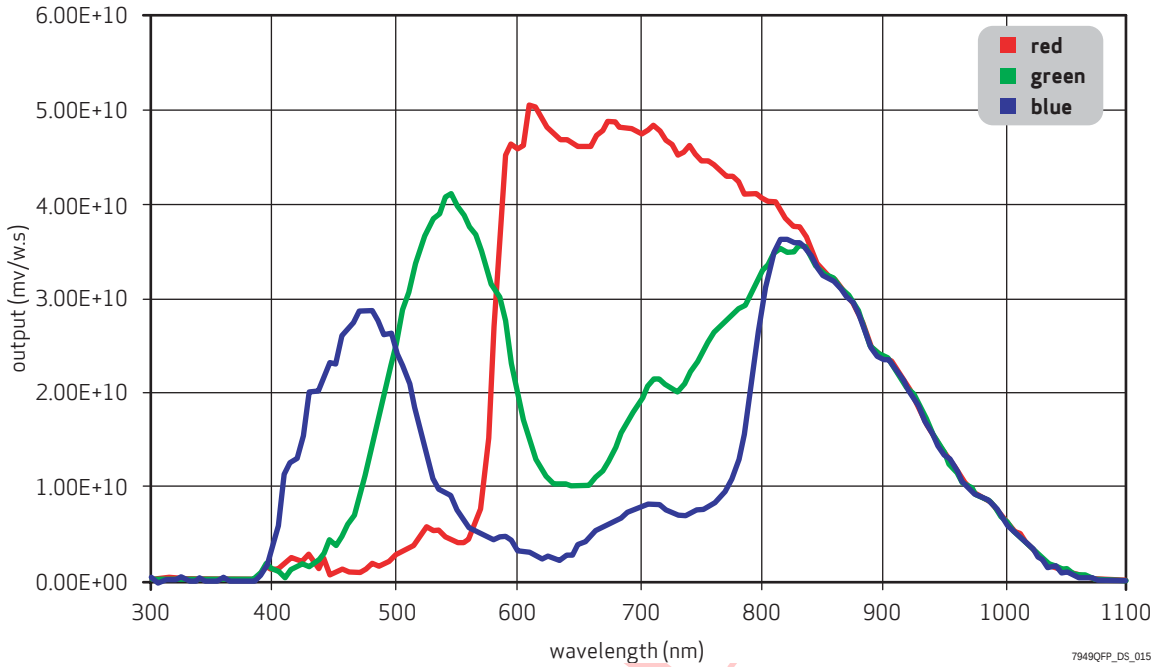


Table 7 SPI Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_{WH}	SCK high time	133			ns
t_{WL}	SCK low time	133			ns
t_{CS}	CS high time	250			ns
t_{CSS}	CS setup time	250			ns
t_{CSH}	CS hold time	250			ns
t_{SU}	Data In setup time	50			ns
t_{H}	data in hold time	50			ns
t_{V}	Output valid			133	ns
t_{HO}	Output hold time	0			ns
t_{DIS}	Output disable time			250	ns

OV7949/OV7449 Light Response

Figure 15 OV7949/OV7449 Light Response



Register Set

Table 8 provides a list and description of the Device Control registers contained in the OV7949/OV7449. The device slave addresses are 60 for write and 61 for read.

Table 8 Device Control Register List (Sheet 1 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC Gain Control Bit[7:0]: Gain setting • Range: 1x - 32x Gain = (Bit[7]+1) x (Bit[6]+1) x (Bit[5]+1) x (Bit[4]+1) x (1+Bit[3:0]/16) ***Note:*** *This register is updated automatically when AGC is enabled. The user can adjust the value through the serial interface if AGC is disabled.*
01	BLUE	80	RW	Blue Gain Control • Range: [00] to [FF] (0 - 2x)
02	RED	80	RW	Red Gain Control • Range: [00] to [FF] (0 - 2x)
03	GREEN	80	RW	Green Gain Control • Range: [00] to [FF] (0 - 2x)
04	COMA	08	RW	Common Control A Bit[7]: Horizontal scan direction control 0: Normal 1: Mirror (effective only when register COMG[6]=1 (0x2C)) Bit[6]: Vertical scan direction control 0: Normal 1: Flip Bit[5]: Reserved Bit[4]: FSO pin output selection 0: Output signal depends on register COME[1] (0x15) 1: Output Odd field indicator Bit[3]: Gamma ON/OFF selection 0: Gamma OFF 1: Gamma ON Bit[2:1]: Reserved Bit[0]: Exposure control LSB
05	BAVG	00	RW	B Channel Average
06	GAVG	00	RW	G Channel Average
07	RAVG	00	RW	R Channel Average
08	RSVD	01	RW	Reserved
09	RSVD	00	RW	Reserved
0A	PIDH	79	R	Product ID Number MSB (Read only)
0B	PIDL	42	R	Product ID Number LSB (Read only)
0C	RSVD	41	RW	Reserved
0D	RSVD	10	RW	Reserved

Table 8 Device Control Register List (Sheet 2 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E	COMB	81	RW	Common Control B Bit[7:1]: Reserved Bit[0]: AEC step control 0: AEC max increasing step less than vertical blank 1: AEC max increasing step has no limit
0F	COMC	64 (NTSC) 62 (PAL)	RW	Common Control C Bit[7]: Sensor scanning even/odd field selection 0: Normal 1: Revised Bit[6]: BLC line selection 0: Electrical BLC 1: Optical black BLC Bit[5:0]: Reserved
10	AEC	82	RW	Automatic Exposure Control MSBs (LSB is in register COMA[0] (0x04)) AEC[8:0]: Exposure time $T_{EX} = t_{LINE}$ x AEC[8:0]
11	ADLY1	00	RW	Analog Circuit Delay Control • Range: [00] to [FF]
12	SYSC	00	RW	System Control Bit[7]: SRST 0: No change 1: Initiates reset and resets all registers to default values after which the device resumes normal operation Bit[6]: PAL/NTSC system selection 0: NTSC 1: PAL ***Note:*** *Pin 42 (ESO/PAL) selection overrules this bit[6] selection.* Bit[5:2]: Reserved Bit[1]: Color bar ON/OFF selection 0: OFF 1: ON Bit[0]: B&W mode ON/OFF 0: Color mode 1: B&W mode

Table 8 Device Control Register List (Sheet 3 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
13	AUTO	8F	RW	AEC, AGC, and AWB Auto/Manual Control Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: NTSC 50/60 Hz banding filter selection 0: 60 Hz 1: 50 Hz Bit[5]: Banding filter ON/OFF selection 0: OFF 1: ON Bit[4]: Reserved Bit[3]: Short exposure ON/OFF selection 0: Minimum AEC value is one line period 1: Enable AEC down to less than one line period Bit[2]: AGC auto/manual control selection 0: Manual 1: Auto Bit[1]: AWB auto/manual control selection 0: Manual 1: Auto Bit[0]: Exposure control 0: Manual 1: Auto
14	COMD	80	RW	Common Control D Bit[7:5]: AGC Gain Ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x Bit[4]: B&W mode maximum exposure option 0: Max exposure for PAL is 1/50s and NTSC is 1/60s 1: Max exposure for PAL is 1/25s and NTSC is 1/30s Bit[3:1]: Reserved Bit[0]: Exposure freeze ON/OFF 0: Normal 1: Exposure freeze at current value
15	COME	10	RW	Common Control E Bit[7:2]: Reserved Bit[1]: VSYNC output selection 0: Field VSYNC 1: Frame VSYNC Bit[0]: Reserved
16	COMF	08	RW	Common Control F Bit[7:0]: Reserved
17	HSTART	18 (NTSC) 1D (PAL)	RW	Horizontal Output Start Point MSBs (LSB in register HLSB[2:0] (0x32))

Table 8 Device Control Register List (Sheet 4 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
18	HEND	05 (NTSC) 03 (PAL)	RW	Horizontal Output Stop Point MSBs (LSB in register HLSB[5:3] (0x32))
19	VWSFT	00	RW	Vertical Window Shift Bit[7]: Shift direction Bit[6:0]: Shift line number
1A	ADLY3	01	RW	Analog Circuit Delay Control Range: [00] to [FF]
1B	PSHFT	00	RW	Pixel Shift Bit[7:0]: Pixel delay count - provides a method to fine tune the output timing of the pixel data relative to the HREF pulse. It physically shifts the video data output time in units of pixel clock counts.
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	PLLC	04	RW	PLL Control Bit[7:5]: Internal clock edge adjustment Bit[4]: Internal PLL reset ON/OFF selection 0: PLL power down 1: PLL ON Bit[3:2]: Internal PLL frequency selection 00: Bypass 01: 4x 10: 6x 11: 8x Bit[1:0]: Reserved
1F	RSVD	00	RW	Reserved
20-23	RSVD	80	RW	Reserved
24	AEW	78	RW	Luminance Signal High Range for AEC/AGC Operation AEC/AGC value is decreased in auto mode when the average luminance is greater than AEW[7:0]
25	AEB	68	RW	Luminance Signal Low Range for AEC/AGC Operation AEC/AGC value is increased in auto mode when the average luminance is less than AEB[7:0]
26	VV	D4	RW	Fast Mode Large Step Range Thresholds - effective only in AEC/AGC fast mode (register AUTO[7]=1 (0x13)) Bit[7:4]: High threshold Bit[3:0]: Low threshold AEC/AGC may change in larger steps when luminance average is greater than 16*VV[7:4] or less than 16*VV[3:0]
27-2A	RSVD	80	RW	Reserved
2B	RSVD	00	RW	Reserved

Table 8 Device Control Register List (Sheet 5 of 10)

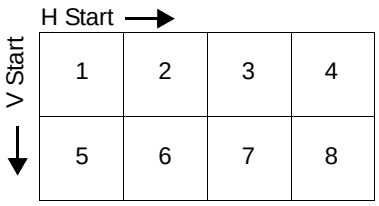
Address (Hex)	Register Name	Default (Hex)	R/W	Description
2C	COMG	80	RW	Common Control G Bit[7]: Reserved Bit[6]: Mirror option ON/OFF 0: Mirror option OFF 1: Mirror option ON Bit[5]: Y channel delay ON/OFF 0: Delay OFF 1: Delay ON Bit[4:2]: Y and UV channel delay selection Bit[1:0]: Pin FSO/FSC output selection as follows: COMG[0] COMG[1] COMA[4] COME[1] Pin FSO/FSC Output 1 x x x ADC clock 0 1 1 x FSO 0 1 0 1 Frame VSYNC 0 1 0 0 Field VSYNC
2D	AVGSL	FF	RW	16-Zone Average Window Selection LSBs, AVGS[7:0] The OV7949 uses two control bytes for the 16-zone AEC/AGC control. AVGSL[7:0] controls the top half of the image divided into two rows of four zones each. Each register bit represents a corresponding zone (i.e., AVGSL[0] represents zone 1, AVGSL[1] represents zone 2, . . ., AVGSL[7] represents zone 8). • Range: [00] (no zones selected) to [FF} (all eight zones in the top half of the image selected)  ***Note:*** *When using both AVGSL and AVGSH, note that the total number of selected zones used for average window control are 1, 2, 4, 8, or 16 zones.*

Table 8 Device Control Register List (Sheet 6 of 10)

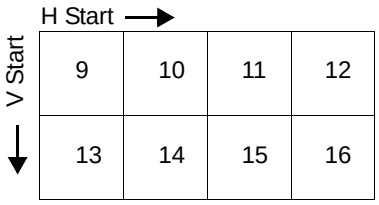
Address (Hex)	Register Name	Default (Hex)	R/W	Description
2E	AVGSH	FF	RW	16-Zone Average Window Selection MSBs, AVGS[15:8] The OV7949 uses two control bytes for the 16-zone AEC/AGC control. AVGSH[7:0] controls the bottom half of the image divided into two rows of four zones each. Each register bit represents a corresponding zone (i.e., AVGSH[0] represents zone 9, AVGSH[1] represents zone 10, . . ., AVGSH[7] represents zone 16). • Range: [00] (no zones selected) to [FF} (all eight zones in the bottom half of the image selected)  ***Note:*** *When using both AVGSL and AVGSH, note that the total number of selected zones used for average window control are 1, 2, 4, 8, or 16 zones.*
2F	YAVG	00	RW	Luminance Average Value
30	COMH	19	RW	Common Control H Bit[7:5]: Reserved Bit[4:3]: BLC line selection 00: Use both B and R line to do BLC 01: Use only R line to do BLC 10: Use only B line to do BLC 11: Use both B and R line to do BLC Bit[2:0]: Reserved
31	COMI	0B	RW	Common Control I Bit[7:6]: Digital gain setting 00: Digital gain bypass 01: 0.75x 10: 1.5x 11: 3x Bit[5:0]: Reserved
32	HLSB	00 (NTSC) 12 (PAL)	RW	Horizontal Output Start and End Position LSBs Bit[7:6]: Reserved Bit[5:3]: End point LSBs Bit[2:0]: Start point LSBs
33	RSVD	07	RW	Reserved
34	ACUR1	72	RW	Analog Circuit Current Control • Range: [00] to [FF]
35	ACUR2	02	RW	Analog Circuit Current Control • Range: [00] to [FF]
36	VREF1	E7	RW	Analog Circuit Reference Control • Range: [00] to [FF]
37	ADC1	04	RW	ADC Reference Control • Range: [00] to [FF]

Table 8 Device Control Register List (Sheet 7 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
38	ADC2	C0	RW	ADC Reference Control • Range: [00] to [FF]
39	SREF1	00	RW	Sensor Reference Control • Range: [00] to [FF]
3A	SREF2	7A	RW	Sensor Reference Control • Range: [00] to [FF]
3B	SREF3	20	RW	Sensor Reference Control • Range: [00] to [FF]
3C	COMJ	03	RW	Common Control J Bit[7]: Reserved Bit[6:4]: Reserved Bit[3]: DAC power down selection 0: Normal 1: Power down DAC Bit[2:0]: DAC 3-channel individual power down selection 0: Normal 1: Power down specific DAC channel
3D-46	RSVD	XX	–	Reserved
47	GFIX	00	RW	Analog Channel Fixed Gain Control Bit[7:6]: B channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[5:4]: Gb channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[3:2]: Gr channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x Bit[1:0]: R channel fixed gain 00: 1x 01: 1.25x 10: 1.5x 11: 1.75x
48-7A	RSVD	XX	–	Reserved
7B	SLOP	24	RW	Gamma Curve Highest Segment Slop Should be calculated as follows: SLOP[7:0] = (FF - GAM15[7:0] + 1) x 40/30 ***Note:*** *Use hex numbers for calculation*
7C	GAM1	0F	RW	Gamma Curve - 1st segment input end point 0x010 output value
7D	GAM2	1F	RW	Gamma Curve - 2nd segment input end point 0x020 output value

Table 8 Device Control Register List (Sheet 8 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
7E	GAM3	36	RW	Gamma Curve - 3rd segment input end point 0x040 output value
7F	GAM4	54	RW	Gamma Curve - 4th segment input end point 0x080 output value
80	GAM5	5F	RW	Gamma Curve - 5th segment input end point 0x0A0 output value
81	GAM6	6A	RW	Gamma Curve - 6th segment input end point 0x0C0 output value
82	GAM7	74	RW	Gamma Curve - 7th segment input end point 0x0E0 output value
83	GAM8	7C	RW	Gamma Curve - 8th segment input end point 0x100 output value
84	GAM9	84	RW	Gamma Curve - 9th segment input end point 0x120 output value
85	GAM10	8C	RW	Gamma Curve - 10th segment input end point 0x140 output value
86	GAM11	9A	RW	Gamma Curve - 11th segment input end point 0x180 output value
87	GAM12	A7	RW	Gamma Curve - 12th segment input end point 0x1C0 output value
88	GAM13	BF	RW	Gamma Curve - 13th segment input end point 0x240 output value
89	GAM14	D3	RW	Gamma Curve - 14th segment input end point 0x2C0 output value
8A	GAM15	E5	RW	Gamma Curve - 15th segment input end point 0x340 output value
8B	RSVD	8E	RW	Reserved
8C	SHP1	A1	RW	Sharpness Control 1 Bit[7]: Sharpness ON/OFF selection 0: OFF 1: ON Bit[6]: Sharpness strength selection 0: Normal 1: Sharpness doubled Bit[5:0]: Reserved
8D	SHP2	20	RW	Sharpness Control 2 Bit[7:4]: Sharpness strength coefficients • Range: [00] to [0F] Bit[3:0]: Reserved
8E	SHP3	40	RW	Sharpness Control 3 Bit[7:2]: Sharpness threshold control • Range: [00] to [3F] Bit[1:0]: Reserved
8F	RSVD	10	RW	Reserved
90	MTX1	BB	RW	Color Matrix Coefficient 1
91	MTX2	AE	RW	Color Matrix Coefficient 2
92	MTX3	0D	RW	Color Matrix Coefficient 3
93	MTX4	1B	RW	Color Matrix Coefficient 4
94	MTX5	62	RW	Color Matrix Coefficient 5
95	MTX6	7D	RW	Color Matrix Coefficient 6

Table 8 Device Control Register List (Sheet 9 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
96	MSIGN	1E	RW	Color Matrix Coefficient Sign Bit[7]: Matrix coefficients control 0: Normal 1: Double all coefficients Bit[6]: Reserved Bit[5:0]: Matrix coefficients sign bits for MTX6 to MTX1 0: Plus 1: Minus
97	BRT	98	RW	Brightness Control Bit[7]: Brightness direction 0: Increase 1: Decrease Bit[6:0]: Brightness control
98	CNTR1	40	RW	Contrast Control • Range: [00] to [FF]
99	CNTR2	80	RW	Contrast Control Center Value
9A	RSVD	30	RW	Reserved
9B	ENC1	C8	RW	Encoder Output White Signal Level
9C	ENC2	3C	RW	Encoder Output Blanking Level
9D	ENC3	23	RW	Encoder Output Burst Level
9E	ENC4	04	RW	Encoder Output Sync Level
9F	ENC5	46	RW	Encoder Output Black Signal Level
A0-AA	RSVD	XX	RW	Reserved
AB	ENC6	08 (NTSC) 10 (PAL)	RW	Encoder Control Byte 6 Bit[7:1]: Reserved Bit[0]: Encoder color bar output ON/OFF selection 0: OFF 1: ON
AC-BB	RSVD	XX	RW	Reserved
BC	OHSFT	00	RW	Overlay Horizontal Pixel Shift • Range: [00] to [FF]

Table 8 Device Control Register List (Sheet 10 of 10)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
BD	OVLY	00	RW	Overlay Control Bit[7]: Reserved Bit[6:5]: Overlay opacity 00: 25% 01: 50% 10: 75% 11: 100% Bit[4:3]: Overlay resolution 00: 2x2 01: 3x3 10: 4x4 11: 5x5 Bit[2]: Overwrite option 0: $Y = r\% \times Y_{ovly} + (1 - r\%)Y_{ori}$ $U = r\% \times U_{ovly} + (1 - r\%)U_{ori}$ $V = r\% \times V_{ovly} + (1 - r\%)V_{ori}$ 1: $Y = r\% \times Y_{ovly} + (1 - r\%)Y_{ori}$ $U = U_{ovly}$ $V = V_{ovly}$ ***Note:*** *r% = Overlay opacity (register bits OVLY[6:5])* *Y_{ovly} = Y Overlay Value (register YOVLY 0xBE)* *U_{ovly} = U Overlay Value (register UOVLY 0xBF)* *V_{ovly} = V Overlay Value (register VOVLY 0xC0)* *Y_{ori} = Original Y data* *U_{ori} = Original U data* *V_{ori} = Original V data* Bit[1:0]: Reserved
BE	YOVLY	00	RW	Y Overlay Value
BF	UOVLY	00	RW	U Overlay Value
C0	VOVLY	00	RW	V Overlay Value
C1	OVRSM	00	RW	Overlay Start Line Address MSBs
C2	OVREM	00	RW	Overlay End Line Address MSBs
C3	OVHSM	00	RW	Overlay Start Column Address MSBs
C4	OVHEM	00	RW	Overlay End Column Address MSBs
C5	OVRHL	00	RW	Overlay Position LSBs Bit[7:6]: Overlay start line address LSBs Bit[5:4]: Overlay end line address LSBs Bit[3:2]: Overlay start column address LSBs Bit[1:0]: Overlay end column address LSBs
C6	MENLN	00	RW	Number of bytes per line used in bit map file
C7-D2	RSVD	00	RW	Reserved
D3	RLMT	F0	RW	AWB R Gain Limit
D4	GLMT	F0	RW	AWB G Gain Limit
D5	BLMT	F0	RW	AWB B Gain Limit
D6-EC	RSVD	XX	RW	Reserved

NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.

Package Specifications

The OV7949/OV7449 uses a 48-pin Quad Flat Package (QFP). Refer to Figure 16 and Table 9 for QFP information and Figure 17 for the sensor array center.

Figure 16 OV7949/OV7449 QFP Specifications

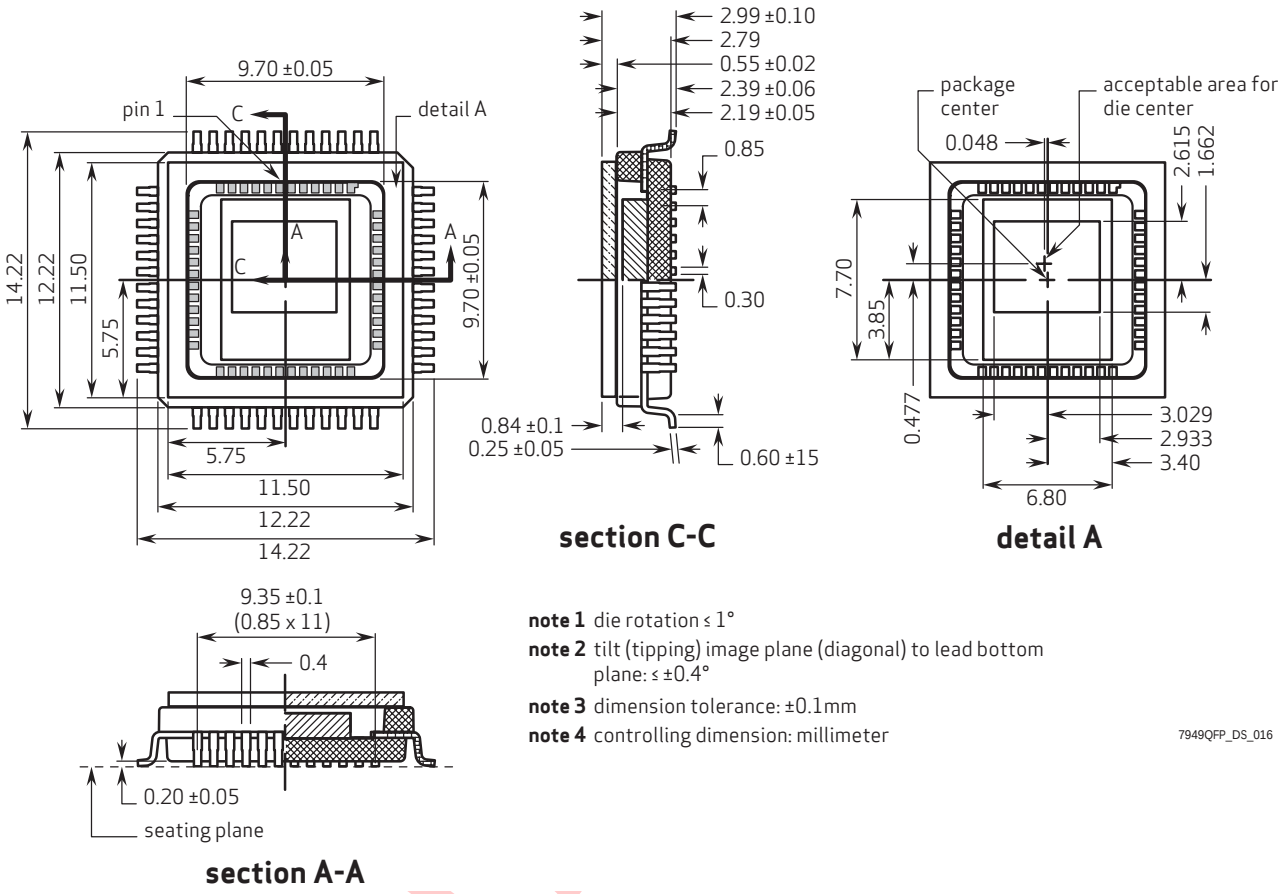
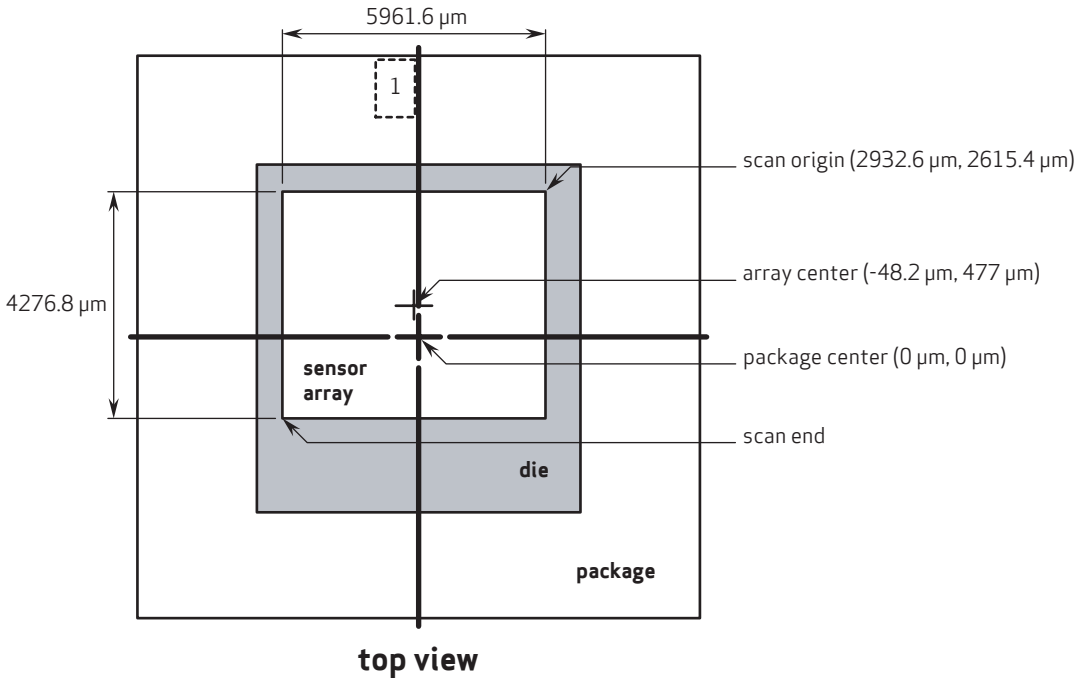


Table 9 OV7949/OV7449 QFP Dimensions

Dimensions	Millimeters (mm)	Inches (in.)
Package Size	14.22 ± 0.1	0.560 ± 0.004
Package Height	2.99 ± 0.10	0.118 ± 0.004
Lead Width	0.30 ± 0.1	0.012 ± 0.004
Lead Pitch	0.85 ± 0.1	0.033 ± 0.004
Glass Size	11.5 ± 0.1 SQ	0.453 ± 0.004 SQ
Glass Height	0.55 ± 0.02	0.022 ± 0.001
Die Thickness	0.733 ± 0.015	0.0289 ± 0.001
Top of Glass to Image Plane	0.84 ± 0.1	0.033 ± 0.004
Substrate Height	2.19 ± 0.05	0.086 ± 0.002

Sensor Array Center

Figure 17 OV7949/OV7449 Sensor Array Center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin 1 oriented down on the PCB.

7949QFP_DS_017

IR Reflow Ramp Rate Requirements

OV7949/OV7449 Lead-Free Packaged Devices

Figure 18 IR Reflow Ramp Rate Requirements

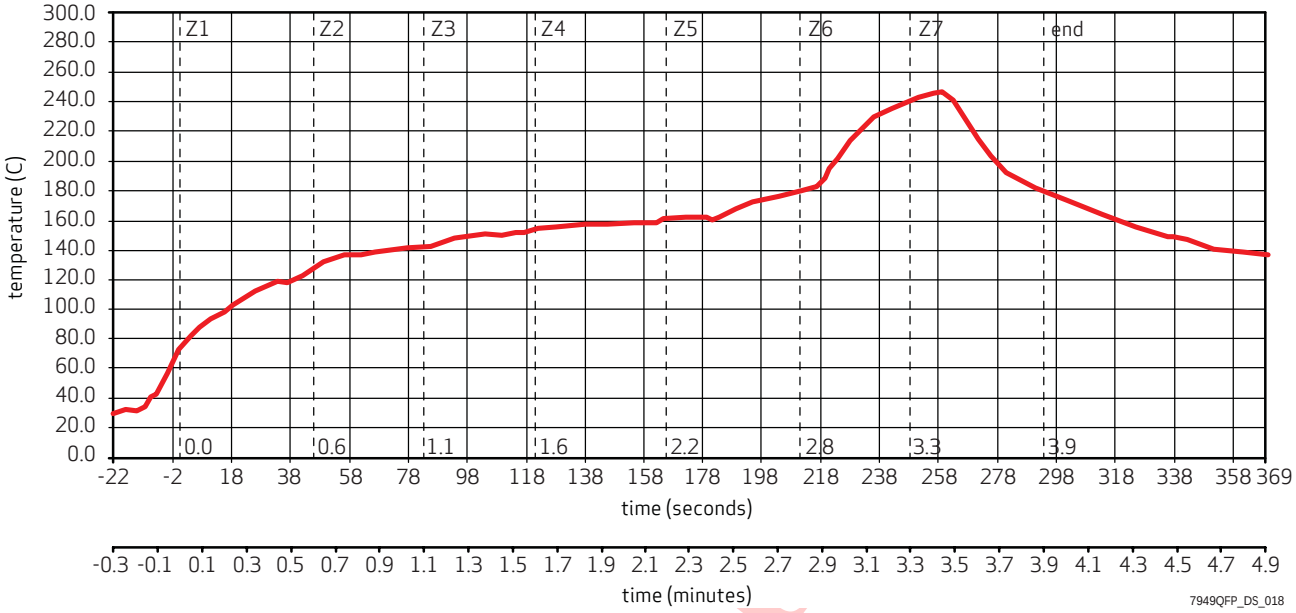


Table 10 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 245°C	No greater than 390 seconds

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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REVISION CHANGE LIST

Document Title: OV7949 Datasheet (auto) **Version:** 1.0

DESCRIPTION OF CHANGES

- Initial Release

REVISION CHANGE LIST

Document Title: OV7949 Datasheet **Version:** 1.1

DESCRIPTION OF CHANGES

The following changes were made to version 1.0:

- In Table 3 on page 9, changed Min and Max for Storage temperature from “0°C” and “+40°C” to “-40°C” and “+125°C”, respectively.
- On page 16, replaced Spectral Response graph with graph using thinner lines.
- In Table 3 on page 9, added the footnote: “Exceeding the stresses listed may permanently damage the device. This is a stress rating only and functional operation of the sensor at these and any other condition above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for any extended period may affect reliability.”

REVISION CHANGE LIST

Document Title: OV7949 Datasheet **Version:** 1.2

DESCRIPTION OF CHANGES

The following changes were made to version 1.1:

- Under Key Specifications on page 1, changed Power Consumption from “250 mW” to “168 mW”
- Under Key Specifications on page 1, changed Sensitivity from “2.26 V/Lux-sec @ 5600K” to “4.6 V/Lux-sec @ 5600K”
- Under Key Specifications on page 1, changed S/N Ratio from “47 dB (Max)” to “48 dB”

REVISION CHANGE LIST

Document Title: OV7949 Datasheet **Version:** 1.3

DESCRIPTION OF CHANGES

The following changes were made to version 1.2:

- Under Key Specifications on page 1, changed Sensitivity from “4.6 V/Lux-sec @ 5600K” to “4.7 V/Lux-sec @ 5600K”
- Added B&W version (OV7449) to datasheet including part numbers OV07449-Q10V and OV07449-Q20V under Ordering Information on page 1 and changed references to “OV7949” to “OV7949/OV7449” throughout the document