OmniVision

datasheet

PRODUCT SPECIFICATION

color CMOS analog NTSC image sensor with OmniPixel3-HS™ technology for automotive applications

OV7955 (rev 2E)

color CMOS analog NTSC image sensor with OmniPixel3-HS™ technology for automotive applications

datasheet (aCSP)
PRODUCT SPECIFICATION

version 2.21
october 2012

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- rear view camera
- 360° view
- front sensing camera
- blind spot detection
- night vision

ordering information

- **OV07955-N53V-RE** (color, NTSC, lead-free)
  53-pin aCSP™, rev 2E, 50°C with protective film in tape and reel
- **OV07955-N53V-PE** (color, NTSC, lead-free)
  53-pin aCSP™, rev 2E, 50°C with protective film in tray

features

- VGA DV output
- NTSC TV output (see **sidebar note**)
- high sensitivity
- automatic exposure/gain with 16 zone control
- auto white balance control
- aperture/gamma correction
- slave compatible serial camera control bus (SCCB) control interface for register programming
- crop and re-size
- low power consumption
- low dark current
- overlay with two layers, eight colors, and four transparencies
- 1280 bits of one time programmable memory (OTP)
- SPI master for overlay images and loading setting
- dynamic overlay controls
- defective pixel correction

note

Since it is impossible to check compatibility with all displays, check the interoperability before committing to mass production.

key specifications (typical)

- **active array size:** 672 x 492
- **power supply:**
  core: 1.5V
  analog: 3.14 ~ 3.47V
  I/O: 1.7 ~ 3.47V
- **power requirements:**
  active: 200 mW
  standby: 20 µA
- **temperature range:**
  operating: -40°C to +105°C sensor ambient temp (operating sensor ambient temperatures above +60°C may result in degraded image quality) (see **table 8-2**)
- **optical size:**
  NTSC: 1/3.7"
- **chief ray angle:** supports up to 25°
- **output formats:** NTSC (TV port), VGA (DV port)
- **maximum image transfer rate:**
  VGA: 60 fps (DV)
  NTSC: 60 fields per second (TV)
- **sensitivity:** 16 V/Lux-sec
- **shutter:** rolling shutter
- **max S/N ratio:** 38 dB
- **dynamic range:** 71 dB @ 8x gain
- **scan mode:** progressive
- **pixel size:** 6.0 µm x 6.0 µm
- **dark current:** 10.7 mV/s @ 60°C junction temp
- **image area:** 4032 µm x 2952 µm
- **package dimensions:** 5660 µm x 5360 µm

table of contents

list of figures

list of tables

1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7955 image sensor. The package information is shown in section 9.

table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
A1	ECK	I/O	SPI clock (output by default)
A2	DOVDD	power	1.8~3.3V power for I/O circuit
A3	SIOC	input	SCCB input clock
A4	FLIP	input	vertical flip enable
A5	SGND	ground	ground for sensor
A6	BW	input	BW mode enable
A7	VBH	reference	internal analog reference
A8	VH	reference	internal analog reference
B1	ESI	input	SPI data input (ESI needs pull down resistor if not used)
B2	ESO	I/O	SPI data (output by default)
B3	SIOD	I/O	SCCB data
B4	FSIN	I/O	frame sync
B5	SVDD	power	3.3V analog power for sensor
B6	PWDN	input	power down input (active high with internal weak pull down)
B7	VRES	reference	internal analog reference
B8	VN	reference	internal analog reference
C1	AVDD	power	3.3V power for analog circuit
C2	DOGND	ground	ground for I/O circuit
C3	ECS	I/O	SPI chip select (output by default)
C4	MIR	input	mirror enable
C5	OVEN	input	overlay enable
C6	TM	input	test mode enable
C7	VBL	reference	internal analog reference
C8	AVDD	power	3.3V power for analog circuit
D1	AGND	ground	ground for analog circuit

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
D2	NC	–	no connect
D8	AGND	ground	ground for analog circuit
G1	DVDD	power	1.5V power for digital circuit
G8	OGND	ground	analog ground for DAC
H1	DGND	ground	ground for digital circuit
H2	D4	I/O	DVP output data 4
H3	HREF	I/O	DVP HREF output
H4	DOGND	ground	ground for I/O circuit
H5	DOVDD	power	1.8~3.3V power for I/O circuit
H6	DGND	ground	ground of digital circuit
H7	PVDD	power	3.3V analog power for PLL
H8	VOP	output	DAC positive output
J1	DOVDD	power	1.8~3.3V power for I/O circuit
J2	VSYNC	I/O	DVP VSYNC output
J3	D0	I/O	DVP output data 0
J4	D1	I/O	DVP output data 1
J5	D5	I/O	DVP output data 5
J6	D7	I/O	DVP output data 7
J7	XI	input	oscillator input
J8	VON	output	DAC negative output
K1	DOVDD	power	1.8~3.3V power for I/O circuit
K2	D6	I/O	DVP output data 6
K3	D2	I/O	DVP output data 2
K4	PCLK	I/O	DVP output clock
K5	D3	I/O	DVP output data 3
K6	DVDD	power	1.5V power for digital circuit
K7	XO	output	oscillator output
K8	OVDD	power	3.3V analog power for DAC

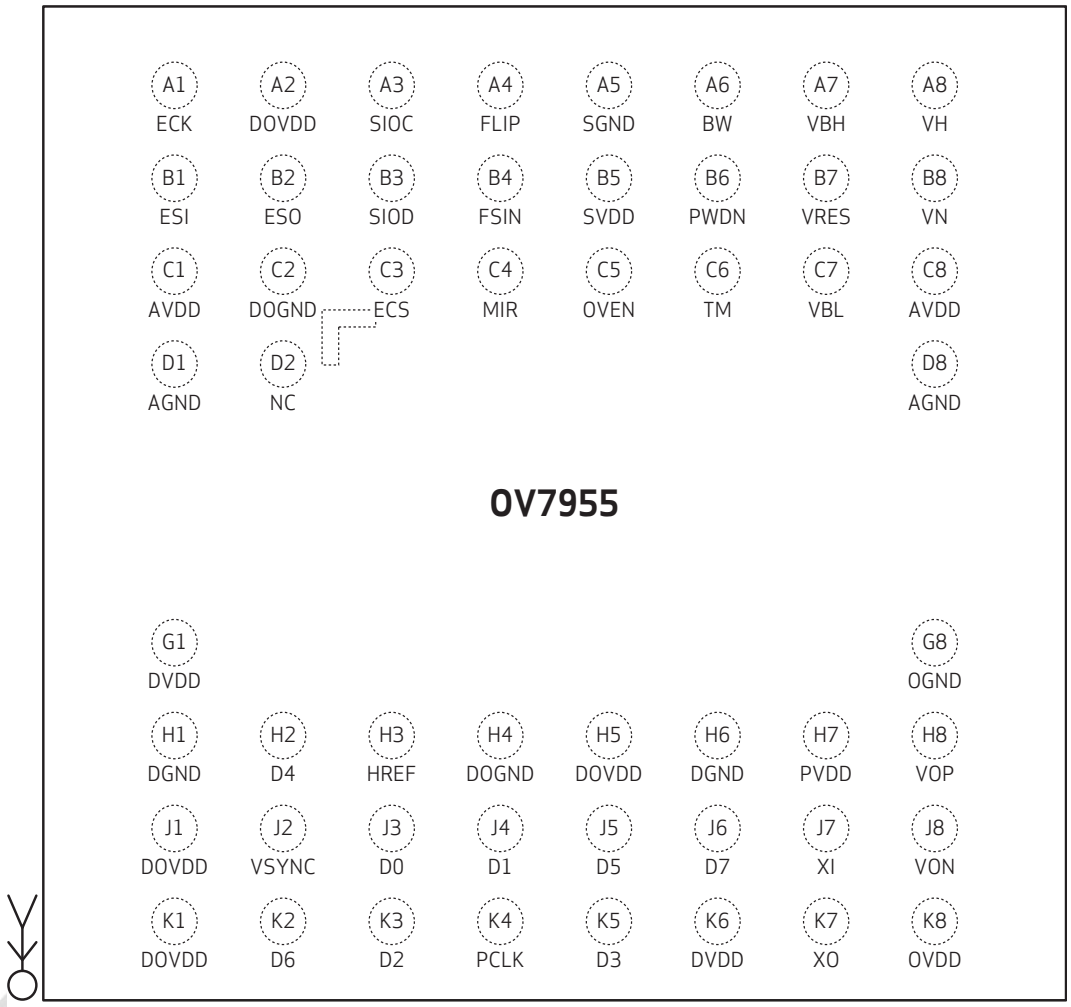
table 1-2 configuration under various conditions (sheet 1 of 2)

pin number	signal name	PWDN=0 OVEN=0	PWDN=0 OVEN=1	PWDN=1 OVEN=0	PWDN=1 OVEN=1	standby OVEN=0	standby OVEN=1
A1	ECK	input	output	high-z	low	input	output low
A3	SIOC	input	input	high-z	high-z	input	input
A4	FLIP	input	input	input	input	input	input
A6	BW	input	input	input	input	input	input
B1	ESI	input	input	high-z	high-z	input	input
B2	ESO	input	output	high-z	low	input	output low
B3	SIOD	input + open-drain	input + open-drain	high-z	high-z	input + open-drain	input + open-drain
B4	FSIN	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
B6	PWDN	input	input	input	input	input	input
C3	ECS	input	output	high-z	low	input	output high
C4	MIR	input	input	input	input	input	input
C5	OVEN	input	input	input	input	input	input
C6	TM	input	input	input	input	input	input
H2	D4	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
H3	HREF	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
H8	VOP	open-drain	open-drain	high-z	high-z	open-drain	open-drain
J2	VSYNC	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
J3	D0	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
J4	D1	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
J5	D5	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default

table 1-2 configuration under various conditions (sheet 2 of 2)

pin number	signal name	PWDN=0 OVEN=0	PWDN=0 OVEN=1	PWDN=1 OVEN=0	PWDN=1 OVEN=1	standby OVEN=0	standby OVEN=1
J6	D7	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
J7	XI	input	input	high-z	high-z	input	input
J8	VON	open-drain	open-drain	high-z	high-z	open-drain	open-drain
K2	D6	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
K3	D2	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
K4	PCLK	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
K5	D3	input by default	input by default	high-z by default (configurable)	high-z by default (configurable)	input by default	input by default
K7	XO	output	output	high	high	output	output

figure 1-1 pin diagram



7955_aCSP_DS_1_1

top view

2 system level description

2.1 overview

The OV7955 color image sensor is a low voltage, high performance CMOS image sensor that provides the full functionality of a single chip digital/analog NTSC image sensor using OmniPixel3-HS™ technology in a small footprint package. The image processing circuit also features black level calibration, lens correction, advanced auto white balance, auto exposure control, white/black pixel correction, color matrix and interpolation. It provides full-frame images via the control of the Serial Camera Control Bus (SCCB) interface. This product is ideal for applications requiring a small footprint, low voltage, low power and low cost color video camera.

2.2 architecture

The OV7955 sensor core generates streaming pixel data at a constant frame rate with analog and digital outputs.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling the rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV7955 block diagram

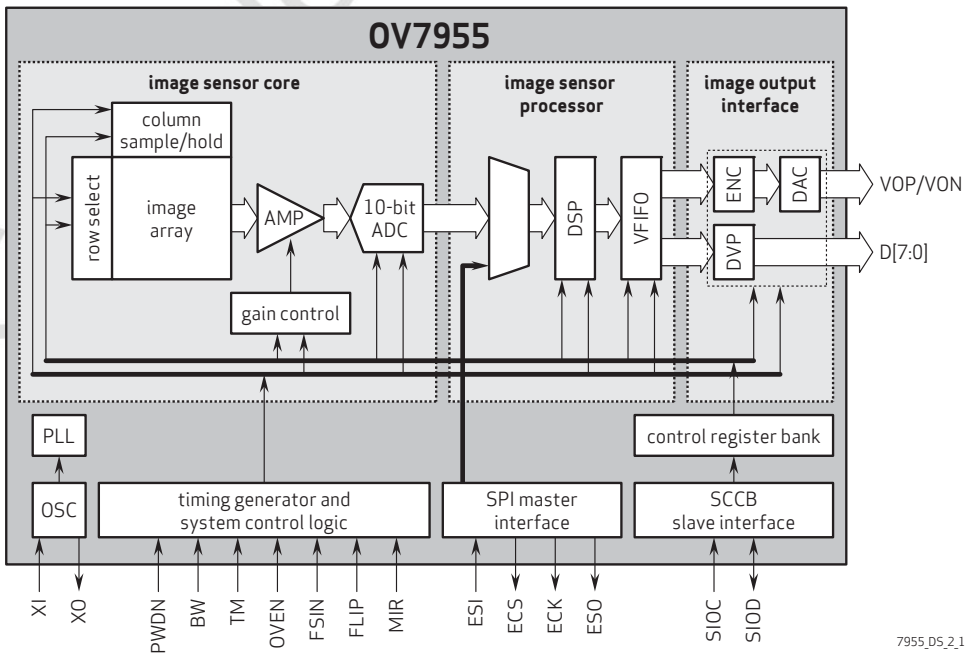
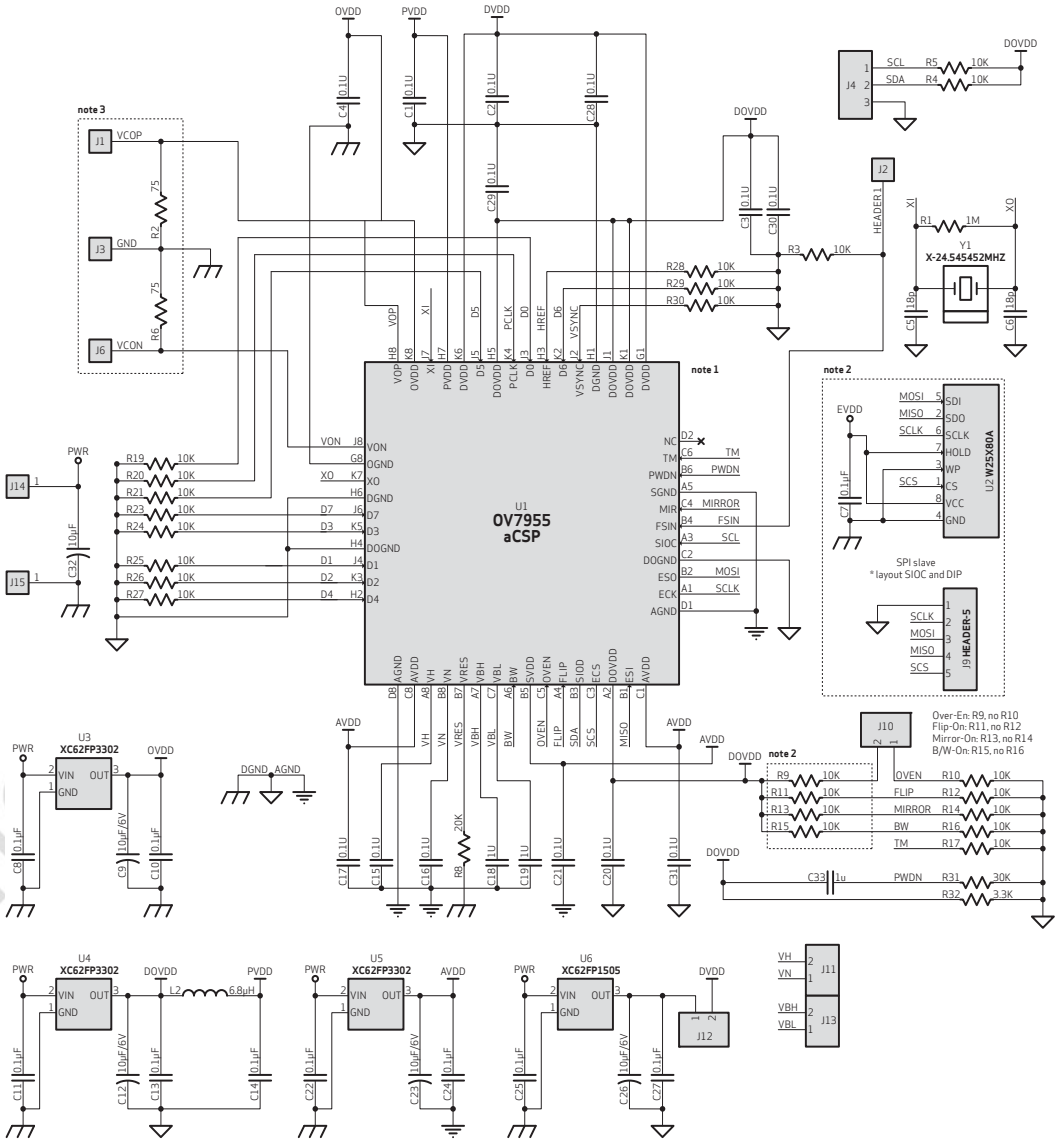


figure 2-2 OV7955 reference schematic



note 1 with the default register settings, DVP pins[D7:D0] are set as inputs as inputs they should be tied to ground through a resistor and not left floating. if registers 0x3001[7:0] are set to 1 then DVP pins [D7:D0] are outputs and may be left floating

note 2 install upon request and remove corresponding pull down resistor

note 3 install VCOP wire and R6 for general analog applications
no R2 and R6 if differential video is used
add both R2 and R6 for digital applications

7955_aCSP_DS_2_2

2.3 PLL control

The OV7955 PLL allows input clock frequencies ranging from 6~27 MHz and has a maximum VCO frequency of 120 MHz and minimum of 96 MHz. For NTSC output, the input clock frequency should be 24.545452 MHz.

figure 2-3 PLL control diagram

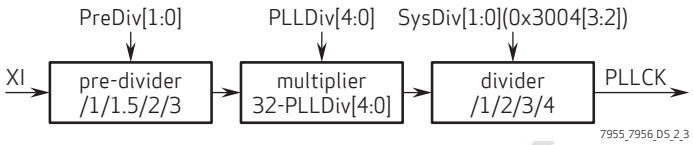


table 2-1 PLL control registers

address	register name	default value	R/W	description
0x3003	PLL CTRL0	0x1C	RW	Bit[7:5]: pll_cp PLL reference current options Bit[4:0]: pll_multiplier = 32 - 0x3003[4:0]
0x3004	PLL CTRL1	0x02	RW	Bit[7:4]: Debug mode Bit[3:2]: pll_sdiv System divider of PLL 00: /1 01: /2 10: /3 11: /4 Bit[1:0]: pll_prediv Pre-divider of PLL 00: /1 01: /1.5 10: /2 11: /3

2.4 external interface

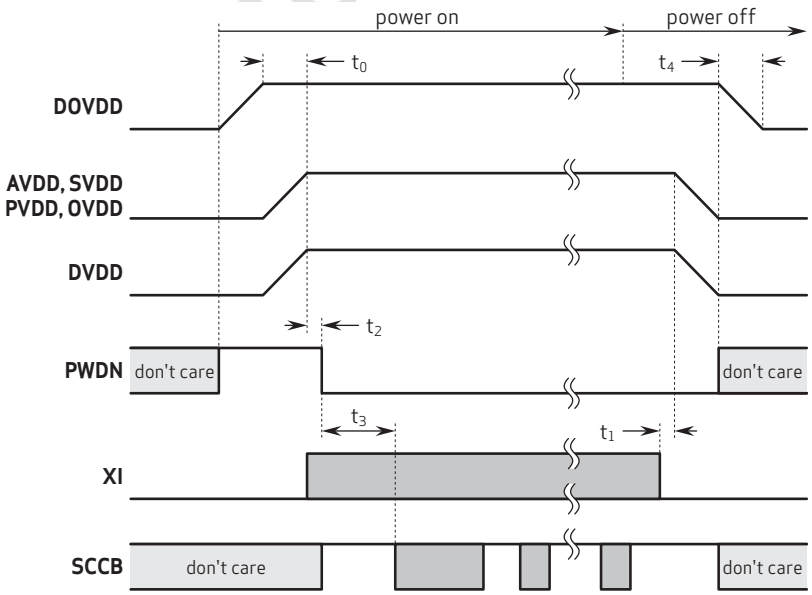
Image sensor power is provided from a 3.3V (typical) system power supply. An internal regulator provides 1.5V for core logic with I/O power (DOVDD). Typical I/O pad power is 3.3V.

2.5 power up sequence

For powering up with the internal DVDD and SCCB access during the power ON period, the following conditions must occur:

1. when DOVDD and AVDD are turned ON, make sure DOVDD becomes stable before AVDD becomes stable
2. PWDN is active high with an asynchronized design (does not need clock)
3. PWDN must be high during the power on period
4. for PWDN to go low, power must first become stable (AVDD to PWDN ≥ 5 ms)
5. master clock should be provided at least 2 ms before host accesses the sensor's registers
6. host can access SCCB bus (if shared) during entire period. 20 ms after PWDN goes low, host can access the sensor's registers to initialize the sensor

figure 2-4 power up timing sequence



note $t_0 \geq 0$ ms, delay from DOVDD stable to AVDD stable,
it is recommended to power up AVDD shortly after DOVDD has been powered up

$t_1 \geq 0$ ms, delay from XI off to AVDD off

$t_2 \geq 5$ ms, delay from AVDD stable to sensor power up stable, PWDN can be pulled low after this point, XI can be turned on after power on

$t_3 \geq 20$ ms, delay from PWDN pull low to SCCB initialization

$t_4 \geq 0$ ms, delay from AVDD off to DOVDD off

7955_7956_DS_2_4

2.6 power management

During power down, all registers keep their values. So, during the resume state, all the registers are restored to their original values.

In power down mode, the clock input of each block is turned off even when the external clock source is still clocking.

2.7 reset

The OV7955 clears all registers and resets them to their default values when system is powered on. A reset can also be initiated through the SCCB interface by setting register **0x0103**[0] to high. Reset requires ~2ms settling time.

2.7.1 power ON reset generation

The power on reset is generated internally after core power becomes stable.

2.8 hardware and software standby

Two suspend modes are available for the OV7955:

- **hardware standby**
- **software standby**

2.8.1 hardware standby

To initiate a hardware standby, the **PWDN** pin (pin **B6**) must be tied to high. When this occurs, the OV7955 internal device clock is halted and all internal counters are reset and registers are maintained. Majority of the digital circuitry will remain in the power-cut state.

2.8.2 software standby

Executing a software standby through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.8.3 system clock

The on-chip PLL takes 24.545452 MHz (NTSC). Clock signals are from an external crystal. A clock divider is provided to generate different system frequencies.

2.9 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

2.10 analog format

table 2-2 analog format and frame rate

function	format	resolution	field rate	input clock
analog output	NTSC	648x488	60 fields/sec	24.545452 MHz

3 block level description

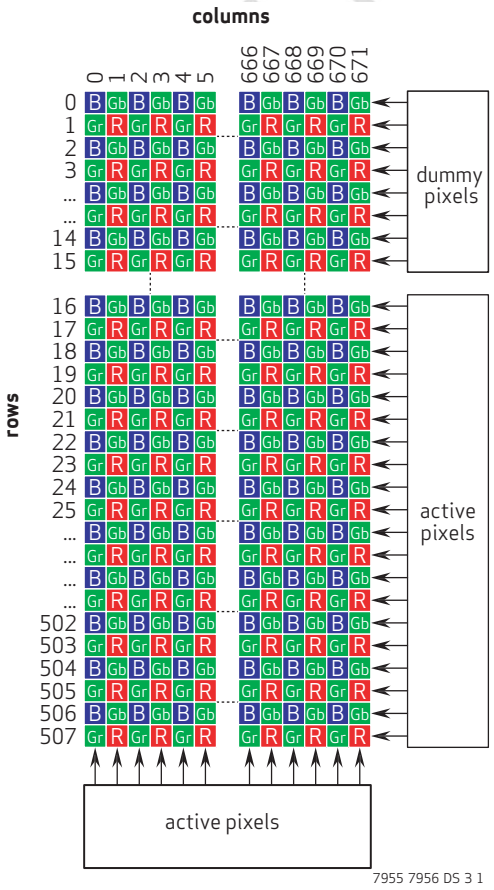
3.1 pixel array structure

The OV7955 sensor has an image array of 672 columns by 508 rows (341,376 pixels). figure 3-1 shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 341,376 pixels, 672 x 492 (330,624) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7955 provides mirror mode, which reverses the sensor data read-out order horizontally, and flip mode which reverses it vertically (see **figure 4-1**).

There are two ways to set mirror and flip modes:

- from the pad MIR and FLIP
- from register 0x3821 and 0x3820

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

7955 7956 DS 4 1

table 4-1 mirror and flip control registers

function	register	description
mirror	0x3821	Bit[2:1]: mirror ON/OFF select 00: mirror OFF 01: not allowed 10: not allowed 11: mirror ON
flip	0x3820	Bit[2:1]: flip ON/OFF select 00: flip OFF 01: not allowed 10: not allowed 11: flip ON

table 4-2 mirror and flip hardware control

function	description
mirror	use MIR pin to control 0: mirror OFF 1: mirror ON
flip	use VFLIP pin to control 0: flip OFF 1: flip ON

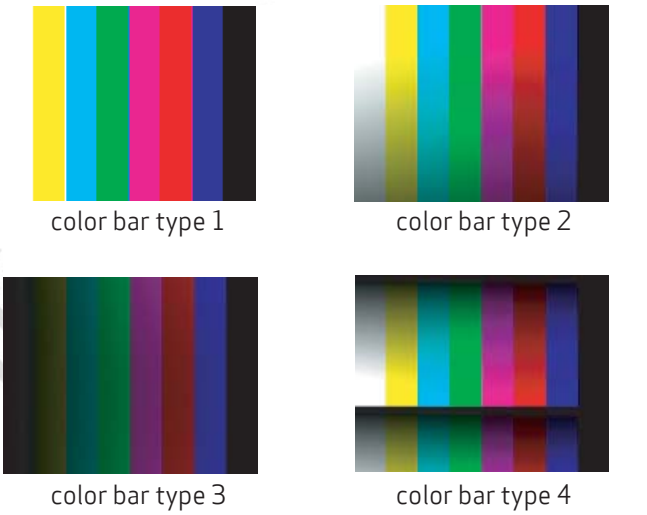
4.2 test pattern

For testing purposes, the OV7955 offers three types of test pattern: color bar, square, random data. The OV7955 also offers two effects: transparent effect and rolling bar effect. The output type of test pattern is controlled by test_mode register (0x5080[1:0]).

4.2.1 color bar

There are four types of color bar which are switched by color_bar_style register (0x5080[3:2]).

figure 4-2 color bar types

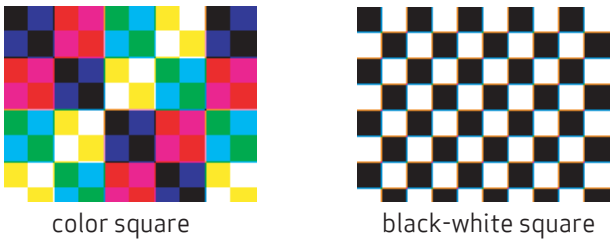


7955_7956_DS_4_2

4.2.2 square

There are two types of square: color square and black-white square. The square_mode register (0x5080[4]) decides which type of square will be output.

figure 4-3 color, black and white square bars



7955_7956_DS_4_3

4.2.3 random data

There are two types of random data test pattern: frame-changing and frame-fixed random data. The output type of random data is decided by same_seed_en register (0x5081[4]). The random seed is set by seed register (0x5081[3:0]).

4.2.4 transparent effect

The transparent effect is enabled by transparent_en register (0x5080[5]). If this register is set, the transparent test pattern will be shown. The following image is an example which shows a transparent color bar image.

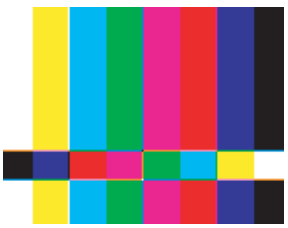
figure 4-4 transparent effect

7955_7956_DS_4_4

4.2.5 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5080[6]). If it is set, an inverted-color rolling bar will roll from up to down. The following image is a example which shows a rolling bar on color bar image.

figure 4-5 rolling bar effect



7955_7956_DS_4_5

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x5080	PRECTRL00	0x00	RW	Bit[7]: test_en 0: Disable test function 1: Enable test function Bit[6]: rolling_bar_en 0: Disable rolling bar function 1: Enable rolling bar function Bit[5]: transparent_en 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: square_mode 0: Color square 1: Black white square Bit[3:2]: color_bar_style 00: Standard color bar 01: Top bottom darker color bar 10: Right-left darker color bar 11: Bottom top darker color bar Bit[1:0]: test_mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5081	PRE CTRL01	0x41	RW	Bit[4]: same_seed_en When this is set, the seed used to generate the random data is same as set in the seed register Bit[3:0]: Seed This is the seed used in generating random data

4.3 AEC/AGC algorithms

The auto exposure control (AEC) and auto gain control (AGC) allow the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain for the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in AEC/AGC algorithms **table 4-4**.

table 4-4 AEC/AGC function controls

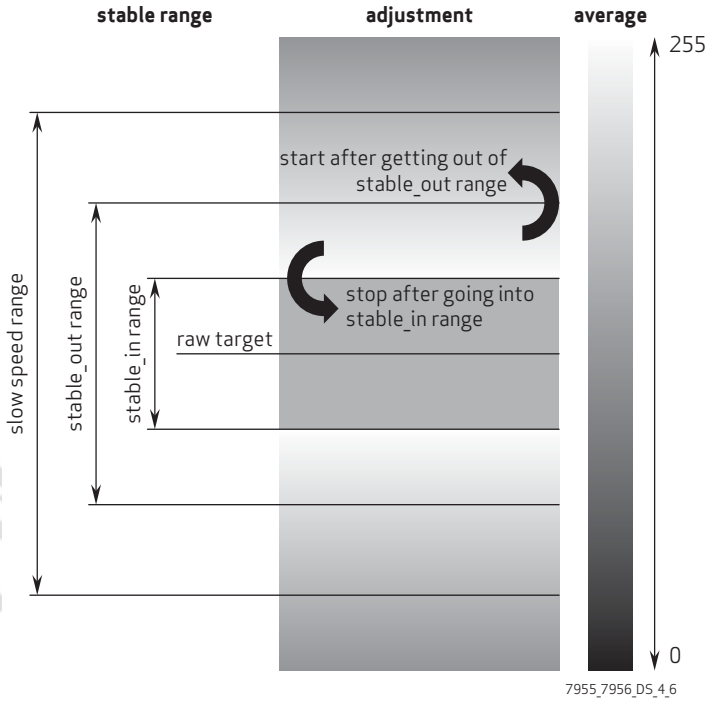
function	register	description
AEC enable	0x3503	Bit[0]: AEC enable 0: Auto enable 1: Manual enable
AEC (exposure time)	{0x3500~0x3502}	0x3502 = AEC[7:0] 0x3501 = AEC[15:8] 0x3500 = AEC[19:16]
AGC enable	0x3503	Bit[1]: AGC enable 0: Auto enable 1: Manual enable
AGC (gain)	0x350A~0x350B	0x350A = analog_gain_code_global[10:8] 0x350B = analog_gain_code_global[7:0]

The average-based algorithms tell whether the current frame is too bright or too dark and determine if the exposure time/gain should increase or decrease for the next frame. It is based on the weighted average of a frame.

4.3.1 average-based algorithm

4.3.1.1 automatic adjustment step mode

figure 4-6 automatic adjustment step mode diagram



- AEC/AGC target is automatically set in the middle of the stable_in range
- manual exposure mode: 0x3503[0]=1
- manual exposure registers: 0x3500, 0x3501, 0x3502
  - exposure = 1/fps
  - value is converted to hex, then 0x3500[3:0] = exposure[19:16], 0x3501[7:0] = exposure[15:8] and 0x3502[7:0] = exposure[7:0]
- manual gain mode: 0x3503[1] = 1
- manual gain registers: 0x350A (MSB), 0x350B (LSB)
  - type of manual gain used: 0x3503[2]
    0x01: sensor gain
    0x00: real gain
- sensor gain is calculated as (1 + (bit[3:0]/16)) x (1+ bit[4]) x (1 + bit[5])...x (1 + bit[15])
  - if bit[3:0] = 0x0F, then the sensor rounds up to 16 instead
- real gain is calculated as: (gain registers)/16

If the current frame exposure is above or below the stable_out range, the sensor will automatically adjust the exposure by the defined fast adjustment step. After this, if the exposure falls between the stable_in and stable_out range, the exposure will be adjusted by the defined slow adjustment step until it reaches the target area.

The sensor will not adjust the exposure again until it falls outside of the stable_out range. This is to prevent oscillation in the image from the sensor adjusting too often.

Automatic step adjustment step size formula is as follows:
Step = abs(target-average)/average)×ratio(0x3A05[4:0])

figure 4-7 AEC/AGC speed (step) diagram

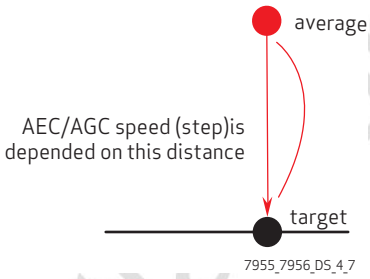


table 4-5 slow adjustment step functions

function	description
stable_in range	upper: 0x3A0F, lower: 0x3A10
stable_out range	upper: 0x3A1B, lower: 0x3A1E
auto step adjustment mode	0x3A05[5] = 1
fast adjustment step	current exposure or gain ×2 if below slow speed range, /2 if above slow speed range
slow adjustment step	next frame exposure or gain = (current exposure or gain) + (current exposure or gain)/16 if in lower stable_out range, (current exposure or gain) - (current exposure)/16 if in upper stable_out range

4.3.1.2 manual adjustment step mode
Manual step AEC is enabled via 0x3A05[5]

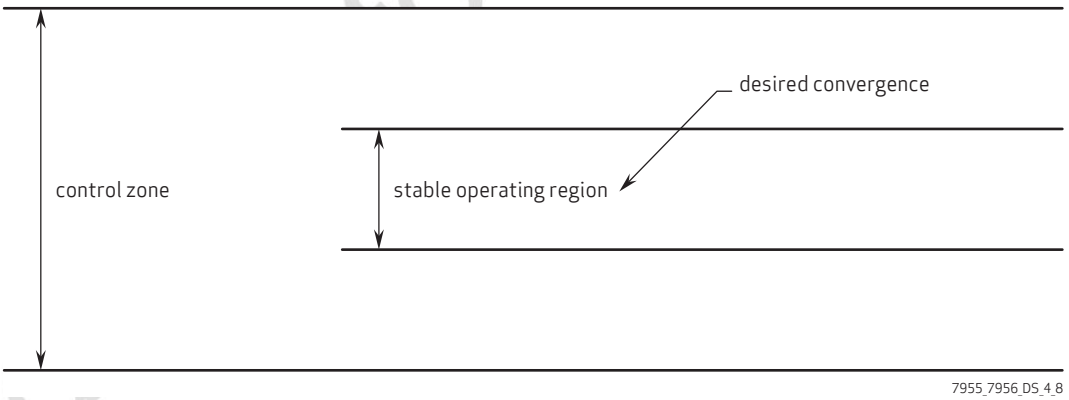
The AEC controls image luminance using registers WPT (0x3A0F) and BPT (0x3A10). The value of register WPT (0x3A0F) indicates the high threshold value and the value of register BPT (0x3A10) indicates the low threshold value. When the target image luminance average value YAVG (0x3A50) is within the range specified by registers WPT (0x3A0F) and BPT (0x3A10), the AEC keeps the image exposure. When register YAVG (0x3A50) is greater than the value in register WPT (0x3A0F), the AEC will decrease the image exposure. When register YAVG (0x3A50) is less than the value in register BPT (0x3A10), the AEC will increase the image exposure. Accordingly, the value in

register WPT (0x3A0F) should be greater than the value in register BPT (0x3A10). The gap between the values of registers WPT (0x3A0F) and BPT (0x3A10) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers WPT (0x3A0F) and BPT (0x3A10). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. A value of '1' in register AEC_CTRL5[5] (0x3A05) will result in normal speed operation and a '0' will result in fast speed operation.

Register VPT_LOW (0x3A1F) and VPT_HIGH (0x3A11) control the fast AEC range. If the target image YAVG (0x3A50) is greater than VPT_HIGH (0x3A11), AEC will decrease by step3 (0x3A07[3:0]). If register YAVG (0x3A50) is less than VPT_LOW, AEC will increase by step1 (0x3A06[4:0]); If register YAVG (0x3A50) is between VPT_HIGH (0x3A11) and VPT_LOW (0x3A1F), AEC will increase or decrease by step2 (0x3A07[7:4]).

figure 4-8 desired convergence



control zone upper limit: VPT_HIGH[7:0] (0x3A11)

control zone lower limit: VPT_LOW[7:0] (0x3A1F)

stable operating region upper limit: WPT[7:0] (0x3A0F)

stable operating region lower limit: BPT[7:0] (0x3A10)

table 4-6 AEC/AGC controls

function	register	description
WPT	0x3A0F	upper limit of stable_in operating region - AEC/AGC value stays in this region until it leaves the stable_out region
BPT	0x3A10	lower limit of stable_in operating region
stable_out_upper	0x3A1B	upper limit of stable_out operating region - AEC/AGC value decreases in auto mode when average luminance is greater than stable_out_upper [7:0]
stable_out_lower	0x3A1E	lower limit of stable_out operating region - AEC/AGC value increases in auto mode when average luminance is greater than stable_out_lower [7:0]
VPT_LOW	0x3A1F	fast mode large step range thresholds - effective only in AEC/AGC fast mode AEC may increase by larger step step1 (0x3A06[4:0]) when luminance average is less than VPT_LOW
VPT_HIGH	0x3A11	fast mode large step range thresholds - effective only in AEC/AGC fast mode AEC may decrease by larger step step3 (0x3A07[3:0]) when luminance average is greater than VPT_HIGH
YAVG	0x3A50	luminance average - this register will auto update when Average luminance is calculated from the B/Gb/Gr/R channel average as follows: B/Gb/Gr/R channel average = (BAVG[7:0] + GbAVG[7:0] + GrAVG[7:0] + RAVG[7:0]) × 0.25
AEC update fast speed enable	0x3A05	fast AEC/AGC enable 0: fast 1: standard
AEC update speed1	0x3A06	if register YAVG (0x3A50) is less than VPT_LOW, AEC will increase by step1 (0x3A06[4:0])
AEC update speed2	0x3A07	if register YAVG (0x3A50) is between VPT_HIGH and VPT_LOW, AEC will increase or decrease by step2 (0x3A07[7:4])
AEC update speed3	0x3A07	if the target image YAVG (0x3A50) is greater than VPT_HIGH (0x3A11), AEC will decrease by step3 (0x3A07[3:0])

4.3.2 AVG

The main purposes of the AVG module is to calculate the luminance average.

table 4-7 AVG registers[a] (sheet 1 of 2)

address	register name	default value	R/W	description
0x5900	AVGCTRL00	0x00	RW	Bit[1:0]: xstart_sub[9:8] AVG sub-window horizontal start position high byte
0x5901	AVGCTRL01	0x00	RW	Bit[7:0]: xstart_sub[7:0] AVG sub-window horizontal start position low byte
0x5902	AVGCTRL02	0x00	RW	Bit[1:0]: ystart_sub[9:8] AVG sub-window vertical start position high byte
0x5903	AVGCTRL03	0x00	RW	Bit[7:0]: ystart_sub[7:0] AVG sub-window vertical start position low byte
0x5904	AVGCTRL04	0x02	RW	Bit[1:0]: hsize_sub[9:8] Sub-window width high byte
0x5905	AVGCTRL05	0x90	RW	Bit[7:0]: hsize_sub[7:0] Sub-window width low byte
0x5906	AVGCTRL06	0x01	RW	Bit[1:0]: vsize_sub[9:8] Sub-window height high byte
0x5907	AVGCTRL07	0xEC	RW	Bit[7:0]: vsize_sub[7:0] Sub-window height low byte
0x5908	AVGCTRL08	0x11	RW	Bit[7:4]: weight 01 Weight of zone 01 Bit[3:0]: weight 00 Weight of zone 00
0x5909	AVGCTRL09	0x11	RW	Bit[7:4]: weight 03 Weight of zone 03 Bit[3:0]: weight 02 Weight of zone 02
0x590A	AVGCTRL0A	0x11	RW	Bit[7:4]: weight 11 Weight of zone 11 Bit[3:0]: weight 10 Weight of zone 10
0x590B	AVGCTRL0B	0x11	RW	Bit[7:4]: weight 13 Weight of zone 13 Bit[3:0]: weight 12 Weight of zone 12

table 4-7 AVG registers[a] (sheet 2 of 2)

address	register name	default value	R/W	description
0x590C	AVGCTRL0C	0x11	RW	Bit[7:4]: Weight 21 Weight of zone 21 Bit[3:0]: Weight 20 Weight of zone 20
0x590D	AVGCTRL0D	0x11	RW	Bit[7:4]: Weight 23 Weight of zone 23 Bit[3:0]: Weight 22 Weight of zone 22
0x590E	AVGCTRL0E	0x11	RW	Bit[7:4]: Weight 31 Weight of zone 31 Bit[3:0]: Weight 30 Weight of zone 30
0x590F	AVGCTRL0F	0x11	RW	Bit[7:4]: Weight 33 Weight of zone 33 Bit[3:0]: Weight 32 Weight of zone 32
0x5910	AVGCTRL10	0x02	RW	Bit[1]: sum_opt 0: Sum = (4*B+9*G*2+10*R)/8 1: Sum = B+G*2+R Bit[0]: sub_win_en Sub-window function enable signal
0x5911	AVGROREG0	–	R	Bit[7:0]: Weight_sum Sum of weight
0x5912	AVGROREG1	–	R	Bit[0]: avg_start AVG calculated in dictating signal weight for SCCB read
0x5913	AVGROREG2	–	R	Bit[7:0]: AVG High 8 bits of whole image AVG output

a. refer to the *OmniVision OV7955 Application Note* for details of window locations and settings

4.4 black level calibration (BLC)

The OV7955 black level calibration function compensates the dark current to ensure constant output black level regardless of change in exposure time, gain and temperature.

table 4-8 BLC control functions

function	register	description
BLC enable	0x5001	Bit[5]: blc_en 0: Disable 1: Enable
auto/manual mode	0x4000	Bit[4]: BLC manual mode 0: Auto mode 1: Manual mode
target	{0x4002[1:0], 0x4003}	Black Level to be Achieved

4.5 one-time programmable (OTP) memory

The high density OTP memory of the OV7955 is organized as 1280-bit (OTP) memory electrical fuses with a random access interface. The primary function is to store chip identification and manufacturing information. OTP is organized as 10 banks (0~9) × 16 bytes (0~0F) × 8 bits.

table 4-9 OTP bank addresses and values[a] (sheet 1 of 2)

OTP bank	OTP address	OTP value
bank 0	0x00	OmniVision product code (programmed by OmniVision)
bank 0	0x01	OmniVision product code (programmed by OmniVision)
bank 0	0x02	OmniVision product code (programmed by OmniVision)
bank 0	0x03	OmniVision product code (programmed by OmniVision)
bank 0	0x04	OmniVision product code (programmed by OmniVision)
bank 0	0x05	0xA1 (load flag, programmed by OmniVision)
bank 0	0x06	0x67 (load address, programmed by OmniVision)
bank 0	0x07	0x03 (load address, programmed by OmniVision)
bank 0	0x08	temperature sensor offset value (programmed by OmniVision)
bank 0	0x09	can be programmed by customer if needed
bank 0	0x0A	can be programmed by customer if needed
bank 0	0x0B	can be programmed by customer if needed

table 4-9 OTP bank addresses and values[a] (sheet 2 of 2)

OTP bank	OTP address	OTP value
bank 0	0x0C	can be programmed by customer if needed
bank 0	0x0D	can be programmed by customer if needed
bank 0	0x0E	can be programmed by customer if needed
bank 0	0x0F	can be programmed by customer if needed
...	...	can be programmed by customer if needed
bank 9	0x0E	0xDD (load setting flag, programmed by OmniVision)
bank 9	0x0F	0x05 (start loading register from OTP address 0x05, programmed by OmniVision)

a. refer to *OmniVision Application Note* for details of OTP load setting function

The OTP memory has three operation modes: program, read, and inactive. The OTP is in the inactive mode by default. OTP write/read is bank based and register 0x3D84[5:0] is the bank selecting. When 0x3D80 is set to 0x01, the OTP enters program mode, and data in OTP registers (0x3D00~0x3D0F) are sequentially burned into the OTP. When 0x3D81 is set to 0x01, the OTP enters read mode, and data in OTP is read out and loaded into OTP registers (0x3D00~0x3D0F). OTP function summarizes the corresponding control and data registers.

The OV7955 also supports OTP load setting when powered up. Also, manual loading is register controlled in normal situations. There are 160 bytes that can be programmed in the chip through the OTP. **figure 4-9** show the memory structure.

figure 4-9 OTP memory structure

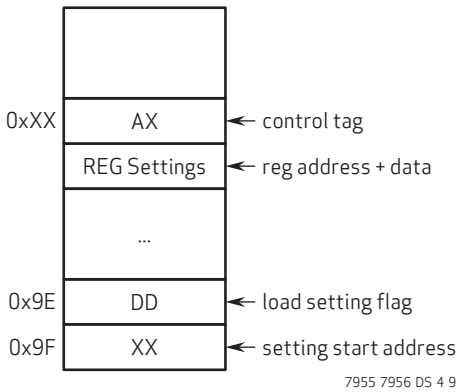


figure 4-9 shows that the data in address 0x9E should be 0xDD as a head byte; otherwise, OTP will not load any settings when powered up. Data in address 0x9F is used for the start address of the stored settings. The register address is 16 bits and the data is 8 bits. The OV7955 supports two setting types:

- Type 1 is: Control TAG (0xAX) + 16 bit address + data (i.e., 0xAX address_high_byte address_low_byte data1.... dataX)
- Type 2 is: Control TAG (0x5X) + data (i.e., 0x5X data1.... dataX)

For example:

byte 0	byte 1	byte 2	byte 3	byte 4	byte 5	byte 6	byte 7	byte 8
0xA2	0x30	0x00	0x00	0x11	0x52	0x22	0x33	0x00

- Byte[4:0] is the first group of the setting, write register 0x3000 to 0x00 and register 0x3001 to 0x11
- Byte[7:5] is the second group of the setting, write register 0x3002 to 0x22, register 0x3003 to 0x33
- Byte[8] is the end flag (any non 0x5X and 0xAX control tag means the end of the setting)

table 4-10 OTP control functions (sheet 1 of 2)

function	register	description
OTP_BYTE0	0x3D00	OTP Write/Read buffer 0
OTP_BYTE1	0x3D01	OTP Write/Read buffer 1
OTP_BYTE2	0x3D02	OTP Write/Read Buffer 2
OTP_BYTE3	0x3D03	OTP Write/Read Buffer 3
OTP_BYTE4	0x3D04	OTP Write/Read Buffer 4
OTP_BYTE5	0x3D05	OTP Write/Read Buffer 5
OTP_BYTE6	0x3D06	OTP Write/Read Buffer 6
OTP_BYTE7	0x3D07	OTP Write/Read Buffer 7
OTP_BYTE8	0x3D08	OTP Write/Read Buffer 8
OTP_BYTE9	0x3D09	OTP Write/Read Buffer 9
OTP_BYTE10	0x3D0A	OTP Write/Read Buffer 10
OTP_BYTE11	0x3D0B	OTP Write/Read Buffer 11
OTP_BYTE12	0x3D0C	OTP Write/Read Buffer 12
OTP_BYTE13	0x3D0D	OTP Write/Read Buffer 13
OTP_BYTE14	0x3D0E	OTP Write/Read Buffer 14
OTP_BYTE15	0x3D0F	OTP Write/Read Buffer 15

table 4-10 OTP control functions (sheet 2 of 2)

function	register	description
PGM CTR	0x3D80	Bit[7]: otp_pgenb_o 1 (read only) Program on going Bit[0]: otp_pgm 0: Default 1: Start program (it will turn 0 automatically after programming)
LOAD CTR	0x3D81	Bit[7]: otp_load_o 1 (read only) Load on going Bit[0]: otp_rd (write only) Writing this register will start load data (when written to 1, it will automatically turn to 0)
MODE CTRL	0x3D84	Bit[7]: program_dis 1: Disable Bit[6]: mode_select 0: Automatic 1: Manual Bit[5:0]: Memory select 0x0: Select memory 0 0x1: Select memory 1 0x2: Select memory 2 0x3: Select memory 3 0x4: Select memory 4 0x5: Select memory 5 0x6: Select memory 6 0x7: Select memory 7 0x8: Select memory 8
START ADDRESS	0x3D85	Bit[5:0]: Start address for manual mode
END ADDRESS	0x3D86	Bit[5:0]: End address for manual mode
PS2CS	0x3D87	Bit[7:0]: Debug control
OTP_LD_WR_GAP	0x3D88	Write Register Gap When OTP Load Setting
OTP_LD_CTRL	0x3D89	OTP Load Register Setting Enable

5 image sensor processor digital functions

5.1 ISP general controls

table 5-1 ISP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFD	RW	Bit[7]: cip_en CIP function enable signal 0: Disable the CIP module 1: Enable the CIP module Bit[6]: gamma_en Gamma function enable signal 0: Disable the gamma module 1: Enable the gamma module Bit[5]: awb_en AWB function enable signal 0: Disable the AWB module 1: Enable the AWB module Bit[4]: awbg_en AWB G function enable signal 0: Disable the AWB_gain module 1: Enable the AWB_gain module Bit[3]: bc_en Black DPC function enable signal 0: Disable the black DPC module 1: Enable the black DPC module Bit[2]: wc_en White DPC function enable signal 0: Disable the white DPC module 1: Enable the white DPC module Bit[1]: lenc_en LENC function enable signal 0: Disable the LENC module 1: Enable the LENC module Bit[0]: isp_en ISP functions enable signal (does not include BLC and DGC modules) 0: Disable the ISP module 1: Enable the ISP module

table 5-1 ISP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x77	RW	Bit[6]: dgc_en DGC function enable signal 0: Disable the DGC module 1: Enable the DGC module Bit[5]: blc_en BLC function enable signal 0: Disable the BLC module 1: Enable the BLC module Bit[4]: avg_en AVG function enable signal 0: Disable the AVG module 1: Enable the AVG module Bit[3]: scaleup_en Scale up function enable signal 0: Disable the scale up module 1: Enable the scale up module Bit[2]: sde_en SDE function enable signal 0: Disable the SDE module 1: Enable the SDE module Bit[1]: uv_avg_en UV_AVG function enable signal 0: Disable the UV_AVG module 1: Enable the UV_AVG module Bit[0]: cmx_en CMX function enable signal 0: Disable the CMX module 1: Enable the CMX module

table 5-1 ISP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5080	PRE CTRL00	0x00	RW	Bit[7]: test_en 0: Disable test function 1: Enable test function Bit[6]: rolling_bar_en 0: Disable rolling bar function 1: Enable rolling bar function Bit[5]: transparent_en 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: square_mode 0: Color square 1: Black white square Bit[3:2]: color_bar_style 00: Standard color bar 01: Top bottom darker color bar 10: Right-left darker color bar 11: Bottom top darker color bar Bit[1:0]: test_mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5081	PRE CTRL01	0x41	RW	Bit[6]: win_cut_en 0: Do not cut the redundant pixels 1: cut the redundant pixels Bit[5]: two_lsb_0_en When it is set two LSB of output date are 0 Bit[4]: same_seed_en When this is set, the seed used to generate the random data is same as set in the seed register Bit[3:0]: Seed This is the seed used in generating random data

5.2 lens correction (LENC)

The lens correction (LENC) algorithm compensates for the illumination drop off in the corners due to the lens. Based on the radius of each pixel to the lens, the algorithm calculates a gain for each pixel and then corrects each pixel with the calculated gain to compensate for the light distribution due to the lens curvature.

table 5-2 LENC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5100	RED_X0	0x01	RW	Bit[1:0]: Red center horizontal position (x0)[9:8]
0x5101	RED_X0	0x50	RW	Bit[7:0]: Red center horizontal position (x0)[7:0]
0x5102	RED_Y0	0x00	RW	Bit[1:0]: Red center vertical position (y0)[9:8]
0x5103	RED_Y0	0xF8	RW	Bit[7:0]: Red center vertical position (y0)[7:0]
0x5104	RED_A1	0x22	RW	Bit[6:0]: Red parameter A1
0x5105	RED_A2	0x07	RW	Bit[3:0]: Red parameter A2
0x5106	RED_B1	0xC2	RW	Bit[7:0]: Red parameter B1
0x5107	RED_B2	0x08	RW	Bit[3:0]: Green parameter B2
0x5108	GRN_X0	0x01	RW	Bit[1:0]: Green center horizontal position[9:8]
0x5109	GRN_X0	0x50	RW	Bit[7:0]: Green center horizontal position[7:0]
0x510A	GRN_Y0	0x00	RW	Bit[1:0]: Green center vertical position (y0)[9:8]
0x510B	GRN_Y0	0xF8	RW	Bit[7:0]: Green center vertical position (y0)[7:0]
0x510C	GRN_A1	0x22	RW	Bit[6:0]: Red parameter A1
0x510D	GRN_A2	0x07	RW	Bit[3:0]: Green parameter A2
0x510E	GRN_B1	0xC2	RW	Bit[7:0]: Green parameter B1
0x510F	GRN_B2	0x08	RW	Bit[3:0]: Green parameter B2
0x5110	BLU_X0	0x01	RW	Bit[1:0]: Blue center horizontal position[9:8]
0x5111	BLU_X0	0x50	RW	Bit[7:0]: Blue center horizontal position[7:0]
0x5112	BLU_Y0	0x00	RW	Bit[1:0]: Blue center vertical position (y0)[9:8]
0x5113	BLU_Y0	0xF8	RW	Bit[7:0]: Blue center vertical position (y0)[7:0]
0x5114	BLU_A1	0x22	RW	Bit[6:0]: Blue parameter A1
0x5115	BLU_A2	0x07	RW	Bit[3:0]: Blue parameter A2
0x5116	BLU_B1	0xC2	RW	Bit[7:0]: Blue parameter B1

table 5-2 LENC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5117	BLU_B2	0x08	RW	Bit[3:0]: Blue parameter B2
0x5118	LENC_CTRL00	0x04	RW	Bit[2]: Round enable to generate random round bit Bit[1]: Coefficient manual mode enable Bit[0]: LENC gain coefficient enable
0x5119	LENC_COEF_TH	0x80	RW	Bit[7:0]: LENC coefficient threshold
0x511A	LENC_GAIN_ THRE1	0x06	RW	Bit[6:0]: LENC gain low threshold (T1)
0x511B	LENC_GAIN_ THRE2	0x0C	RW	Bit[6:0]: LENC gain high threshold (T2)
0x511C	COEF_MAN	0x80	RW	Bit[7:0]: Coefficient manual set input

5.3 auto white balance (AWB)

The purpose of the auto white balance (AWB) block is to avoid unrealistic colors so that objects that appear white to the human eye are rendered white in the final image or video. Thus, the AWB makes sure that white is consistent with different color temperatures. This image sensor supports both manual and automatic white balance. There are both simple and advanced AWB methods available. Advanced AWB takes into account the color temperature of the light source, which relates to the relative warmth or coolness of white light and adjusts the R, G, and B gains to make the average R, G, and B values in a gray area the same. With simple AWB, the gains are adjusted to make the average R, G, and B values in the scene the same.

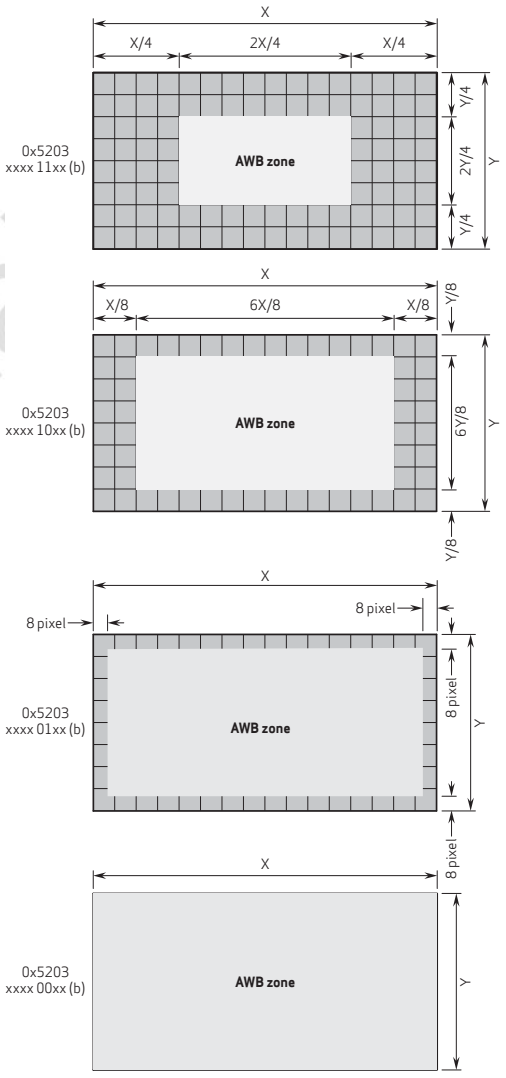
table 5-3 AWB registers

address	register name	default value	R/W	description
0x5200	AWB_CTRL0	0xFF	RW	Bit[7:0]: awb_b_block
0x5201	AWB_CTRL1	0x58	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x Bit[2]: slop_4x Bit[1]: one_zone Bit[0]: avg_all
0x5202	AWB_CTRL2	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x5203	AWB_CTRL3	0x90	RW	Bit[7]: AWB mode select 0: Advanced 1: Simple

5.3.1 AWB region of interest

Both simple and advanced AWB calculations are based on data from the color pixels. By default, all imaging pixels in the array are used for this calculation. However, there may be applications where it is advantageous to ignore pixels around the periphery of the imager. Those applications include those with large FOV lenses (180 degrees, for example) or with a known object in the FOV, like a car bumper, that should be ignored. In those cases, a smaller region of interest (ROI) can be selected within the imager for the AWB calculations.

figure 5-1 AWB region of interest diagram



note 1 AWB all zone equals ISP input size: 648x488

7955_7956_DS_5_1

5.4 gamma

Gamma correction converts the linear response data of the image sensor to compensate for properties of human vision. It maximizes the use of digital data relative to how humans perceive light and color. Higher gain is added at low light levels and lower gain at higher light levels. This non-linear function can be described by the power function, whose exponent value is called gamma. This module is designed to implement the gamma curve correction in piece-wise linear segments.

- gamma correction is performed in the RAW domain
- curve is segmented into 15 sections (16 points)
- registers 0x5301~0x530F set Gam1~Gam15
- slope between Yst1, Yst2, etc..., are automatically set when Gam1~Gam15 are defined. The slope between Yst14 and Yst15 is defined as:
  - SLOPE = (256 - GAM15)* 2/3
  - slope can be manually enabled 0x5300[1]
    byte 0: automatic Yst15 slope
    byte 1: manual Yst15 slope
- 0x5310, manual slope value

figure 5-2 gamma curve

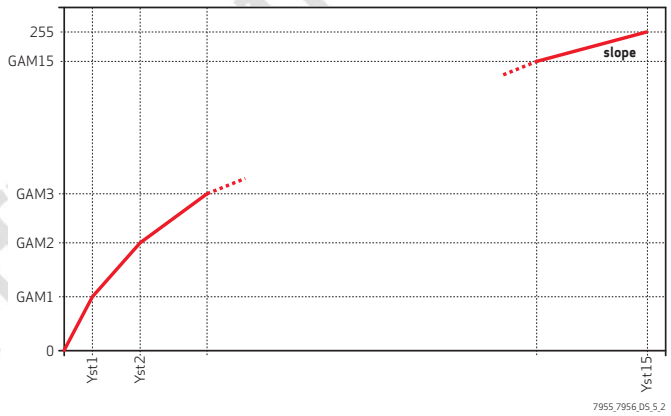


table 5-4 gamma registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5300	GAMMA_CTRL	0x01	RW	Bit[1]: yslp15_man Enable manual set YST15 slope 0: YST15 slope input disable 1: YST15 slope input enable Bit[0]: bias_plus Enable bias 0: Bias disable 1: Bias enable

table 5-4 gamma registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5301	YST1	0x26	RW	Bit[7:0]: Parameter of YST1
0x5302	YST2	0x35	RW	Bit[7:0]: Parameter of YST2
0x5303	YST3	0x48	RW	Bit[7:0]: Parameter of YST3
0x5304	YST4	0x63	RW	Bit[7:0]: Parameter of YST4
0x5305	YST5	0x6E	RW	Bit[7:0]: Parameter of YST5
0x5306	YST6	0x77	RW	Bit[7:0]: Parameter of YST6
0x5307	YST7	0x80	RW	Bit[7:0]: Parameter of YST7
0x5308	YST8	0x88	RW	Bit[7:0]: Parameter of YST8
0x5309	YST9	0x8F	RW	Bit[7:0]: Parameter of YST9
0x530A	YST10	0x96	RW	Bit[7:0]: Parameter of YST10
0x530B	YST11	0xA3	RW	Bit[7:0]: Parameter of YST11
0x530C	YST12	0xAF	RW	Bit[7:0]: Parameter of YST12
0x530D	YST13	0xC5	RW	Bit[7:0]: Parameter of YST13
0x530E	YST14	0xD7	RW	Bit[7:0]: Parameter of YST14
0x530F	YST15	0xE8	RW	Bit[7:0]: Parameter of YST15
0x5310	YSLP15	0x0F	RW	Bit[7:0]: Slope of YST15

5.5 defective pixel cancellation (DPC)

Primarily due to process anomalies, pixel defects in the sensor array will occur, generating incorrect pixel levels and color values. The purpose of the DPC is to remove the effects caused by defective pixels.

table 5-5 DPC registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	1'b1 1'b1	RW	Bit[3]: Black pixel cancellation enable 0: Disable 1: Enable Bit[2]: White pixel cancellation enable 0: Disable 1: Enable

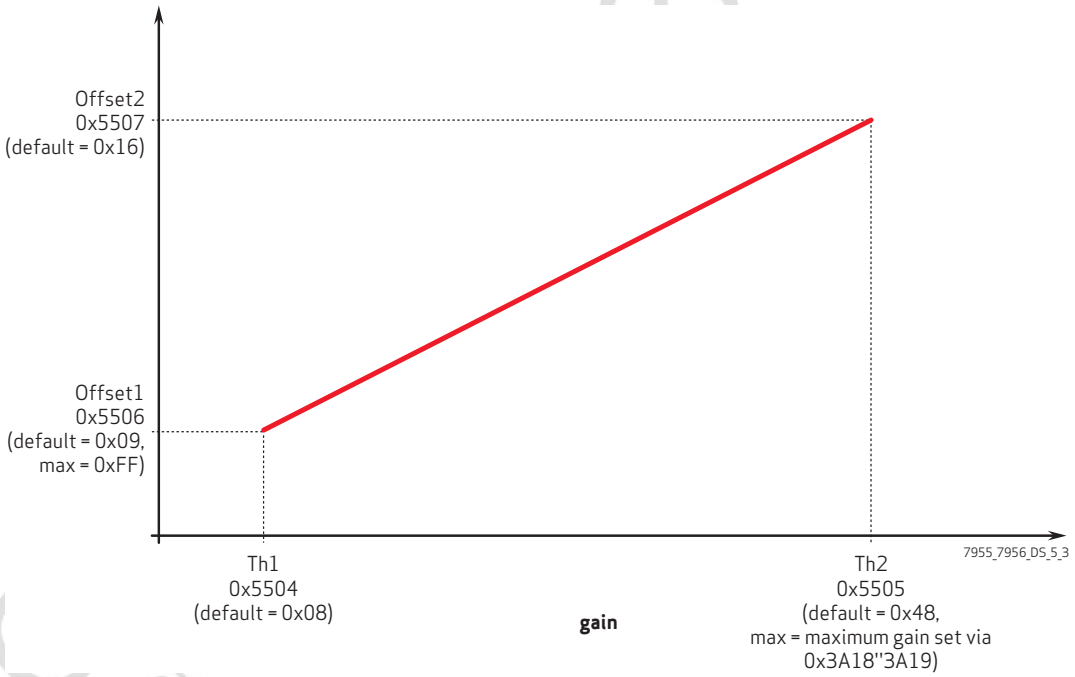
5.6 color interpolation (CIP)

The main function of the color interpolation (CIP) block is to interpolate raw data to YUV data and perform denoise and sharpness. For sharpness, both manual and automatic modes are provided. RAW format is used for the source image data, which means only one R, G, or B is used for each pixel. CIP needs to get the other two color values by calculating them from the neighboring pixels to get the full RGB information for each pixel.

5.6.1 denoise adjustment

- de-noise is set in Y domain in CIP block
- control registers: 0x5504~0x5507
- turn off by setting the offsets to 0x00

figure 5-3 denoise adjustment

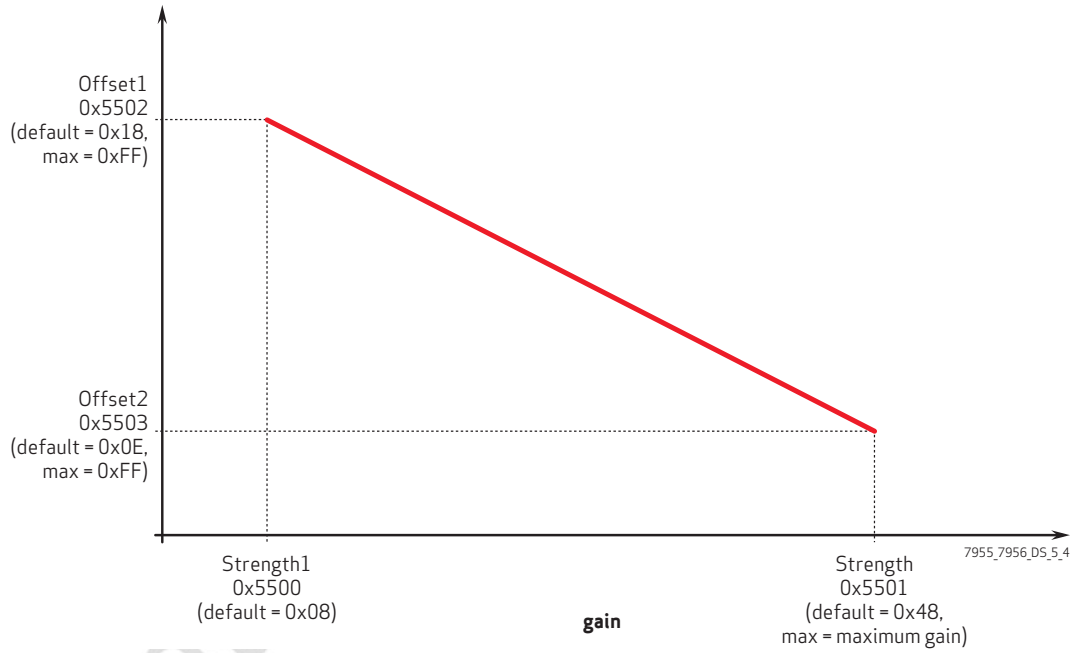


The threshold is normalized by 0x08. For example, if the value is 0x08, the gain where the threshold value will apply is 0x08/0x08 = 1x gain. The offset values are relative. It is recommended that the values are adjusted by the user to suit their needs.

5.6.2 sharpness adjustment

- 0x5500~0x5501: sharpness strength based on gain
- 0x5502~0x5503: sharpness strength offset
- turn off by setting the offsets to 0x00

figure 5-4 sharpness adjustment



The strength is normalized by 0x08. For example, if the value is 0x08, the gain where the threshold value will be applied is 0x08/0x08= 1x gain. The offset values are relative. It is recommended that the values are adjusted by the user to suit their needs.

table 5-6 CIP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5500	R_CIP_CTRL0_O	0x08	RW	Bit[7:0]: Sharpen strength low gain
0x5501	R_CIP_CTRL1_O	0x48	RW	Bit[7:0]: Sharpen strength high gain
0x5502	R_CIP_CTRL2_O	0x18	RW	Bit[6:0]: Sharpen strength offset 1
0x5503	R_CIP_CTRL3_O	0x0E	RW	Bit[6:0]: Sharpen strength offset 2
0x5504	R_CIP_CTRL4_O	0x08	RW	Bit[7:0]: Denoise low gain
0x5505	R_CIP_CTRL5_O	0x48	RW	Bit[7:0]: Denoise high gain
0x5506	R_CIP_CTRL6_O	0x09	RW	Bit[6:0]: Denoise offset 1
0x5507	R_CIP_CTRL7_O	0x16	RW	Bit[6:0]: Denoise offset 2

table 5-6 CIP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5508	R_CIP_CTRL8_O	0xAD	RW	Bit[7]: cip_interlace_en Bit[6]: Sharpen manual mode Bit[5]: Boundary process enable Bit[4]: Denoise manual mode Bit[3]: cip_bw_mode_switch Bit[2:0]: BR sharpen control threshold adjusts the weight of high frequency chroma. The larger threshold, the higher weight. Changing these bits is not recommended
0x5509	R_CIP_CTRL9_O	0x08	RW	Bit[7:0]: Sharpen threshold low gain
0x550A	R_CIP_CTRLA_O	0x48	RW	Bit[7:0]: Sharpen threshold high gain
0x550B	R_CIP_CTRLB_O	0x04	RW	Bit[4:0]: Sharpen threshold offset 1
0x550C	R_CIP_CTRLC_O	0x06	RW	Bit[4:0]: Sharpen threshold offset 2
0x550D	R_CIP_CTRLD_O	–	R	Bit[6:0]: Auto calculate sharpen strength
0x550E	R_CIP_CTRLE_O	–	R	Bit[6:0]: Auto calculated denoise threshold
0x550F	R_CIP_CTRLF_O	–	R	Bit[4:0]: Auto calculated sharpen threshold

5.7 color matrix (CMX)

The main purpose of color matrix (CMX) is converting the image from RGB domain to YUV domain. For a different color temperature, the parameters in the transmitting function will change.

table 5-7 CMX registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5600	R_CMX_CTRL0	0x00	RW	Bit[1]: cmx_precision_s Bit[0]: gb_cbcr
0x5601	R_CMX_CTRL1	0x20	RW	Bit[7:0]: CMX1
0x5602	R_CMX_CTRL2	0x64	RW	Bit[7:0]: CMX2
0x5603	R_CMX_CTRL3	0x08	RW	Bit[7:0]: CMX3
0x5604	R_CMX_CTRL4	0x30	RW	Bit[7:0]: CMX4
0x5605	R_CMX_CTRL5	0x90	RW	Bit[7:0]: CMX5
0x5606	R_CMX_CTRL6	0xC0	RW	Bit[7:0]: CMX6

table 5-7 CMX registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5607	R_CMX_CTRL7	0xA0	RW	Bit[7:0]: CMX7
0x5608	R_CMX_CTRL8	0x98	RW	Bit[7:0]: CMX8
0x5609	R_CMX_CTRL9	0x08	RW	Bit[7:0]: CMX9
0x560A	R_CMX_CTRL10	0x01	RW	Bit[0]: cmxsign[8]
0x560B	R_CMX_CTRL11	0x98	RW	Bit[7:0]: cmxsign[7:0]

5.8 special digital effect (SDE)

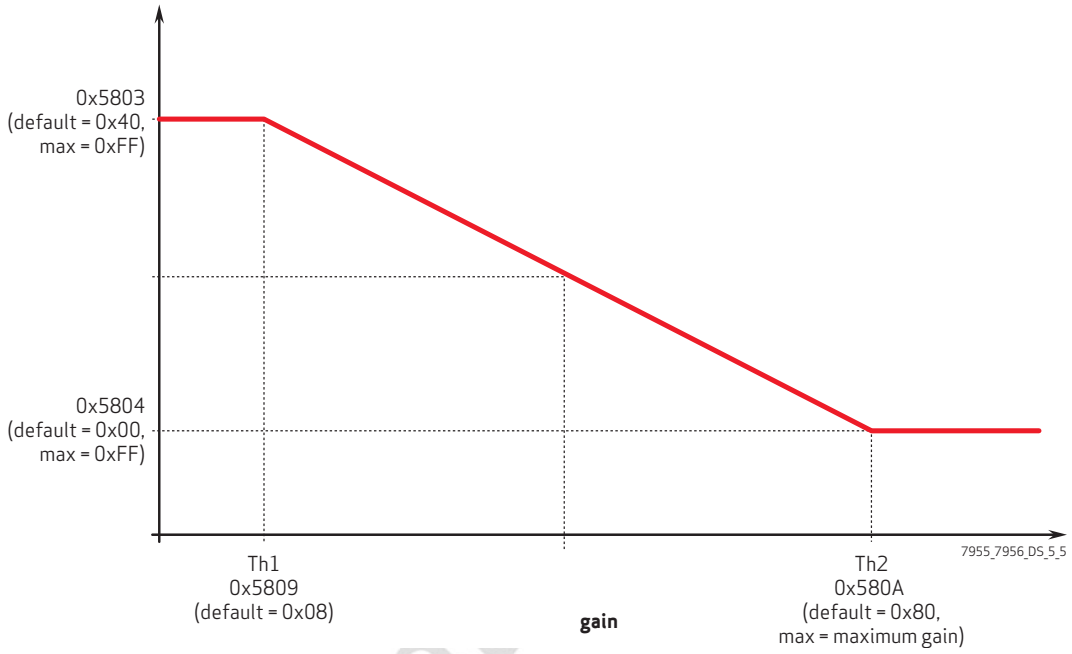
The main purpose of special digital effects (SDE) is special effects such as modified hue/saturation, negative image, B&W mode, etc. Use SDE_Ctrl for the following effects:

- calculate the new U and V based on Hue Cos, Hue Sin and sign of the parameters; if the hue angle is enabled, calculation will be based on hue angle
- set U and V to be fixed values
- UV adjustment
- calculate Y from Y offset, Y gain, and Y bright
- set Y to be a fixed value
- invert Y, U, and V values to get a negative image
- fixed U and V to 128 (8-bit data) resulting in a gray image

5.8.1 UV (saturation) adjustment

- saturation decreases based on gain
- 0x5800[1]: UV adjust enable
- Registers: 0x5803~0x5804 and 0x5809~0x580A
- disable by setting 0x5803, 0x5804 to 0x00

figure 5-5 UV (saturation) adjustment



The threshold is normalized by 0x40. For example, if the value is 0x40, the gain where the threshold value will apply is 0x40/0x40 =1x gain. The offset values are relative. It is recommended that the values are adjusted by the user to suit their needs.

5.8.2 contrast adjustment

- 0x5800[2]: contrast enable
- 0x5805: Yoffset
- 0x5806: Ygain
- 0x5807: Ybright
- 0x5808[2][3]
  [2]: Sign_yoffset
  [3]: Sign_ybright

$Y_{out} = [Y_{in} + (1-2*sign_{ybright})*ybright + (2*sign_{yoffset} - 1)* yoffset)]*ygain + (1-2*sign_{yoffset})*yoffset$

table 5-8 SDE registers

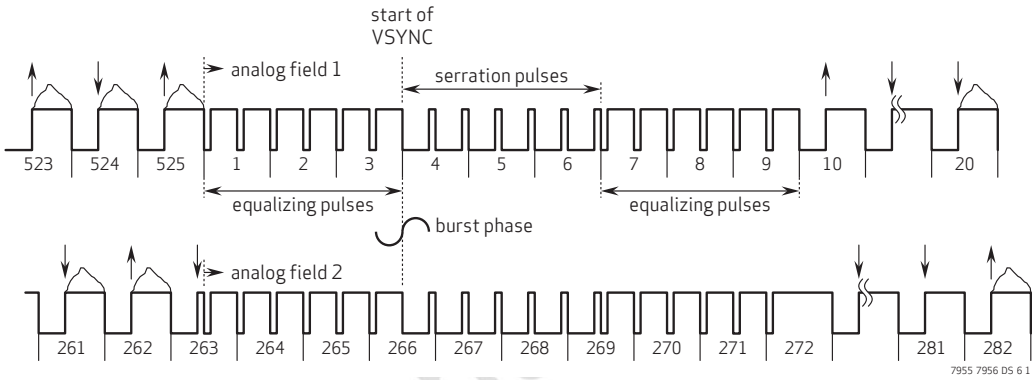
address	register name	default value	R/W	description
0x5800	R_SDE_CTRL0	0x02	RW	Bit[7]: Fixed Y enable Bit[6]: Negative enable Bit[5]: Gray enable Bit[4]: Fixed V enable Bit[3]: Fixed U enable Bit[2]: Contrast enable Bit[1]: Saturation enable Bit[0]: Hue enable
0x5801	R_SDE_CTRL1	0x80	RW	Bit[7:0]: hue_cos
0x5802	R_SDE_CTRL2	0x00	RW	Bit[7:0]: hue_sin
0x5803	R_SDE_CTRL3	0x40	RW	Bit[7:0]: sat_1 UV saturation coefficient for 0x5809
0x5804	R_SDE_CTRL4	0x20	RW	Bit[7:0]: sat_2 UV saturation coefficient for 0x580A
0x5805	R_SDE_CTRL5	0x75	RW	Bit[7:0]: Y offset or fixed Y
0x5806	R_SDE_CTRL6	0x20	RW	Bit[7:0]: Y gain
0x5807	R_SDE_CTRL7	0x00	RW	Bit[7:0]: Y bright
0x5808	R_SDE_CTRL8	0x00	RW	Bit[5:0]: Sign set
0x5809	R_SDE_CTRL9	0x08	RW	Bit[7:0]: uvadj_th1 UV adjust threshold parameter
0x580A	R_SDE_CTRLA	0x80	RW	Bit[7:0]: uvadj_th2 UV adjust threshold parameter
0x580B	R_SDE_CTRLB	0x00	RW	Bit[0]: uvadj_man_en UV adjust value manual enable
0x580C	SDE_R00	–	R	Bit[7:0]: UV adjust manual value

6 image sensor output interface digital functions

6.1 TV mode

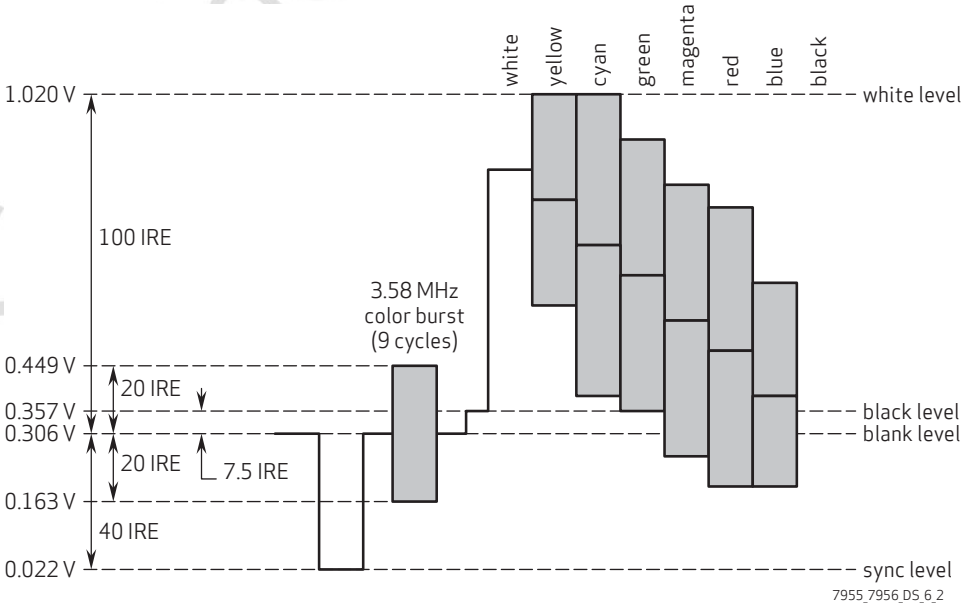
6.1.1 timing diagrams

figure 6-1 NTSC timing diagram



6.1.2 composite video signals

figure 6-2 NTSC composite video signal



6.2 DVP

figure 6-3 DVP timing diagram

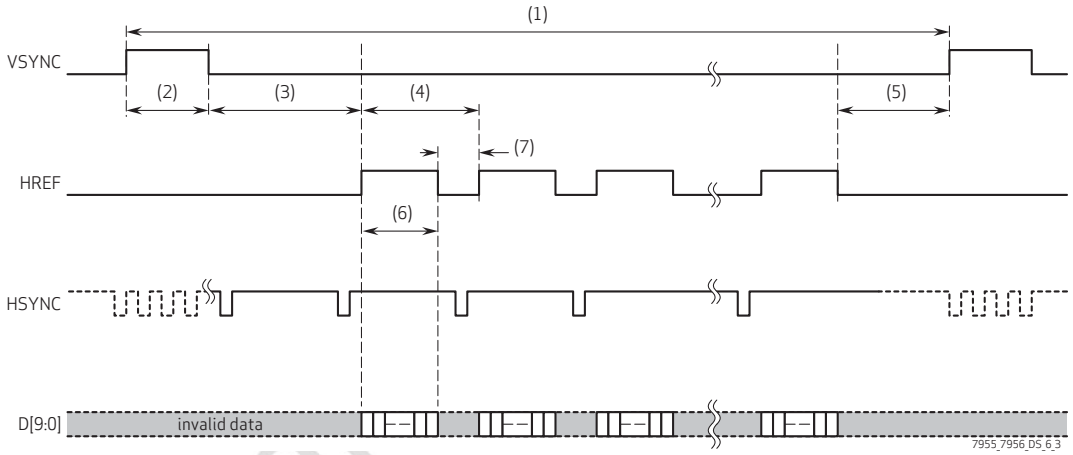


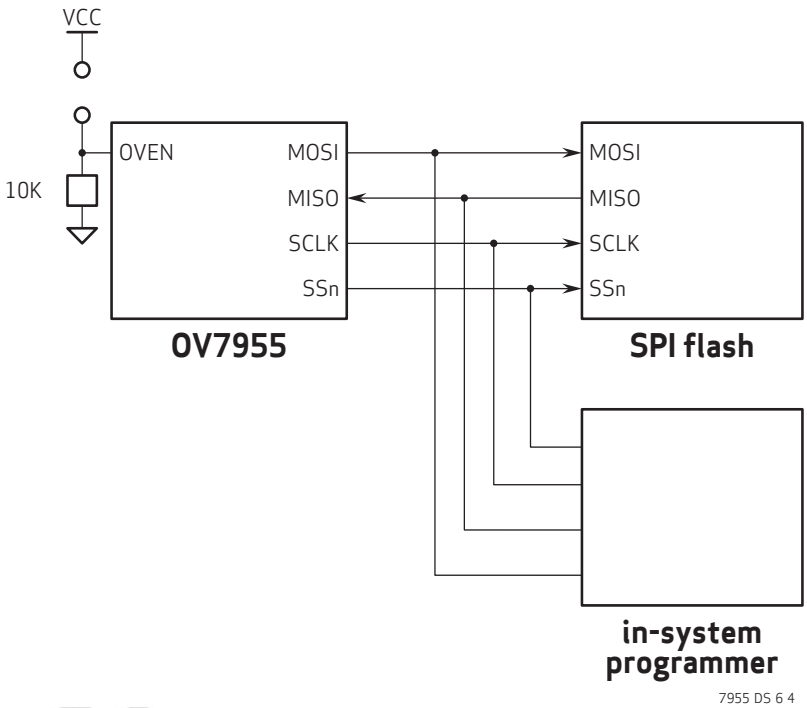
table 6-1 DVP timing specification

mode	timing	
VGA 640x480	(1) (2) (3) (4) (5) (6) (7)	409500 tp (780x525) 128 tp 34984 tp 780 tp 128 tp 640 tp 140 tp where tp = SCLK

6.3 overlay

6.3.1 hardware connection

figure 6-4 in-system programmer



On the hardware level, the connection from OV7955 to serial flash is through a standard SPI interface. The OV7955 supports in-system programming of SPI flash. Pull down OVEN pin and all four pins on the SPI port will become inputs; thus, enabling an external downloader to program the flash. They change to tri-state when powered down.

6.3.2 internal overlay structure

The overlay image is read in from SPI flash on a line-by-line, on-demand basis. Once inside, it is decompressed and mixed with pixel data. Up to two overlay images can be mixed in succession to produce the final output.

figure 6-5 overlay channels

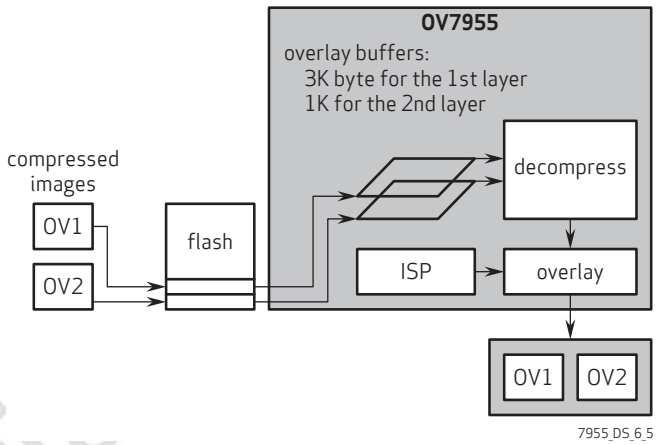
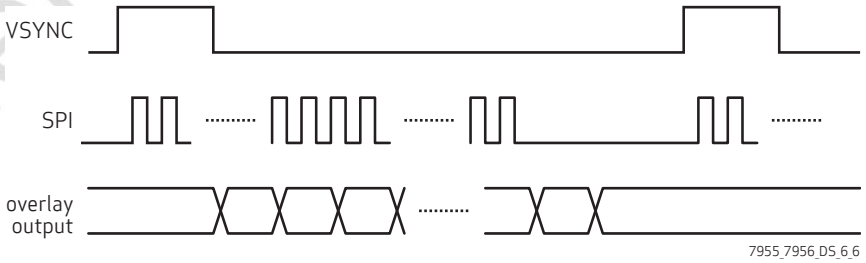


figure 6-6 relative timing



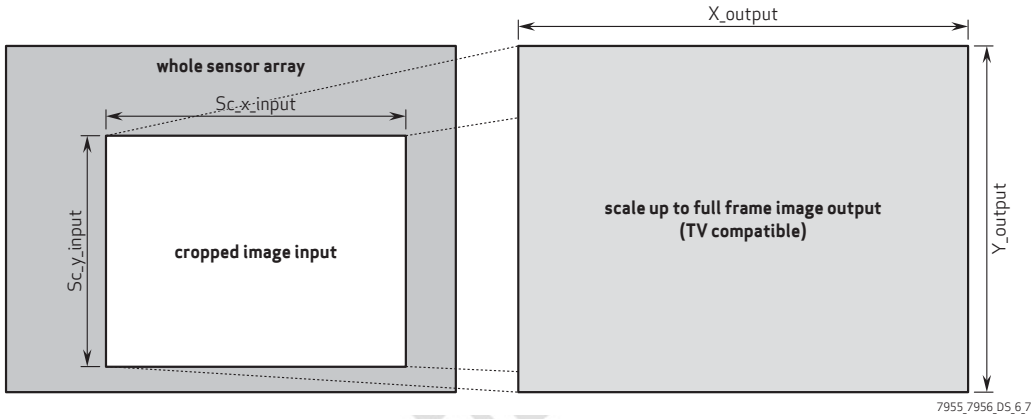
6.3.3 flash memory structure

The memory structure supports bitmap format in B&W. It also supports the storage of register settings. For detailed overlay setting and memory structure, please contact your local OmniVision FAE.

6.4 scale up mode (TV compatible)

The OV7955 supports scale up mode for both TV and DV. It is different from the normal scale up mode since the output data can be compatible with NTSC TV timing.

figure 6-7 scale up mode



When scale up mode is enabled, HTS and VTS will be changed to match SC input image size. There is also a register to define extra_tp to make the full frame rate match the NTSC TV standard. Input size sc_x_input is defined by x_addr_start {0x3800, 0x3801} and x_addr_end {0x3804, 0x3805}, sc_y_input is defined by y_addr_start {0x3802, 0x3803} and y_addr_end {0x3806, 0x3807}. The output size is defined by registers 0x3808 ~ 0x380B. Output data will be a full frame image. Scale-up image input size can be any size between 80% ~ 100% of the whole sensor array size.

Please refer to the *OV7955 Scale and Crop Application Note* to generate register settings for the desired output size.

table 6-2 resolution related registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[1:0]: x_addr_start[9:8] Array horizontal start point high byte
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point low byte
0x3802	Y ADDR START	0x00	RW	Bit[1:0]: y_addr_start[9:8] Array vertical start point high byte
0x3803	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point low byte
0x3804	X ADDR END	0x02	RW	Bit[1:0]: x_addr_end[9:8] Array horizontal end point high byte

table 6-2 resolution related registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3805	X ADDR END	0x9F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point low byte
0x3806	Y ADDR END	0x01	RW	Bit[1:0]: y_addr_end[9:8] Array vertical end point high byte
0x3807	Y ADDR END	0xEB	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point low byte
0x3808	XOUTPUT SIZE	0x02	RW	Bit[7:0]: x_output_size[15:8] MSB of the image data output width from the sensor
0x3809	XOUTPUT SIZE	0x88	RW	Bit[7:0]: x_output_size[7:0] LSB of the image data output width from the sensor
0x380A	YOUTPUT SIZE	0x01	RW	Bit[7:0]: y_output_size[15:8] MSB of the image data output height from the sensor
0x380B	YOUTPUT SIZE	0xE8	RW	Bit[7:0]: y_output_size[7:0] LSB of the image data output height from the sensor
0x3820	FORMAT2	0x00	RW	Bit[4]: scaleup_en Scale up mode enable
0x3829	HTS SU	0x03	RW	Bit[5:0]: hts_su[13:8] High byte of total horizontal timing size for scale up
0x382A	HTS SU	0x0C	RW	Bit[7:0]: hts_su[7:0] Low byte of total horizontal timing size for scale up
0x382B	VTS SU	0x02	RW	Bit[5:0]: vts_su[13:8] High byte of total vertical timing size for scale up
0x382C	VTS SU	0x0D	RW	Bit[7:0]: vts_su[7:0] Low byte of total vertical timing size for scale up
0x382D	EXT TP	0x00	RW	Bit[5:0]: ext_tp[13:8] High byte of extra tp for scale up mode
0x382E	EXT TP	0x01	RW	Bit[7:0]: ext_tp[7:0] Low byte of extra tp for scale up mode

7 register tables

The following tables provides a description of the device control registers contained in the OV7955. The device slave addresses are 0x80 for write and 0x81 for read.

7.1 system control [0x0100 - 0x3043]

table 7-1 system control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x0100	STREAMING_CTRL	0x01	RW	Bit[7:1]: Debug mode Bit[0]: Streaming enable 0: software_standby 1: Streaming
0x0103	SOFTWARE_RESET	–	W	Bit[7:1]: Debug mode Bit[0]: software_reset
0x3000	PAD OEN0	0x00	RW	Bit[7:5]: Debug mode Bit[4]: io_fsin_oen FSIN pin output/input switch 0: Input 1: Output Bit[3]: io_sda_oen SIOD pin output/input switch 0: Input 1: Output Bit[2]: io_href_oen HREF pin output/input switch 0: Input 1: Output Bit[1]: io_vsync_oen VSYNC pin output/input switch 0: Input 1: Output Bit[0]: io_pclk_oen PCLK pin output/input switch 0: Input 1: Output
0x3001	PAD OEN1	0x00	RW	Bit[7:0]: io_y_oen[7:0] Data pin output/input switch 0: Input 1: Output
0x3002	DEBUG MODE	–	–	Debug Mode
0x3003	PLL CTRL0	0x1C	RW	Bit[7:5]: pll_cp PLL reference current options Bit[4:0]: pll_multiplier=32~0x3003[4:0]

table 7-1 system control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3004	PLL CTRL1	0x02	RW	Bit[7:4]: Debug mode Bit[3:2]: pll_sdiv System divider of PLL 00: /1 01: /2 10: /3 11: /4 Bit[1:0]: pll_prediv Pre-divider of PLL 00: /1 01: /1.5 10: /2 11: /3
0x3005	NOT USED	–	–	Not Used
0x3006	PLL CTR13	0x0A	RW	Bit[7:6]: Debug mode Bit[5:3]: SDIV Divider for sigma-delta Clock divider for 50/60 auto detection clock Bit[2:0]: Debug mode
0x3007	DEBUG MODE	–	–	Debug Mode
0x3008	PAD OUT0	0x00	RW	Bit[7:5]: Debug mode Bit[4]: io_fsin_o FSIN pin manual output register bit Bit[3]: Reserved Bit[2]: io_href_o HREF pin manual output register bit Bit[1]: io_vsync_o VSYNC pin manual output register bit Bit[0]: io_pclk_o PCLK pin manual output register bit
0x3009	PAD OUT1	0x00	RW	Bit[7:0]: io_y_o[7:0] Data pins manual output register bit
0x300A	CHIP ID	0x79	R	Bit[7:0]: chip_id[23:16]
0x300B	CHIP ID	0x55	R	Bit[7:0]: chip_id[15:8]
0x300C	CHIP ID	0x00	R	Bit[7:0]: chip_id[7:0]
0x300D	PAD OUT2	0x00	RW	Bit[7:0]: Debug mode

table 7-1 system control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x300E	PAD SEL0	0x00	RW	Bit[7:5]: Debug mode Bit[4]: io_fsin_sel FSIN pin output selection 0: fsin_o 1: Manual FSIN pin output (0x3008[4]) Bit[3]: Reserved Bit[2]: io_href_sel HREF pin output selection 0: HREF output 1: Manual HREF pin output (0x3008[2]) Bit[1]: io_vsync_sel VSYNC pin output selection 0: VSYNC output 1: Manual VSYNC pin output (0x3008[1]) Bit[0]: io_pclk_sel PCLK pin output selection 0: PCLK output 1: Manual PCLK pin output (0x3008[0])
0x300F	PAD SEL1	0x00	RW	Bit[7:0]: io_y_sel[7:0] Data pins output selection 0: PCLK output 1: Manual PCLK pin output (0x3008[0])
0x3011	PAD	0x02	RW	Bit[7]: a_sleep_en Bit[6:2]: Debug mode Bit[1:0]: pad_drive_cap Data pads, VSYNC, HREF, FSIN pad drive capability options 00: 1x 01: 2x 10: 3x 11: 4x
0x301A~ 0x3043	SYSTEM CONTROL	–	–	System Control Registers Changing these registers is not recommended

7.2 group hold [0x3200 - 0x320F]

table 7-2 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group 0 Start Address in SRAM (actual address is {0x3200[4:0] x16)
0x3201	GROUP ADR1	0x08	RW	Group1 Start Address in SRAM (actual address is {0x3201[4:0] x16)
0x3202	GROUP ADR2	0x10	RW	Group2 Start Address in SRAM (actual address is {0x3202[4:0] x16)
0x3203	GROUP ADR3	0x18	RW	Group3 Start Address in SRAM (actual address is {0x3203[4:0] x16)
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group launch at frame boundary 1110: Group launch immediately others: Debug mode Bit[3:0]: group_id 0000: Group bank0 Default start from address 8'h00 0001: Group bank1 Default start from address 8'h40 0010: Group bank2 Default start from address 8'h80 0011: Group bank3 Default start from address 8'hB0 Others: Debug mode
0x3209	SRAM TEST	0x00	RW	When context_en = 1, frames for staying in grp0 When context_en = 0, Bit[7]: Auto switch back enable Bit[6:5]: Switch back group ID Bit[4:0]: Frames stay in current group

table 7-2 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320A	GRP1 PERIOD	0x00	RW	Bit[7:0]: Frames for staying in grp1
0x320B	GRP SW CTRL	0x01	RW	Bit[7:4]: Debug mode Bit[3]: group_switch_repeat Bit[2]: context_en Bit[1:0]: Second group selection
0x320C	SRAM	0x0F	RW	Bit[7:5]: Debug mode Bit[4]: Test_srm Bit[3:0]: sram_rm
0x320D	GRP ACT	–	R	Bit[7:0]: grp_act Indicates which group is active
0x320E	FRAME CNT GRP0	–	R	Bit[7:0]: frame_cnt_grp0
0x320F	FRAME CNT GRP1	–	R	Bit[7:0]: frame_cnt_grp1

7.3 AEC control [0x3500 - 0x350B]

table 7-3 AEC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	AEC EXPO	0x00	RW	Bit[7:4]: Debug mode Bit[3:0]: Expo[19:16]
0x3501	AEC EXPO	0x02	RW	Bit[7:0]: Expo[15:8]
0x3502	AEC EXPO	0x00	RW	Bit[7:0]: Expo[7:0]

table 7-3 AEC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3503	AEC CTRL0	0x00	RW	Bit[7:6]: Debug mode Bit[5]: Gain delay option 0: 1 frame latch 1: Delay 1 frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[3]: dig_gain_man_en Bit[2]: gain_man_as_gain_snr 0: Manual gain is real gain 1: Manual gain is sensor gain Bit[1]: AGC manual 0: Auto enable 1: Manual enable Bit[0]: AEC manual 0: Auto enable 1: Manual enable
0x350A	AEC GAIN	0x00	RW	Bit[7:3]: Debug mode Bit[2:0]: AGC gain[10:8] When agc_manual is 0, this gain is real gain which is calculated automatically When the gain_man_as_gain_snr and agc_manual are set to 1, the output gain will be sensor gain. Otherwise, the output gain is real gain
0x350B	AEC GAIN	0x10	RW	Bit[7:0]: AGC gain[7:0] When the agc_manual is 0, the gain is real and calculated automatically When the gain_man_as_gain_snr and agc_manual are set to 1, the output gain will be sensor gain. Otherwise, the output gain is real gain.

7.4 analog control [0x3600 - 0x5913]

table 7-4 analog control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3600~ 0x3618	ANALOG CONTROL	–	–	Analog Control Registers Changing these registers is not recommended

table 7-4 analog control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3A00	AEC_CTRL00	0x78	RW	Bit[7]: Debug mode Bit[6]: Enable the function that exposure can be less than 1 line Bit[5]: Enable banding effect remove Bit[4]: Enable the function that exposure can be less than 1 band Bit[3]: eof_sel 0: Select tc_eof_blc_i as start signal 1: Select avg_done_i as start signal Bit[2]: Debug mode Bit[1]: Select new balance method Bit[0]: Enable freeze mode
0x3A01	AEC_CTRL01	0x01	RW	Bit[7:0]: Minimum exposure (set 1, high 4 bits represent integer lines, low 4 bits represent fraction lines)
0x3A02	AEC_CTRL02	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 60Hz (set 1)
0x3A03	AEC_CTRL03	0x06	RW	Bit[7:0]: Minimum exposure for 60Hz (set 1, no fraction lines)
0x3A05	AEC_CTRL05	0x30	RW	Bit[7]: Reverse flag signal of 50/60Hz Bit[6]: Debug mode Bit[5]: Enable automatic step calculation Bit[4:0]: Step ratio in automatic step calculation
0x3A06	AEC_CTRL06	0x10	RW	Bit[7:5]: Debug mode Bit[4:0]: Step 1 in manual step calculation
0x3A07	AEC_CTRL07	0x18	RW	Bit[7:4]: Step 2 in manual step calculation Bit[3:0]: Step 3 in manual step calculation
0x3A08	AEC_CTRL08	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Band step for 50Hz light
0x3A09	AEC_CTRL09	0x39	RW	Bit[7:0]: Band step for 50Hz light
0x3A0A	AEC_CTRL0A	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Band step for 60Hz light
0x3A0B	AEC_CTRL0B	0x05	RW	Bit[7:0]: Band step for 60Hz light
0x3A0C	AEC_CTRL0C	0xE4	RW	Bit[7:4]: Maximum fraction exposure Bit[3:0]: Minimum fraction exposure
0x3A0D	AEC_CTRL0D	0x04	RW	Bit[7:6]: Debug mode Bit[5:0]: Minimum band number in one frame for 60Hz light source

table 7-4 analog control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3A0E	AEC_CTRL0E	0x03	RW	Bit[7:6]: Debug mode Bit[5:0]: Minimum band number in one frame for 50Hz light source
0x3A0F	AEC_CTRL0F	0x78	RW	Bit[7:0]: Upper bound of stable range (set 1)
0x3A10	AEC_CTRL10	0x68	RW	Bit[7:0]: Lower bound of stable range (set 1)
0x3A11	AEC_CTRL11	0xD0	RW	Bit[7:0]: Upper bound of the range to determine step value in manual step calculation
0x3A12	AEC_CTRL12	0x00	RW	Bit[7:0]: Manual average value
0x3A13	AEC_CTRL13	0x90	RW	Bit[7]: Debug mode Bit[6]: Enable pre sensor gain Bit[4]: Value of pre sensor gain Bit[3:0]: Debug mode
0x3A14	AEC_CTRL14	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 50Hz (set 1)
0x3A15	AEC_CTRL15	0x06	RW	Bit[7:0]: Minimum exposure for 50Hz (set 1, no fraction lines)
0x3A17	AEC_CTRL17	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Threshold value of gain_night
0x3A18	AEC_CTRL18	0x01	RW	Bit[7:2]: Reverse Bit[1:0]: Upper bound of output sensor gain[9:8]
0x3A19	AEC_CTRL19	0xF0	RW	Bit[7:0]: Upper bound of output sensor gain[7:0]
0x3A1A	AEC_CTRL1A	0x06	RW	Bit[7:0]: Minimum difference between VTS and max one frame exposure
0x3A1B	AEC_CTRL1B	0x78	RW	Bit[7:0]: Upper bound of stable range (set 2)
0x3A1C	AEC_CTRL1C	0x06	RW	Bit[7:0]: Number of added rows number LED mode
0x3A1D	AEC_CTRL1D	0x18	RW	Bit[7:0]: Number of added rows number LED mode
0x3A1E	AEC_CTRL1E	0x68	RW	Bit[7:0]: Lower bound of stable range (set 2)
0x3A1F	AEC_CTRL1F	0x40	RW	Bit[7:0]: Lower bound of the range to determine step value in manual step calculation

table 7-4 analog control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x3A20	AEC_CTRL20	0x20	RW	Bit[7]: Enable the function of subtracting the black level Bit[6:3]: Black level Bit[2]: Enable strobe option Bit[1]: Enable manual average Bit[0]: Enable the calculation of the case current exposure does not change
0x3A25	AEC_CTRL25	0x00	RW	Bit[7:5]: Debug mode Bit[4:2]: freeze_cnt AEC update once per freeze_cnt frames Bit[1:0]: Debug mode
0x3A26	AEC_CTRL26	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 60Hz (set 2)
0x3A27	AEC_CTRL27	0x06	RW	Bit[7:0]: Minimum exposure for 60Hz (set 2)
0x3A28	AEC_CTRL28	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 50Hz (set 2)
0x3A29	AEC_CTRL29	0x06	RW	Bit[7:0]: Minimum exposure for 50Hz (set 2)
0x3A2A	AEC_CTRL2A	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 60Hz (set 2)
0x3A2B	AEC_CTRL2B	0x06	RW	Bit[7:0]: Minimum exposure for 60Hz (set 2)
0x3A2C	AEC_CTRL2C	0x02	RW	Bit[7:5]: Debug mode Bit[4:0]: Minimum exposure for 50Hz (set 2)
0x3A2D	AEC_CTRL2D	0x06	RW	Bit[7:0]: Minimum exposure for 50Hz (set 2)
0x3A50	AEC_CTRL50	–	R	Bit[7:0]: Average of current frame image
0x3A56~ 0x3A62	DEBUG MODE	–	–	Debug Mode
0x5900	AVGCTRL00	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: xstart_sub[9:8] AVG sub-window horizontal start position high byte
0x5901	AVGCTRL01	0x00	RW	Bit[7:0]: xstart_sub[7:0] AVG sub-window horizontal start position low byte
0x5902	AVGCTRL02	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: ystart_sub[9:8] AVG sub-window vertical start position high byte

table 7-4 analog control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5903	AVGCTRL03	0x00	RW	Bit[7:0]: ystart_sub[7:0] AVG sub-window vertical start position low byte
0x5904	AVGCTRL04	0x02	RW	Bit[7:6]: Debug mode Bit[5:0]: hsize_sub[13:8] Sub-window width high byte
0x5905	AVGCTRL05	0x90	RW	Bit[7:0]: hsize_sub[7:0] Sub-window width low byte
0x5906	AVGCTRL06	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: vsize_sub[9:8] Sub-window height high byte
0x5907	AVGCTRL07	0xEC	RW	Bit[7:0]: vsize_sub[7:0] Sub-window height low byte
0x5908	AVGCTRL08	0x11	RW	Bit[7:4]: weight 01 Weight of zone 01 Bit[3:0]: weight 00 Weight of zone 00
0x5909	AVGCTRL09	0x11	RW	Bit[7:4]: weight 03 Weight of zone 03 Bit[3:0]: weight 02 Weight of zone 02
0x590A	AVGCTRL0A	0x11	RW	Bit[7:4]: weight 11 Weight of zone 11 Bit[3:0]: weight 10 Weight of zone 10
0x590B	AVGCTRL0B	0x11	RW	Bit[7:4]: weight 13 Weight of zone 13 Bit[3:0]: weight 12 Weight of zone 12
0x590C	AVGCTRL0C	0x11	RW	Bit[7:4]: Weight 21 Weight of zone 21 Bit[3:0]: Weight 20 Weight of zone 20
0x590D	AVGCTRL0D	0x11	RW	Bit[7:4]: Weight 23 Weight of zone 23 Bit[3:0]: Weight 22 Weight of zone 22
0x590E	AVGCTRL0E	0x11	RW	Bit[7:4]: Weight 31 Weight of zone 31 Bit[3:0]: Weight 30 Weight of zone 30

table 7-4 analog control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x590F	AVGCTRL0F	0x11	RW	Bit[7:4]: Weight 33 Weight of zone 33 Bit[3:0]: Weight 32 Weight of zone 32
0x5910	AVGCTRL10	0x02	RW	Bit[7:2]: Debug mode Bit[1]: sum_opt 0: Sum = (4×B+9×G×2+10×R)/8 1: Sum = B+G×2+R Bit[0]: sub_win_en Sub-window function enable signal
0x5911	AVGROREG0	–	R	Bit[7:0]: Weight_sum Sum of weight
0x5912	AVGROREG1	–	R	Bit[7:1]: Debug mode Bit[0]: avg_start AVG calculated in dictating signal weight for SCCB read
0x5913	AVGROREG2	–	R	Bit[7:0]: AVG High 8 bits of whole image AVG output

7.5 sensor timing control [0x3700 - 0x3717]

table 7-5 sensor timing control registers

address	register name	default value	R/W	description
0x3700~ 0x3717	SENSOR CONTROL	–	–	Sensor Control Registers Changing these registers is not recommended

7.6 system timing control [0x3800 - 0x383D]

table 7-6 system timing registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3800	XADDRSTART	0x00	RW	Bit[7:5]: Debug mode Bit[1:0]: x_addr_start[9:8] Array horizontal start point high byte

table 7-6 system timing registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3801	XADDRSTART	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point low byte
0x3802	YADDRSTART	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: y_addr_start[9:8] Array vertical start point high byte
0x3803	YADDRSTART	0x00	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point low byte
0x3804	XADDREND	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: x_addr_end[9:8] Array horizontal end point high byte
0x3805	XADDREND	0x9F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point low byte
0x3806	YADDREND	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: y_addr_end[9:8] Array vertical end point high byte
0x3807	YADDREND	0xEB	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point low byte
0x3808	XOUTPUT SIZE	0x02	RW	Bit[7:0]: x_output_size[15:8] MSB of the image data output width from the sensor
0x3809	XOUTPUT SIZE	0x88	RW	Bit[7:0]: x_output_size[7:0] LSB of the image data output width from the sensor
0x380A	YOUTPUT SIZE	0x01	RW	Bit[7:0]: y_output_size[15:8] MSB of the image data output height from the sensor
0x380B	YOUTPUT SIZE	0xE8	RW	Bit[7:0]: y_output_size[7:0] LSB of the image data output height from the sensor
0x380C	HTS	0x03	RW	Bit[7:6]: Debug mode Bit[5:0]: hts[13:8] Total horizontal timing size high byte
0x380D	HTS	0x0C	RW	Bit[7:0]: hts[7:0] Total horizontal timing size low byte
0x380E	VTS	0x02	RW	Bit[7:6]: Debug mode Bit[5:0]: vts[13:8] Total vertical timing size high byte
0x380F	VTS	0x0D	RW	Bit[7:0]: vts[7:0] Total vertical timing size low byte

table 7-6 system timing registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3810~ 0x383D	SYSTEM TIMING CONTROLS	–	–	System Timing Control Registers Changing these registers is not recommended

7.7 OTP control [0x3D00 - 0x3D89]

table 7-7 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D00	OTP_BYTE0	0x00	RW	OTP Write/Read Buffer0
0x3D01	OTP_BYTE1	0x00	RW	OTP Write/Read Buffer1
0x3D02	OTP_BYTE2	0x00	RW	OTP Write/Read Buffer2
0x3D03	OTP_BYTE3	0x00	RW	OTP Write/Read Buffer3
0x3D04	OTP_BYTE4	0x00	RW	OTP Write/Read Buffer4
0x3D05	OTP_BYTE5	0x00	RW	OTP Write/Read Buffer5
0x3D06	OTP_BYTE6	0x00	RW	OTP Write/Read Buffer6
0x3D07	OTP_BYTE7	0x00	RW	OTP Write/Read Buffer7
0x3D08	OTP_BYTE8	0x00	RW	OTP Write/Read Buffer8
0x3D09	OTP_BYTE9	0x00	RW	OTP Write/Read Buffer9
0x3D0A	OTP_BYTE10	0x00	RW	OTP Write/Read Buffer10
0x3D0B	OTP_BYTE11	0x00	RW	OTP Write/Read Buffer11
0x3D0C	OTP_BYTE12	0x00	RW	OTP Write/Read Buffer12
0x3D0D	OTP_BYTE13	0x00	RW	OTP Write/Read Buffer13
0x3D0E	OTP_BYTE14	0x00	RW	OTP Write/Read Buffer14
0x3D0F	OTP_BYTE15	0x00	RW	OTP Write/Read Buffer15
0x3D80	PGM CTR	0x00	RW	Bit[7]: otp_pgenb_o 1 (read only) Program on going Bit[6:1]: Not used Bit[0]: otp_pgm 0: Default 1: Start program (it will turn 0 automatically after programming)

table 7-7 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D81	LOADCTR	–	R	Bit[7]: otp_load_o 1 (read only) Load on going Bit[6:1]: Not used Bit[0]: otp_rd (write only) Writing this register will start load data (when written to 1, it will automatically turn to 0)
0x3D82	PGM PULSE	0x21	RW	Bit[7:0]: Control program strobe pulse by 8 × SCLK
0x3D83	LOAD PULSE	0x02	RW	Bit[3:0]: Control load strobe pulse by SCLK
0x3D84	MODE CTRL	0x40	RW	Bit[7]: program_dis 1: Disable Bit[6]: mode_select 0: Automatic 1: Manual Bit[5:0]: Memory select 0x0: Select memory 0 0x1: Select memory 1 0x2: Select memory 2 0x3: Select memory 3 0x4: Select memory 4 0x5: Select memory 5 0x6: Select memory 6 0x7: Select memory 7 0x8: Select memory 8
0x3D85	START ADDRESS	0x00	RW	Bit[5:0]: Start address for manual mode
0x3D86	END ADDRESS	0x0F	RW	Bit[7:6]: Debug mode Bit[5:0]: End address for manual mode
0x3D87	PS2CS	0x03	RW	Bit[7:0]: Debug mode
0x3D88	OTP_LD_WR_ GAP	0x08	RW	Write Register Gap When OTP Load Setting
0x3D89	OTP_LD_CTRL	0x01	RW	OTP Load Register Setting Enable

7.8 global ADC sync [0x3E00]

table 7-8 global ADC sync register

address	register name	default value	R/W	description
0x3E00	ADC CONTROL	–	–	ADC Control Registers Changing this register is not recommended

7.9 BLC control [0x4000 - 0x4070]

table 7-9 BLC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4000	BLC_CTRL00	0x03	RW	Bit[7]: freeze_en BLC freeze function enable signal When this is set, the BLC freezes. The offsets will keep the pre-frame values Bit[6]: offset_adj_en BLC offset adjust enable 0: Disable 1: Enable Bit[5]: manual_trig Manual trigger signal Its rising edge will trigger BLC Bit[4]: man_offset_en BLC offset value manual enable 0: Disable 1: Enable Bit[3]: black_line_out_en 0: Black line pixels will not be output 1: Black line pixels will be output Bit[2]: always_do BLC always triggers signals when it is set. BLC triggers every frame unless the freeze_en is enabled. Bit[1]: off_smth_en BLC offset smooth enable 0: Disable 1: Enable Bit[0]: median_en 5-point median filter function enable signal 0: Disable 1: Enable

table 7-9 BLC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4001	BLC_CTRL01	0x70	RW	Bit[7]: aec_update_rvs AEC update reversed Bit[6]: format_chg_en Format change trigger function enable signal 0: Disable 1: Enable Bit[5]: gain_chg_en Gain change trigger function enable signal 0: Disable 1: Enable Bit[4]: exp_chg_en Exposure change trigger function enable signal 0: Disable 1: Enable Bit[3:2]: win_sel 00: Full image 01: Windows do not contain the first 16 pixels and the end 16 pixels 10: Windows do not contain the first 1/16 image and the end 1/16 image 11: Windows do not contain the first 1/8 image and the end 1/8 image Bit[1:0]: bypass_mode 00: Bypass data_i after limit bits 01: Bypass data_i[11:0] 1x: Bypass data_i[12:1]
0x4002	TARGET	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: BLC target[9:8]
0x4003	TARGET	0x10	RW	Bit[7:0]: BLC target[7:0]
0x4004~ 0x4070	BLC DEBUG MODE	–	–	BLC Debug Mode Registers Changing these registers is not recommended

7.10 frame control [0x4200 - 0x4203]

table 7-10 frame control registers

address	register name	default value	R/W	description
0x4200~ 0x4203	FRAME DEBUG MODE	–	–	Frame Debug Mode Registers Changing these registers is not recommended

7.11 clip control [0x4300 - 0x4305]

table 7-11 clip control registers

address	register name	default value	R/W	description
0x4300	CLIPMAX	0xFF	RW	Bit[7:0]: Not used
0x4301	CLIPMAX	0xFF	RW	Bit[7:0]: clip_max[7:0] Maximum value of output data
0x4302	CLIPMIN	0x00	RW	Bit[7:0]: Not used
0x4303	CLIPMIN	0x00	RW	Bit[7:0]: clip_min[7:0] Minimum value of output data
0x4304	NOT USED	–	–	Not Used
0x4305	CORE CTRL	0x00	RW	Bit[7:6]: Debug mode Bit[5]: dvp_high8bit 0: DVP output high 8-bit 1: DVP output low 8-bit Bit[4]: Debug mode Bit[3]: sensor_high10bit 0: Original sensor data output 1: Output 2 × sensor data Bit[2]: Debug mode Bit[1]: isp_raw_sel 0: Output[9:2] 1: Output[7:0] Bit[0]: isp_raw enable Enable RAW data mode in ISP

7.12 DVP control [0x4700 - 0x470A]

table 7-12 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	MODSEL	0x04	RW	Bit[7:6]: Debug mode Bit[5]: r_field_inv Field reverse (field for CCIR656 header) Bit[4]: r_field_sel Field selection 0: Fix field signal as ccir_f_value 1: Follow internal field signal for header switch Bit[3]: ccir_v_select Fixed VREF field for CCIR656 Bit[2]: ccir_f_value Fixed field value Bit[1]: ccir656_mode_enable Bit[0]: hsync_mode_enable
0x4701	VSYNC WIDTH	0x00	RW	Bit[7:0]: vsync_width[7:0] VSYNC length by line counter
0x4702	HSYVSYNEG WIDTH	0x01	RW	Bit[7:0]: hsyvsy_neg_width[15:8]
0x4703	HSYVSYNEG WIDTH	0x00	RW	Bit[7:0]: hsyvsy_neg_width[7:0]
0x4704	VSYNCMODE	0x01	RW	Bit[7:4]: Debug mode Bit[3:2]: r_vsyncout_sel Bit[1]: r_vsync3_mod Bit[0]: r_vsync2_mod
0x4705	EOF VSYNC DELAY	0x00	RW	Bit[7:0]: eof_vsync_delay[23:16] SOF/EOF negative edge to VSYNC positive edge high byte
0x4706	EOF VSYNC DELAY	0x01	RW	Bit[7:0]: eof_vsync_delay[15:8] SOF /EOF negative edge to VSYNC positive edge middle byte
0x4707	EOF VSYNC DELAY	0x00	RW	Bit[7:0]: eof_vsync_delay[7:0] SOF /EOF negative edge to VSYNC positive edge low byte

table 7-12 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4708	POL CTRL	0x01	RW	Bit[7:6]: Debug mode Bit[5]: vsync_gate_clk_enable Bit[4]: href_gate_clk_enable Bit[3]: no_frst_for_fifo Bit[2]: href_polarity Bit[1]: vsync_polarity Bit[0]: pclk_polarity/PCLK gate low enable
0x4709	BIT ORDER	0x00	RW	Bit[7]: fifo_bypassmode Bit[6:4]: data_bit_swap Bit[3]: bit_test_mode Bit[2]: bit_test_bit10 Bit[1]: bit_test_bit8 Bit[0]: bit_test_enable
0x470A	BYPSEL	0x00	RW	Bit[7:6]: Not used Bit[5]: HREF selection 0: HSYNC signal from timing control block 1: HSYNC signal is DVP HREF Bit[4:0]: bypass_sel (debug only)

7.13 TV encoder [0x4800 - 0x4820]

table 7-13 TV encoder registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4800	WHITELEVEL	0xC8	RW	Bit[7:0]: Whitelevel[7:0]
0x4801	NORMALLEVEL	0x46	RW	Bit[7:0]: Normallevel[7:0] Normal = black level
0x4802	BLANKLEVEL	0x3C	RW	Bit[7:0]: Blanklevel[7:0] Blank level = 240
0x4803	SYNCLEVEL	0x84	RW	Bit[7]: TV DAC reference enable Bit[6:0]: Sync level[6:0]
0x4804	BURSTLEVEL	0x22	RW	Bit[7:0]: Burst level[7:0] Burst level 112
0x4805	MAXLEVEL	0xFF	RW	Bit[7:0]: Max level[7:0]
0x4806	CHROMASAT	0x7F	RW	Bit[7]: Debug mode Bit[6:0]: Chromasat[6:0] Chroma saturation

table 7-13 TV encoder registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4807	MODSHIFT	0x25	RW	Bit[7:0]: Modshift[23:16]
0x4808	MODSHIFT	0x55	RW	Bit[7:0]: Modshift[15:8]
0x4809	MODSHIFT	0x55	RW	Bit[7:0]: Modshift[7:0]
0x480A	SCUSER	0x80	RW	Bit[7:0]: Scuser Burst phase
0x480B	SCACTNTSC	0x00	RW	Bit[7:0]: Scactntsc[7:0] NTSC sub carrier phase: 0x00
0x480C	RSVD	–	–	Reserved
0x480D	SCH INIT	0x35	RW	Bit[7:0]: sch_init[7:0] Sch initial value
0x480E	LINE PHASE ADJUST SIN	0x02	RW	Bit[7:0]: line_phase_adjust_sin[15:8] NTSC: 0x02
0x480F	LINE PHASE ADJUST COS	0x07	RW	Bit[7:0]: line_phase_adjust_cos[7:0] NTSC: 0x07
0x4810	LINERST	0x00	RW	Bit[7:0]: line_rst[7:0] Line reset value low 8 bits for FSIN
0x4811	COEF Y HIGH	0x41	RW	Bit[7:0]: coef_y_high[7:0] Y coefficient high 8 byte NTSC: 0.644 -> 10'h0101001010
0x4812	COEF U HIGH	0x40	RW	Bit[7:0]: coef_u_high[7:0] U coefficient high 8 byte NTSC: 0.656 -> 8'h0101010000
0x4813	COEF V HIGH	0x5B	RW	Bit[7:0]: coef_v_high[7:0] V coefficient high 8 byte NTSC: 0.656 -> 8'h0101010000
0x4814	COEF YUV LOW	0x08	RW	Bit[7:6]: line_rst_high[9:8] Bit[5:4]: coef_v_low[1:0] Bit[3:2]: coef_u_low[1:0] Bit[1:0]: coef_y_low[1:0]
0x4815	VBLKLEN	0x13	RW	Bit[7:6]: v_rst[9:8] V control reset value high 2 bits for FSIN Bit[5:0]: Vblklen

table 7-13 TV encoder registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4816	COLORBAR	0x10	RW	Bit[7]: Half line option 0: Remove half line at field start 1: Keep half line at field start Bit[6:4]: Color bar option Bit[3]: clk27m Bit[2]: Test mode change SC output as test data Bit[1]: y_offset[0] Set Y bigger than 0x10 or not Bit[0]: Color bar enable
0x4817	FILTER CTRL	0x03	RW	Bit[7:3]: filter_ctrl LP filter control Bit[2:0]: Y delay number
0x4818	HSYNC LEN	0x73	RW	Bit[7:0]: hsync_len[7:0]
0x4819	BURST LEN	0xBE	RW	Bit[7]: Debug mode Bit[6:0]: burst_len[6:0]
0x481A	F PORCH LEN	0x21	RW	Bit[7:6]: Debug mode Bit[5:0]: fporch_len[5:0]
0x481B	B PORCH1 LEN	0xCF	RW	Bit[7:6]: Debug mode Bit[5:0]: bporch1_len[5:0]
0x481C	VRST	0x00	RW	Bit[7:0]: v_rst[7:0] V control reset value low 8 bits for FSIN
0x481D	LINE VRST BW	0x00	RW	Bit[7:6]: Debug mode Bit[5:4]: line_rst_bw[9:8] Line reset value high 2 bits for FSIN Bit[3:2]: Debug mode Bit[1:0]: v_rst_bw[9:8] V control reset value high 2 bits for FSIN
0x481E	LINE RST BW	0x00	RW	Bit[7:0]: line_rst_bw[7:0] Line reset value low 8 bits for FSIN
0x481F	VRST BW	0x00	RW	Bit[7:0]: v_rst_bw[7:0] V control reset value low 8 bits for FSIN
0x4820	TV CTRL20	0x00	RW	Bit[7]: r_no_burst Bit[6]: r_tvsync_en Bit[5:0]: Debug mode

7.14 50Hz, 60Hz auto detection (D5060) control [0x4C00 - 0x4C1E]

table 7-14 D5060 control registers

address	register name	default value	R/W	description
0x4C00	R00	0x00	RW	Bit[7:3]: Reserved Bit[2]: 5060 banding control in manual mode 0: 60 Hz 1: 50 Hz Bit[1:0]: Reserved
0x4C01	R01	0x00	RW	Bit[7]: Auto 5060 detection disable 0: Automatic 1: Manual Bit[6:0]: Reserved
0x4C02~ 0x4C0B	D5060 CONTROL	–	–	D5060 Control Registers Changing these registers is not recommended
0x4C0C	R12	–	R	Bit[7:1]: Reserved Bit[0]: Indicator of 50 Hz or 60 Hz lighting in auto mode 0: 60 Hz 1: 50 Hz
0x4C0D~ 0x4C1E	D5060 CONTROL	–	–	D5060 Control Registers Changing these registers is not recommended

7.15 ISP control [0x5000 - 0x50A5]

table 7-15 ISP registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xFD	RW	Bit[7]: cip_en CIP function enable signal 0: Disable the CIP module 1: Enable the CIP module Bit[6]: gamma_en Gamma function enable signal 0: Disable the gamma module 1: Enable the gamma module Bit[5]: awb_en AWB function enable signal 0: Disable the AWB module 1: Enable the AWB module Bit[4]: awbg_en AWB G function enable signal 0: Disable the AWB_gain module 1: Enable the AWB_gain module Bit[3]: bc_en Black DPC function enable signal 0: Disable the black DPC module 1: Enable the black DPC module Bit[2]: wc_en White DPC function enable signal 0: Disable the white DPC module 1: Enable the white DPC module Bit[1]: lenc_en LENC function enable signal 0: Disable the LENC module 1: Enable the LENC module Bit[0]: isp_en ISP functions enable signal Does not include BLC and DGC modules 0: Disable the ISP module 1: Enable the ISP module

table 7-15 ISP registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x77	RW	Bit[7]: Debug mode Bit[6]: dgc_en DGC function enable signal 0: Disable the DGC module 1: Enable the DGC module Bit[5]: blc_en BLC function enable signal 0: Disable the BLC module 1: Enable the BLC module Bit[4]: avg_en AVG function enable signal 0: Disable the AVG module 1: Enable the AVG module Bit[3]: scaleup_en Scale up function enable signal 0: Disable the scale up module 1: Enable the scale up module Bit[2]: sde_en SDE function enable signal 0: Disable the SDE module 1: Enable the SDE module Bit[1]: uv_avg_en UV_AVG function enable signal 0: Disable the UV_AVG module 1: Enable the UV_AVG module Bit[0]: cmx_en CMX function enable signal 0: Disable the CMX module 1: Enable the CMX module
0x5002~ 0x500E	ISP CTRL	–	–	ISP Control Registers Changing these registers is not recommended

table 7-15 ISP registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5080	PRE CTRL00	0x00	RW	Bit[7]: test_en 0: Disable test function 1: Enable test function Bit[6]: rolling_bar_en 0: Disable rolling bar function 1: Enable rolling bar function Bit[5]: transparent_en 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: square_mode 0: Color square 1: Black white square Bit[3:2]: color_bar_style 00: Standard color bar 01: Top bottom darker color bar 10: Right-left darker color bar 11: Bottom top darker color bar Bit[1:0]: test_mode 00: Color bar 01: Random data 10: Square 11: Black image
0x5081~ 0x50A5	PRE CTRL	–	–	Pre Control Registers Changing these registers is not recommended

7.16 LENC [0x5100 - 0x511C]

table 7-16 LENC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5100	RED_X0	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Red center horizontal position (x0)[9:8]
0x5101	RED_X0	0x50	RW	Bit[7:0]: Red center horizontal position (x0)[7:0]
0x5102	RED_Y0	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Red center vertical position (y0)[9:8]
0x5103	RED_Y0	0xF8	RW	Bit[7:0]: Red center vertical position (y0)[7:0]
0x5104	RED_A1	0x22	RW	Bit[7]: Debug mode Bit[6:0]: Red parameter A1

table 7-16 LENC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5105	RED_A2	0x07	RW	Bit[7:4]: Debug mode Bit[3:0]: Red parameter A2
0x5106	RED_B1	0xC2	RW	Bit[7:0]: Red parameter B1
0x5107	RED_B2	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: Green parameter B2
0x5108	GRN_X0	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Green center horizontal position[9:8]
0x5109	GRN_X0	0x50	RW	Bit[7:0]: Green center horizontal position[7:0]
0x510A	GRN_Y0	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Green center vertical position (y0)[9:8]
0x510B	GRN_Y0	0xF8	RW	Bit[7:0]: Green center vertical position (y0)[7:0]
0x510C	GRN_A1	0x22	RW	Bit[7]: Debug mode Bit[6:0]: Red parameter A1
0x510D	GRN_A2	0x07	RW	Bit[7:4]: Debug mode Bit[3:0]: Green parameter A2
0x510E	GRN_B1	0xC2	RW	Bit[7:0]: Green parameter B1
0x510F	GRN_B2	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: Green parameter B2
0x5110	BLU_X0	0x01	RW	Bit[7:2]: Debug mode Bit[1:0]: Blue center horizontal position[9:8]
0x5111	BLU_X0	0x50	RW	Bit[7:0]: Blue center horizontal position[7:0]
0x5112	BLU_Y0	0x00	RW	Bit[7:2]: Debug mode Bit[1:0]: Blue center vertical position (y0)[9:8]
0x5113	BLU_Y0	0xF8	RW	Bit[7:0]: Blue center vertical position (y0)[7:0]
0x5114	BLU_A1	0x22	RW	Bit[7]: Debug mode Bit[6:0]: Blue parameter A1
0x5115	BLU_A2	0x07	RW	Bit[7:4]: Debug mode Bit[3:0]: Blue parameter A2
0x5116	BLU_B1	0xC2	RW	Bit[7:0]: Blue parameter B1
0x5117	BLU_B2	0x08	RW	Bit[7:4]: Debug mode Bit[3:0]: Blue parameter B2
0x5118	LENC_CTRL00	0x04	RW	Bit[7:3]: Debug mode Bit[2]: Round enable to generate random round bit Bit[1]: Coefficient manual mode enable Bit[0]: LENC gain coefficient enable

table 7-16 LENC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5119	LENC_COEF_TH	0x80	RW	Bit[7:0]: LENC coefficient threshold
0x511A	LENC_GAIN_ THRE1	0x06	RW	Bit[7]: Debug mode Bit[6:0]: LENC gain low threshold (T1)
0x511B	LENC_GAIN_ THRE2	0x0C	RW	Bit[7]: Debug mode Bit[6:0]: LENC gain high threshold (T2)
0x511C	COEF_MAN	0x80	RW	Bit[7:0]: Coefficient manual set input

7.17 AWB control [0x5200 - 0x5250]

table 7-17 AWB registers

address	register name	default value	R/W	description
0x5200	AWB_CTRL0	0xFF	RW	Bit[7:0]: awb_b_block
0x5201	AWB_CTRL1	0x58	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x Bit[2]: slop_4x Bit[1]: one_zone Bit[0]: avg_all
0x5202	AWB_CTRL2	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt
0x5203	AWB_CTRL3	0x90	RW	Bit[7]: AWB mode select 0: Advanced 1: Simple Bit[6:4]: Reserved Bit[3:2]: awb_win AWB ROI registers (see section 5.3) Bit[1:0]: Reserved
0x5204~ 0x5250	AWB_CTRL	–	–	AWB Control Registers Changing these registers is not recommended

7.18 gamma [0x5300 - 0x5310]

table 7-18 gamma registers

address	register name	default value	R/W	description
0x5300	GAMMA_CTRL	0x01	RW	Bit[7:2]: Debug mode Bit[1]: yslp15_man Enable manual set YST15 slope 0: YST15 slope input disable 1: YST15 slope input enable Bit[0]: bias_plus Enable bias 0: Bias disable 1: Bias enable
0x5301	YST1	0x26	RW	Bit[7:0]: Parameter of YST1
0x5302	YST2	0x35	RW	Bit[7:0]: Parameter of YST2
0x5303	YST3	0x48	RW	Bit[7:0]: Parameter of YST3
0x5304	YST4	0x63	RW	Bit[7:0]: Parameter of YST4
0x5305	YST5	0x6E	RW	Bit[7:0]: Parameter of YST5
0x5306	YST6	0x77	RW	Bit[7:0]: Parameter of YST6
0x5307	YST7	0x80	RW	Bit[7:0]: Parameter of YST7
0x5308	YST8	0x88	RW	Bit[7:0]: Parameter of YST8
0x5309	YST9	0x8F	RW	Bit[7:0]: Parameter of YST9
0x530A	YST10	0x96	RW	Bit[7:0]: Parameter of YST10
0x530B	YST11	0xA3	RW	Bit[7:0]: Parameter of YST11
0x530C	YST12	0xAF	RW	Bit[7:0]: Parameter of YST12
0x530D	YST13	0xC5	RW	Bit[7:0]: Parameter of YST13
0x530E	YST14	0xD7	RW	Bit[7:0]: Parameter of YST14
0x530F	YST15	0xE8	RW	Bit[7:0]: Parameter of YST15
0x5310	YSLP15	0x0F	RW	Bit[7:0]: Slope of YST15

7.19 DPC control [0x5400 - 0x541D]

table 7-19 DPC registers

address	register name	default value	R/W	description
0x5400~ 0x541D	DPC CONTROL	–	–	DPC Control Registers Changing these registers is not recommended

7.20 CIP control [0x5500 - 0x550F]

table 7-20 CIP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5500	R_CIP_CTRL0_O	0x08	RW	Bit[7:0]: Sharpen strength low gain
0x5501	R_CIP_CTRL1_O	0x48	RW	Bit[7:0]: Sharpen strength high gain
0x5502	R_CIP_CTRL2_O	0x18	RW	Bit[7]: Debug mode Bit[6:0]: Sharpen strength offset 1
0x5503	R_CIP_CTRL3_O	0x0E	RW	Bit[7]: Debug mode Bit[6:0]: Sharpen strength offset 2
0x5504	R_CIP_CTRL4_O	0x08	RW	Bit[7:0]: Denoise low gain
0x5505	R_CIP_CTRL5_O	0x48	RW	Bit[7:0]: Denoise high gain
0x5506	R_CIP_CTRL6_O	0x09	RW	Bit[6:0]: Denoise offset 1
0x5507	R_CIP_CTRL7_O	0x16	RW	Bit[6:0]: Denoise offset 2
0x5508	R_CIP_CTRL8_O	0xAD	RW	Bit[7]: cip_interlace_en Bit[6]: Sharpen manual mode Bit[5]: Boundary process enable Bit[4]: Denoise manual mode Bit[3]: cip_bw_mode_switch Bit[2:0]: BR sharpen control threshold
0x5509	R_CIP_CTRL9_O	0x08	RW	Bit[7:0]: Sharpen threshold low gain
0x550A	R_CIP_CTRLA_O	0x48	RW	Bit[7:0]: Sharpen threshold high gain
0x550B	R_CIP_CTRLB_O	0x04	RW	Bit[7:5]: Debug mode Bit[4:0]: Sharpen threshold offset 1
0x550C	R_CIP_CTRLC_O	0x06	RW	Bit[7:5]: Debug mode Bit[4:0]: Sharpen threshold offset 2

table 7-20 CIP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x550D	R_CIP_CTRLD_O	–	R	Bit[7]: Debug mode Bit[6:0]: Auto calculate sharpen strength
0x550E	R_CIP_CTRLE_O	–	R	Bit[7]: Debug mode Bit[6:0]: Auto calculated denoise threshold
0x550F	R_CIP_CTRLF_O	–	R	Bit[7:5]: Debug mode Bit[4:0]: Auto calculated sharpen threshold

7.21 CMX control [0x5600 - 0x560B]

table 7-21 CMX registers

address	register name	default value	R/W	description
0x5600	R_CMX_CTRL0	0x00	RW	Bit[7:2]: Debug mode Bit[1]: cmx_precision_s Bit[0]: gb_cbcr
0x5601	R_CMX_CTRL1	0x20	RW	Bit[7:0]: CMX1
0x5602	R_CMX_CTRL2	0x64	RW	Bit[7:0]: CMX2
0x5603	R_CMX_CTRL3	0x08	RW	Bit[7:0]: CMX3
0x5604	R_CMX_CTRL4	0x30	RW	Bit[7:0]: CMX4
0x5605	R_CMX_CTRL5	0x90	RW	Bit[7:0]: CMX5
0x5606	R_CMX_CTRL6	0xC0	RW	Bit[7:0]: CMX6
0x5607	R_CMX_CTRL7	0xA0	RW	Bit[7:0]: CMX7
0x5608	R_CMX_CTRL8	0x98	RW	Bit[7:0]: CMX8
0x5609	R_CMX_CTRL9	0x08	RW	Bit[7:0]: CMX9
0x560A	R_CMX_CTRL10	0x01	RW	Bit[7:1]: Debug mode Bit[0]: Cmxsign[8]
0x560B	R_CMX_CTRL11	0x98	RW	Bit[7:0]: Cmxsign[7:0]

7.22 UV_AVG [0x5700]

table 7-22 UV_AVG register

address	register name	default value	R/W	description
0x5700	R_CTRL00_O	0x00	R/W	Bit[7:1]: Debug mode Bit[0]: median_en 0: Median enable 1: Median disable

7.23 special digital effects (SDE) [0x5800 - 0x580C]

table 7-23 SDE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5800	R_SDE_CTRL0	0x02	RW	Bit[7]: Fixed Y enable Bit[6]: Negative enable Bit[5]: Gray enable Bit[4]: Fixed V enable Bit[3]: Fixed U enable Bit[2]: Contrast enable Bit[1]: Saturation enable Bit[0]: Hue enable
0x5801	R_SDE_CTRL1	0x80	RW	Bit[7:0]: hue_cos
0x5802	R_SDE_CTRL2	0x00	RW	Bit[7:0]: hue_sin
0x5803	R_SDE_CTRL3	0x40	RW	Bit[7:0]: sat_1 UV saturation coefficient for 0x5809
0x5804	R_SDE_CTRL4	0x20	RW	Bit[7:0]: sat_2 UV saturation coefficient for 0x580A
0x5805	R_SDE_CTRL5	0x75	RW	Bit[7:0]: Y offset or fixed Y
0x5806	R_SDE_CTRL6	0x20	RW	Bit[7:0]: Y gain
0x5807	R_SDE_CTRL7	0x00	RW	Bit[7:0]: Y bright
0x5808	R_SDE_CTRL8	0x00	RW	Bit[7:6]: Debug mode Bit[5:0]: Sign set
0x5809	R_SDE_CTRL9	0x08	RW	Bit[7:0]: uvadj_th1 UV adjust threshold parameter
0x580A	R_SDE_CTRLA	0x80	RW	Bit[7:0]: uvadj_th2 UV adjust threshold parameter

table 7-23 SDE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x580B	R_SDE_CTRLB	0x00	RW	Bit[7:1]: Debug mode Bit[0]: uvadj_man_en UV adjust value manual enable
0x580C	SDE_R00	–	R	Bit[7:0]: UV adjust manual value

7.24 window control (WINC) [0x5A00 - 0x5A08]

table 7-24 WINC registers

address	register name	default value	R/W	description
0x5A00~ 0x5A08	WINC CONTROL	–	–	WINC Control Registers Changing these registers is not recommended

7.25 on-screen display (OSD) overlay control [0x6200 - 0x6233]

table 7-25 OSD registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x6200	OSD CTRL00	0x84	RW	Bit[7:6]: SPI address space of EEPROM 00: 1 byte address space of SPI EEPROM 01: 2 byte address space of SPI EEPROM 10: 3 byte address space of SPI EEPROM 11: 4 byte address space of SPI EEPROM Bit[5]: SPI clock debug mode Bit[4:0]: SPI_SPD, SPI clock speed coefficient SPI_clock_frequency = system clock frequency/SPI_SPD if SPI_SPD = 0, SPI_clock_frequency = 2 × system clock frequency

table 7-25 OSD registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x6201	OSD CTRL01	0x02	RW	Bit[7]: Overlay image load mode 0: Load image start from start of frame 1: Load image start from end of frame Bit[6]: Register take effect option 0: Register will take effect in current frame 1: Register will take effect in next frame Bit[5]: Debug mode Bit[4:0]: SPI internal delay adjust SPI internal delay for every command, system clock cycle per unit. Changing these values is not recommended
0x6202	OSD CTRL02	0x3B	RW	Bit[7]: Enable SCCB manual control SPI Bit[6]: Manual drive CSB to low and enable SPI manual output data (register 0x6217) Bit[5]: Fast read enable for SPI EEPROM Bit[4]: SPI read data clock option 0: Use system clock latch SPI input data 1: Use round back SCK to latch SPI input data Bit[3:2]: Debug mode Bit[1]: osd_en Bit[0]: Reserved
0x6203	OSD CTRL03	0x0B	RW	Bit[7:0]: Fast read instruction of SPI EEPROM
0x6204	OSD CTRL04	0x03	RW	Bit[7:0]: Normal read instruction of SPI EEPROM
0x6205	OSD CTRL05	0x01	RW	Bit[7:0]: Overlay picture number[7:0] for layer0
0x6206	OSD CTRL06	0x02	RW	Bit[7:0]: Overlay Picture number[7:0] for layer1
0x6207	OSD CTRL07	–	RW	Bit[7:0]: Not used
0x6208	OSD CTRL08	–	RW	Bit[7:0]: Not used
0x6209	OSD CTRL09	0x00	RW	Bit[7:4]: Not used Bit[3:2]: Overlay picture number[9:8] for layer1 Bit[1:0]: Overlay picture number[9:8] for layer0

table 7-25 OSD registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x620A	OSD CTRL0A	0x01	RW	Bit[7:4]: Not used Bit[3:2]: Resolution for layer 1 00: No overlay 01: 1x1 overlay 1x: Not used Bit[1:0]: Resolution for layer 0 00: No overlay 01: 1x1 overlay 1x: Not used
0x620B	OSD CTRL0B	0x00	RW	Bit[7:0]: Overlay x offset[7:0] for layer0
0x620C	OSD CTRL0C	0x00	RW	Bit[7:0]: Overlay y offset[7:0] for layer0
0x620D	OSD CTRL0D	0x00	RW	Bit[7]: Sign bit of overlay x offset for layer0 Bit[6:4]: Overlay x offset[10:8] for layer0 Bit[3]: Sign bit of overlay y offset for layer0 Bit[2:0]: Overlay y offset[10:8] for layer0
0x620E	OSD CTRL0E	0x00	RW	Overlay X Offset[7:0] for Layer1
0x620F	OSD CTRL0F	0x00	RW	Overlay Y Offset[7:0] for Layer1
0x6210	OSD CTRL10	0x00	RW	Bit[7]: Sign bit of overlay x offset for layer1 Bit[6:4]: Overlay x offset[10:8] for layer1 Bit[3]: Sign bit of overlay y offset for layer1 Bit[2:0]: Overlay y offset[10:8] for layer1
0x6211~ 0x6216	NOT USED	–	–	Not Used
0x6217	OSD CTRL17	0x00	RW	Bit[7:0]: SPI write data SPI will output the written data if 0x6202[7:6]=2'b11
0x6218	OSD CTRL18	0xE4	RW	Bit[7:4]: Not used Bit[3:2]: Layer number for layer position 1 in overlay buffer Bit[1:0]: Layer number for layer position 0 in overlay buffer
0x6219	OSD CTRL19	0x00	RW	Bit[7:0]: Index of load setting file in EEPROM
0x621A	OSD CTRL1A	0x00	RW	Bit[7:6]: Not used Bit[5]: Enable auto Y move mode for layer 1 Bit[4]: Enable auto Y move mode for layer 0 Bit[3:2]: Not used Bit[1]: Enable auto X move mode for layer 1 Bit[0]: Enable auto X move mode for layer 0

table 7-25 OSD registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x621B	OSD CTRL1B	0x00	RW	Bit[7:6]: Not used Bit[5]: Enable auto Y move back for layer1 Bit[4]: Enable auto Y move back for layer0 Bit[3:2]: Not used Bit[1]: Enable auto X move back for layer1 Bit[0]: Enable auto X move back for layer0
0x621C	OSD CTRL1C	0x02	RW	Bit[7:2]: Debug mode Bit[1:0]: Number of attempts for EEPROM load setting at power up 00: Once 01: Twice 10: 4 times 11: 8 times
0x621D	OSD CTRL1D	0xFF	RW	Bit[7:0]: Max load byte number for each layer
0x621E	DEBUG MODE	–	–	Debug Mode
0x621F	OSD CTRL1F	0x04	RW	Bit[7:4]: Layer read options Changing these values is not recommended Bit[3]: Not used Bit[2:0]: Debug timing option Changing these values is not recommended
0x6220	OSD CTRL20	0x00	RW	Bit[7:6]: Not used Bit[5]: Enable auto change round back for layer1 Bit[4]: Enable auto change round back for layer0 Bit[3:2]: Not used Bit[1]: Enable auto change mode for layer1 Bit[0]: Enable auto change mode for layer0
0x6221	OSD CTRL21	0x00	RW	X End Point[7:0] for Layer0 in Auto Move Mode (auto move mode, 0x621A[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN) Start Index[7:0] for Layer0 in Auto Change Mode (auto change mode, 0x6220[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN)
0x6222	OSD CTRL22	0x00	RW	Y End Point[7:0] for Layer0 in Auto Move Mode (auto move mode, 0x621A[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN) End Index[7:0] for Layer0 in Auto Change Mode (auto change mode, 0x6220[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN)

table 7-25 OSD registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x6223	OSD CTRL23	0x00	RW	X End Point[7:0] for Layer1 in Auto Move Mode (auto move mode, 0x621A[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN) Start Index[7:0] for Layer1 in Auto Change Mode (auto change mode, 0x6220[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN)
0x6224	OSD CTRL24	0x00	RW	Y End Point[7:0] for layer1 in Auto Move Mode (auto move mode, 0x621A[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN) End Index[7:0] for Layer1 in Auto Change Mode (auto change mode, 0x6220[4][0]: Layer0 EN, 0x621A[5][1]: Layer1 EN)
0x6229	OSD CTRL29	0x00	RW	Bit[7:6]: Y end point[9:8] for layer1 in auto move mode (auto move mode, 0x621A[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) End index[9:8] for layer1 in auto change mode (auto change mode, 0x6220[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) Bit[5:4]: X end point[9:8] for layer1 in auto move mode (auto move mode, 0x621A[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) Start index[9:8] for layer1 in auto change mode (auto change mode, 0x6220[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) Bit[3:2]: Y end point[9:8] for layer0 in auto move mode (auto move mode, 0x621A[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) End index[9:8] for layer0 in auto change mode (auto change mode, 0x6220[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) Bit[1:0]: X end point[9:8] for layer0 in auto move mode (auto move mode, 0x621A[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN) Start index[9:8] for layer0 in auto change mode (auto change mode, 0x6220[4][0]: layer0 EN, 0x621A[5][1]: layer1 EN)
0x622B	OSD CTRL2B	0x00	RW	Bit[7:0]: Auto change step[7:0]
0x622C	OSD CTRL2C	0x00	RW	Bit[7:0]: Auto change step[15:8]

table 7-25 OSD registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x622D	OSD CTRL2D	0x00	RW	Bit[7:4]: Y auto move step for layer0 Bit[3:0]: X auto move step for layer0
0x622E	OSD CTRL2E	0x00	RW	Bit[7:4]: Y auto move/change step for layer1 Bit[3:0]: X auto move/change step for layer1
0x6230	DEBUG MODE	–	–	Debug Mode
0x6231	OSD CTRL31	–	RW	Bit[7:0]: SPI read data
0x6232	SRAM RM0	0xF7	RW	Bit[7:4]: SRAM1 debug Bit[3:0]: SRAM0 debug
0x6233	SRAM TEST1	0x00	RW	Bit[7:2]: SRAM1 debug Bit[1]: SRAM1 debug Bit[0]: SRAM0 debug

7.26 temperature sensor control [0x6700 - 0x3721]

table 7-26 temperature sensor control registers

address	register name	default value	R/W	description
0x6700~ 0x6721	TEMPERATURE CONTROL	–	–	Temperature Control Registers Changing these registers is not recommended

7.27 DVP FIFO control [0x6800 - 0x6803]

table 7-27 DVP FIFO control registers

address	register name	default value	R/W	description
0x6800~ 0x6803	DVP FIFO	–	–	DVP FIFO Registers Changing these registers is not recommended

8 operating specifications

8.1 absolute maximum ratings

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

8.2 functional temperature

table 8-2 functional temperature

parameter	range
operating temperature[a]	-40°C to +105°C sensor ambient temperature

a. sensor functions in the operating range; however, some image quality changes may be noticed at the temperature extremes.

8.3 DC characteristics

table 8-3 DC characteristics

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current	–	39	55	mA
I_{DD-IO}		–	20	35	mA
$I_{DDS-SCCB}$	standby current[a]	–	1.7	2.4	mA
$I_{DDS-PWDN}$		–	20	50	µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.7V ~ 3.3V)					
V_{IL}	input voltage LOW	–	–	0.3 × DOVDD	V
V_{IH}	input voltage HIGH	0.7 × DOVDD	–	–	V
C_{IN}	input capacitor	–	–	10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	0.9 × DOVDD	–	–	V
V_{OL}	output voltage LOW	–	–	0.1 × DOVDD	V
serial interface inputs					
V_{IL}	SIOC and SIOD	-0.5	0.0	0.3 × DOVDD	V
V_{IH}	SIOC and SIOD	0.7 × DOVDD	DOVDD	DOVDD + 0.5	V

a. test is conducted under room temperature

8.4 AC characteristics

table 8-4 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		24.545452		MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-5 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XI) for NTSC		24.545452		MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

8.5 DAC electrical characteristics

table 8-6 video DAC electrical characteristics single end mode

symbol	parameter	min	typ	max	unit
EXTCLK = 20MHz, VDD = 1.5V, VDD_IO = 3.3V					
resolution			10		bits
DNL			0.2	0.35	bits
INL			0.7	2	bits
output local load	output pad (VOP)		75		Ω
	unused output (VON)		75		Ω
output voltage	single-ended mode, code 000h		0.01		V
	single-ended mode, code 3FFh		1.46		V
output current	single-ended mode, code 000h		2.67		nA
	single-ended mode, code 3FFh		19.4		mA
supply current	estimate		22		mA
DAC_REF	DAC reference		1.2		V
R_DAC_REF	DAC reference		20		KΩ

table 8-7 video DAC electrical characteristics differential mode (sheet 1 of 2)

symbol	parameter	min	typ	max	unit
EXTCLK = 20MHz, VDD = 1.5V, VDD_IO = 3.3V					
DNL			0.2	0.35	bits
INL			0.7	2	bits
output local load	differential mode per pad (VOP and VON)		75		Ω
output voltage	differential mode, code 000h, VOP		0.2		µV
	differential mode, code 000h, VON		1.46		V
	differential mode, code 3FFh, VOP		1.46		V
	differential mode, code 3FFh, VON		0.2		µV

table 8-7 video DAC electrical characteristics differential mode (sheet 2 of 2)

symbol	parameter	min	typ	max	unit
output current	differential mode, code 000h, VOP		2.67		nA
	differential mode, code 000h, VON		19.4		mA
	differential mode, code 3FFh, VOP		19.4		mA
	differential mode, code 3FFh, VON		2.67		nA
differential output, mid level			0.73		V
supply current	estimate		22		mA
DAC_REF	DAC reference		1.2		V
R_DAC_REF	DAC reference		20		KΩ

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

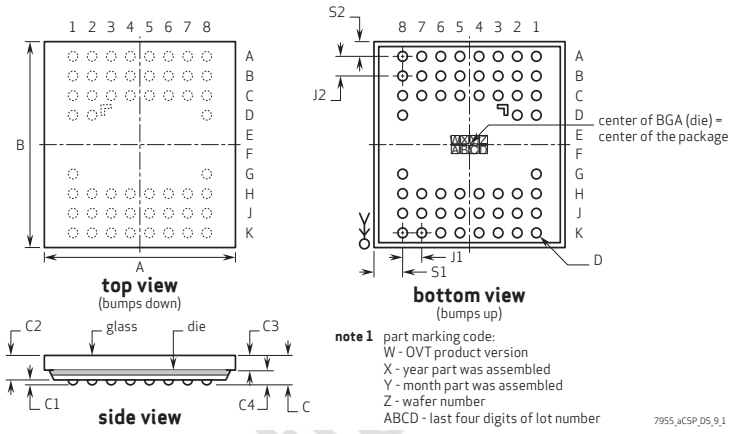
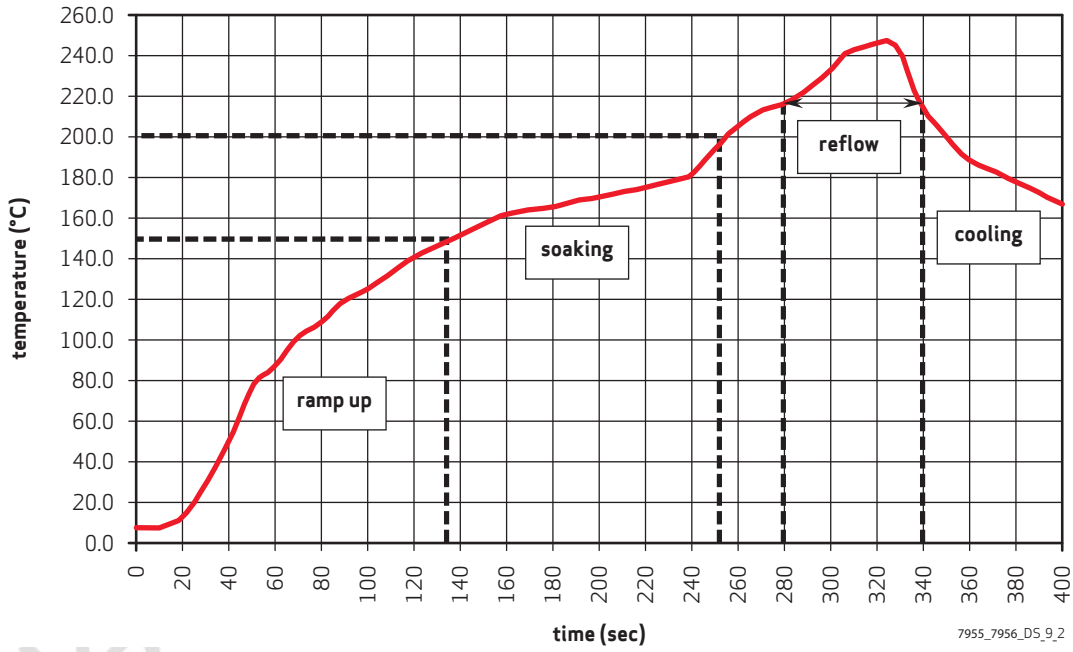


table 9-1 package dimensions

parameter	symbol	min	typ	max	unit
package body dimension x	A	5635	5660	5685	µm
package body dimension y	B	5335	5360	5385	µm
package height	C	690	750	810	µm
ball height	C1	100	130	160	µm
package body thickness	C2	575	620	665	µm
thickness of glass surface to die	C3	425	445	465	µm
image plane height	C4	250	305	360	µm
ball diameter	D	220	250	280	µm
total pin count	N		53 (1 NC)		
pin count x-axis	N1		8		
pin count y-axis	N2		10		
pins pitch x-axis	J1		600		µm
pins pitch y-axis	J2		500		µm
edge-to-pin center distance analog x	S1	700	730	760	µm
edge-to-pin center distance analog y	S2	400	430	460	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note
The OV7955 uses a lead free package.

note
OmniVision recommends under-fill for aCSP

note
To reduce image artifacts from infrared light and to provide the best image quality, OmniVision recommends an IR cut filter

table 9-2 reflow conditions[ab]

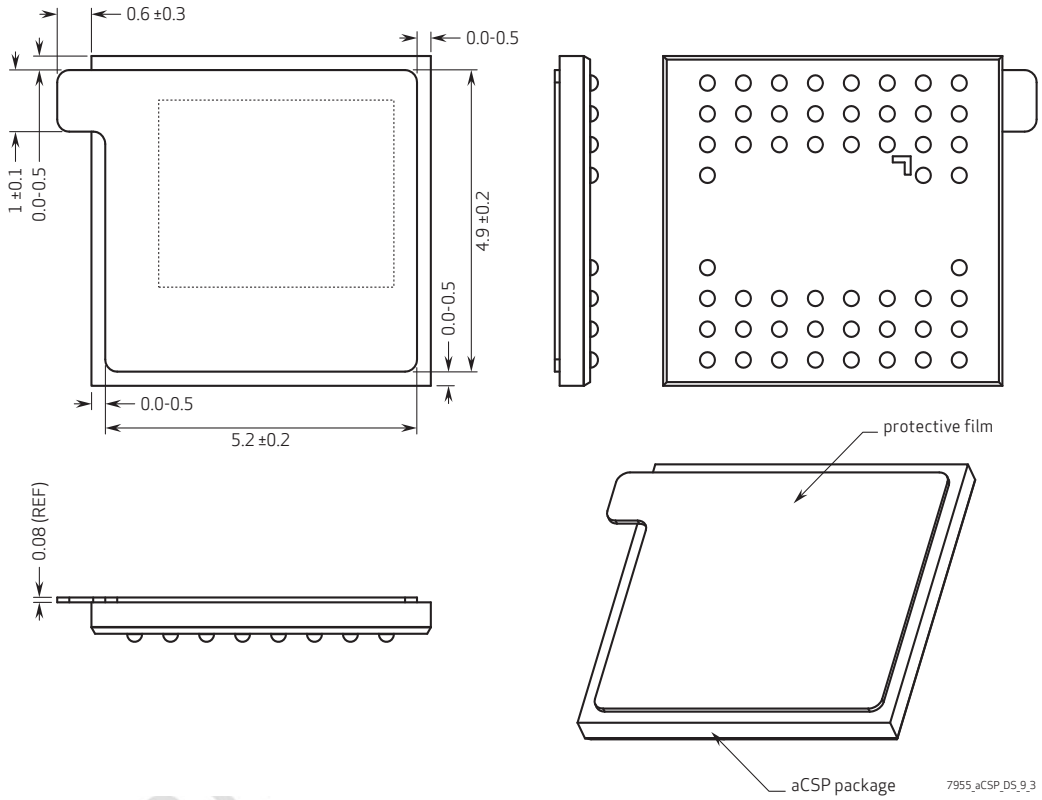
zone	description	exposure
ramp up	heating from room temperature to 150°C	temperature slope ≤ 3°C per second
soaking	heating from 150°C to 200°C	60 ~120 seconds
reflow	temperature higher than 217°C	30 ~120 seconds
peak	maximum temperature in SMT	245°C
cooling	cooling from 217°C to room temperature	temperature slope ≤ 6°C per second

a. maximum number of reflow cycles = 3

b. N2 gas reflow or control O2 gas <500 PPM is recommended

9.3 protective film specifications

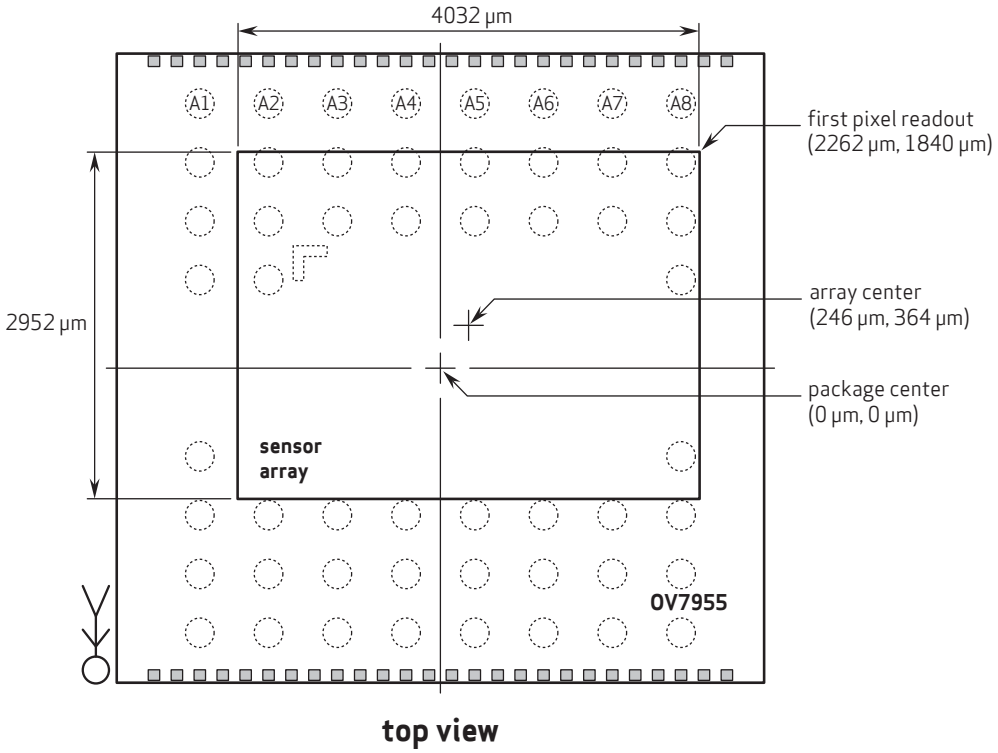
figure 9-3 protective film specifications



10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

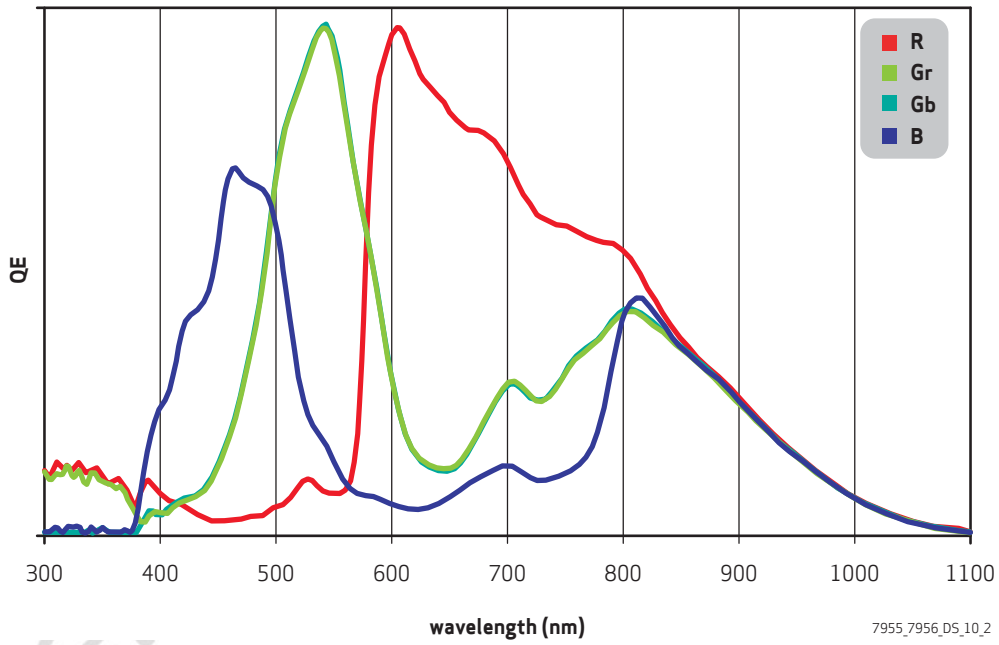
note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin A1 to A8 oriented down on the PCB.

7955_aCSP_DS_10_1

10.2 light response

figure 10-2 light response graph



revision history

version 1.0 06.15.2012

- initial release

version 1.1 07.30.2012

- in sub-section 4.3.1.2, changed "0x3A06[3:0]" to "0x3A06[4:0]" in last sentence of section description
- in table 4-6, changed "0x3A06[3:0]" to "0x3A06[4:0]" in description for VPT LOW and AEC update speed1
- in section 5.3, added sub-section 5.3.1 and new figure 5-1
- in table 7-17, added row for register 0x5203[3:2]

version 2.2 10.05.2012

- changed datasheet from Preliminary Specification to Product Specification
- on page i, under key specifications, changed NTSC optical size from 1/3.6" to "1/3.7" and changed dark current from "16 mV/s @ 50°C..." to "10.7 mV/s @ 50°C..."
- in figure 2-4, changed XVCLK to XI

version 2.21 10.23.2012

- in section 2, updated figures 2-2 and 2-4
- in table 5-3, added register 0x5203
- in table 7-17, added bit description to register 0x5203[7]

defining the future of digital imaging™

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