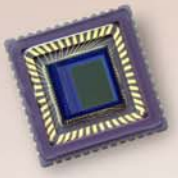
OmniVision™



datasheet

PRELIMINARY SPECIFICATION

CMOS digital / analog NTSC/PAL image sensor
with OmniPixel3-HS™ technology

OV7960/OV7461

CMOS digital / analog NTSC/PAL image sensor with OmniPixel3-HS™ technology

datasheet (CLCC)
PRELIMINARY SPECIFICATION

version 1.11
april 2009

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- security and surveillance cameras
- videoconferencing
- video phones
- video e-mail
- medical equipment
- dental equipment

ordering information

- **OV07960-C48A** (color, lead-free)
  48-pin CLCC
- **OV07461-C48A** (b&w, lead-free)
  48-pin CLCC

features

- NTSC and PAL output
- parallel DVP interface
- high sensitivity
- automatic exposure/gain with 16 zone control
- horizontal and vertical windowing capability
- auto white balance control
- aperture/gamma correction
- external frame sync capability (Genlock)
- slave compatible serial camera control bus (SCCB) control interface for register programming
- low power consumption
- extremely low dark current for high temperature applications
- 50/60 Hz flicker cancellation
- overlay with four layers, 16 colors and eight transparencies each
- 16 bytes of one time programmable memory (OTP) to control overlay and set other customer variables
- SPI master for single static overlay and loading setting
- dynamic overlay controls
- video feedback loop
- defective pixel correction

key specifications

- **active array size:**
  NTSC: 656 x 492
  PAL: 768 x 576
  digital: 752 x 480
- **power supply:**
  core: 1.5V
  analog: 3.3V
  I/O: 1.8 ~ 3.3V
- **power requirements:**
  active: 225 mW
  standby: TBD
- **temperature range:**
  operating: -20°C to +70°C (see **table 8-1**)
  stable image: 0°C to +50°C (see **table 8-1**)
- **optical size:**
  NTSC: 1/4"
  PAL: 1/3"
  VGA: 1/4"
  WVGA: 1/3.2"
- **lens chief ray angle:** 0°
- **output formats:** NTSC/PAL, RAW RGB, RGB565, RGB666, YUV422, CCIR656
- **maximum image transfer rate:**
  NTSC: 60 fields per second
  PAL: 50 fields per second
  WVGA (752x480): 30 frames per second
  VGA (640x480): 30 frames per second
  QVGA (320x240): 60 frames per second
- **sensitivity:** TBD
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **scan mode:** TBD
- **pixel size:** 6.0 µm x 6.0 µm
- **dark current:** TBD
- **image area:** 4752 µm x 3552 µm
- **package dimensions:** 14.22 mm x 14.22 mm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7960/OV7461 image sensor. The package information is shown in **section 9**.

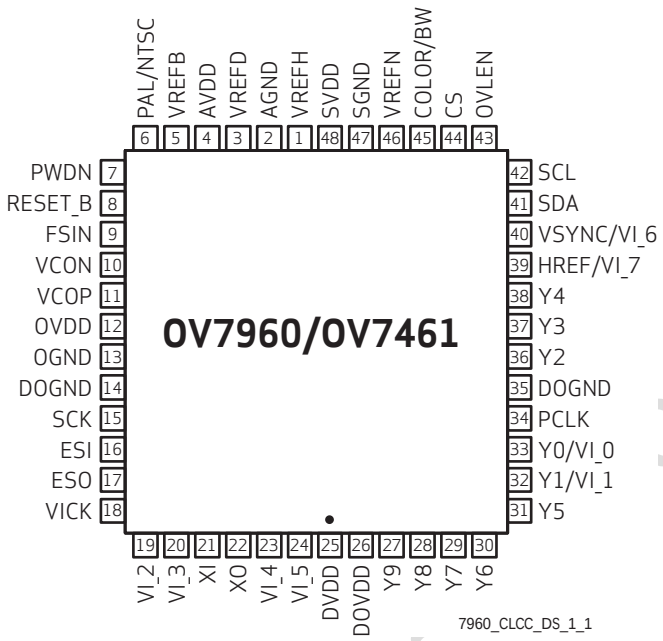
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description
01	VREFH	analog	internal reference
02	AGND	ground	analog ground
03	VREFD	analog	internal reference
04	AVDD	power	3.3V power
05	VREFB	reference	internal reference
06	PAL/NTSC	input	PAL/NTSC switch
07	PWDN	input	power down input with pull-down resistor (active high)
08	RESET_B	input	reset input with pull-up resistor (active low)
09	FSIN	I/O	frame sync signal
10	VCON	output	composite video output negative
11	VCOP	output	composite video output positive
12	OVDD	power	3.3V power
13	OGND	ground	ground
14	DOGND	ground	digital ground
15	SCK	output	SPI clock
16	ESI	input	SPI data input
17	ESO	output	SPI data output
18	VICK	I/O	video input clock
19	VI_2	I/O	video data input[2]
20	VI_3	I/O	video data input[3]
21	XI	input	clock input
22	XO	output	clock output
23	VI_4	I/O	video data input[4]
24	VI_5	I/O	video data input[5]
25	DVDD	power	1.5V power

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description
26	DOVDD	power	1.8~3.3V power
27	Y9	output	video data output[9]
28	Y8	output	video data output[8]
29	Y7	output	video data output[7]
30	Y6	output	video data output[6]
31	Y5	output	video data output[5]
32	Y1/VI_1	I/O	video data output[1] or video data input[1]
33	Y0/VI_0	I/O	video data output[0] or video data input[0]
34	PCLK	I/O	video output clock
35	DOGND	ground	ground
36	Y2	output	video data output[2]
37	Y3	output	video data output[3]
38	Y4	output	video data output[4]
39	HREF/VI_7	I/O	video output horizontal signal or video data input[7]
40	VSYNC/VI_6	I/O	video output vertical signal or video data input[6]
41	SDA	I/O	SCCB interface data pin
42	SCL	input	SCCB interface input clock
43	OVLEN	input	overlay ON/OFF
44	CS	output	SPI chip select
45	COLOR/BW	input	color or black and white switch
46	VREFN	reference	internal reference
47	SGND	power	sensor array ground
48	SVDD	power	3.3V power

figure 1-1 pin diagram



2 system level description

2.1 overview

The OV7960 (color) and OV7461 (b&w) image sensors are low voltage, high performance CMOS image analog sensors that provide the full functionality of a single chip digital / analog NTSC/PAL image sensor using OmniPixel3-HS™ technology in a small footprint package. They provide full-frame images via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7960/OV7461 has an image array capable of operating at 30 frames per second in VGA mode. This product is ideal for applications requiring a small footprint, low voltage, low power and low cost color video camera.

2.2 architecture

The OV7960/OV7461 sensor core generates stream pixel data at a constant frame rate with analog output.

The timing generator outputs signals to access the rows of the image array, pre-charging and sampling the rows of array in series. In the time between pre-charging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light. This is known as exposure time.

The exposure time is controlled by adjusting the time interval between pre-charging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV7960/OV7461 block diagram

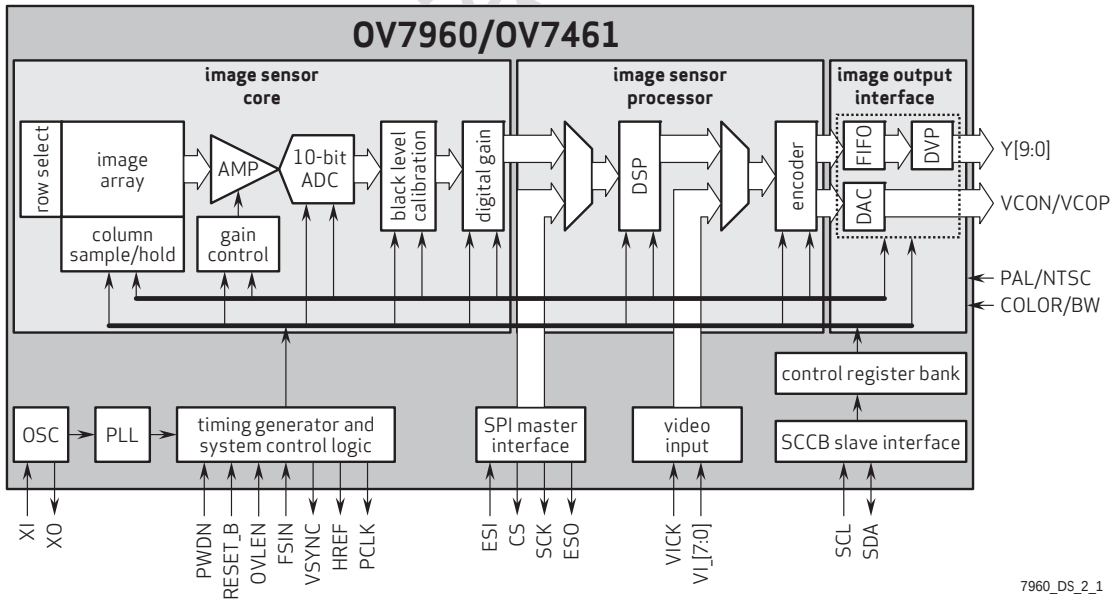
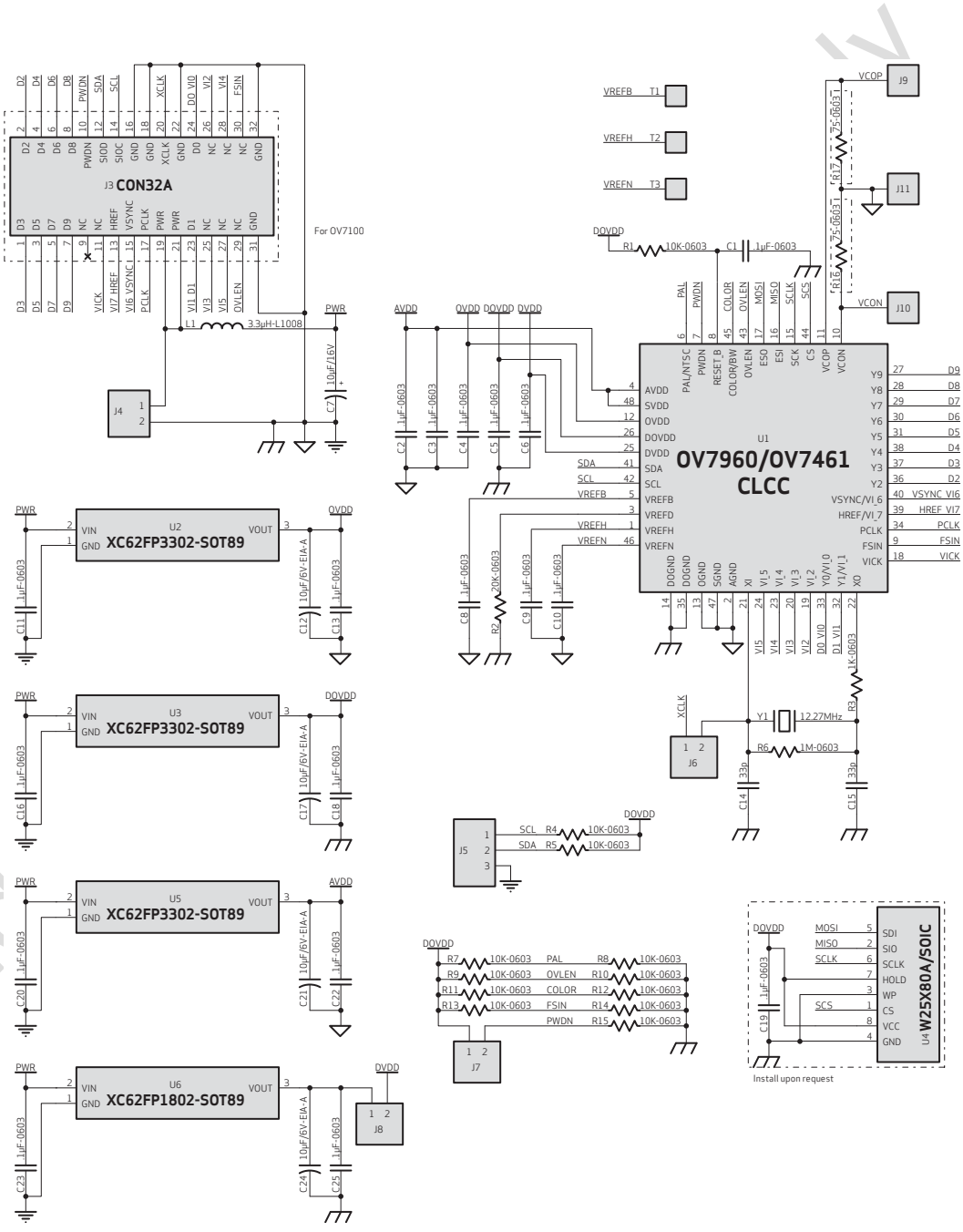


figure 2-2 OV7960/OV7461 reference schematic



2.3 PLL control

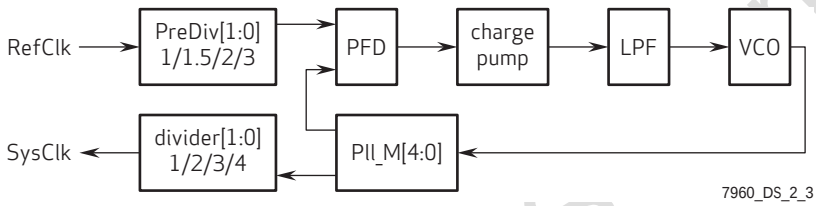
The OV7960/OV7461 PLL allows input clock frequency ranging from 6~27 MHz and has a maximum VCO frequency of 500 MHz. PLLOUT is the input clock for the digital part of the sensor.

Divider[1:0] (0x3095[6:5])00 – /1, 01 – /2, 10 – /2, 11 – /4

PREDIV[1:0] (0x3095[6:5])00 – /1, 01 – /1.5, 10 – /2, 11 – /3

PLLdiv[4:0] (0x3095) is the multiplier parameter: multiplier = (32 - PLLdiv)

figure 2-3 PLL control diagram



2.4 I/O control

The OV7960/OV7461 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pads.

2.4.1 TV output mode (NTSC or PAL)

VCON and VCOP composite video output signals are from DAC.

table 2-1 driving capability and direction control for I/O pads

function	register	description	
DAC power down	0x3052	Bit[2]:	Stops VCON, VCOP output, power down DAC block

2.4.2 DV output mode

Composite video output signals VCON, VCOP are from DAC. In DV output mode, Y[9:0], VSYNC, PCLK and HREF are all output pins.

table 2-2 DV output mode

function	register	description
output capability control	0x300E	Bit[1:0]: output drive capability 00: 1x 01: 2x 10: 3x 11: 4x
Y[9:0] I/O control	0x3093[7:0], 0x3094[1:0]	input/output selections of Y9, Y8…Y0 pins 0: input 1: output
PCLK I/O control	0x3094	Bit[2]: input/output selection of PCLK pin 0: input 1: output
VSYNC I/O control	0x3094	Bit[3]: input/output selection of VSYNC pin 0: input 1: output
HREF I/O control	0x3094	Bit[4]: input/output selection of HREF pin 0: input 1: output

2.5 system control

2.5.1 external components

An external 3.13 ~ 3.47V power supply is used for array power. PAD power can be from 1.7 to 3.47V. 1.5V core power is converted from PAD power by the internal regulator.

The OV7960/OV7461 needs at least three external passive devices to reduce noise. The capacitor value should be at least 0.1µf.

A resistor is required for TV out DAC power reference.

2.5.2 power management

Suspend mode is controlled by the PWDN pin. In suspend mode, the internal clocks are stopped, sensor modules are powered off, and logic control blocks clock input from internal circuitry by logic control. Register values are saved while the sensor is in suspend mode.

Sleep mode can be controlled by register. During sleep mode, the SCCB clock keeps running. Register values can still be accessed while the sensor is in this mode.

In both suspend and sleep modes, the TV output pin state is turned OFF and the 75 ohm termination is connected to GND.

2.5.3 system clock

The on-chip PLL takes 24.545452 MHz (NTSC) or 29.5 MHz (PAL) clock signals from an external crystal. A clock divider can be used to generate a different system frequency.

2.6 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.7 standby and sleep

Two suspend modes are available for the OV7960/OV7461:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7960/OV7461 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

2.8 video feedback mode

2.8.1 video feedback mode

- output 8-bit data: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2 pins
- output PCLK: PCLK pin
- input 8-bit data: HREF,VSYNC,VI_3,VI_2,VI_1,VI_0,Y1,Y0 pins
- input PCLK: VICK pin
- input HREF: PAL pin (when using CCIR601)
- input VSYNC: BW pin (when using CCIR601)

2.8.2 DVP slave mode

- input PCLK: PCLK pin
- input HREF: VSYNC pin
- output 10-bit data: Y9,Y8,Y7,Y6,Y5,Y4,Y3,Y2,Y1,Y0 pins

table 2-3 video feedback mode

function	register	description
video feedback IO control	0x3062	Bit[1]: input/output selections of VICK, VI0, VI1, VI2, VI3 pins 0: input 1: output

2.9 FSIN

table 2-4 FSIN control register

function	register	description
FSIN I/O control	0x3062	Bit[2]: input/output selections of FSIN pin 0: input 1: output

For TV output, there are three modes for frame sync.

- VSYNC pin outputs FODD
- master chip FSIN pin outputs FODD, slave chip FSIN pin gets FODD from master chip
- all chips work as slave, pin FSIN gets a 30Hz (NTSC) / 25Hz (PAL) signal to synchronize

For DVP mode, slave chip FSIN gets VSYNC signal.

2.9.1 analog format

table 2-5 analog format and frame rate

function	format	resolution	field rate	input clock
analog output	NTSC	656x492	60 fields/sec	24.545452 MHz
	PAL	768x576	50 fields/sec	29.5 MHz

2.9.2 digital format

table 2-6 progressive format and frame rate

function	resolution	frame rate	input clock	output clock	
				RAW	YUV422
DVP output	WVGA (752x480)	30 fps	6~27 MHz	≥13.5 MHz ≤14.5 MHz	≥27 MHz ≤29 MHz
	VGA (640x480)	30 fps	6~27 MHz	≥12 MHz ≤14.5 MHz	≥24 MHz ≤29 MHz
	QVGA (320x240)	60 fps	6~27 MHz	≥12 MHz ≤14.5 MHz	≥24 MHz ≤29 MHz

3 block level description

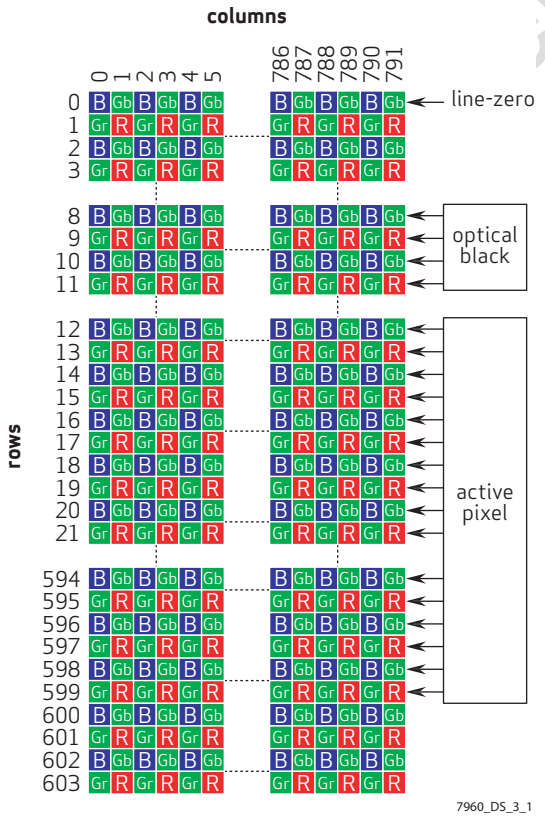
3.1 pixel array structure

The OV7960/OV7461 sensor has an image array of 792 columns by 604 rows (478,368 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 478,368 pixels, 768 x 576 (442,368) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7960/OV7461 provides mirror mode, which reverses the sensor data read-out order horizontally, and flip mode which reverses it vertically (see **figure 4-1**). In mirror mode, since the Bayer order changes from BGBG... to GBGB..., the read-out sequence will be adjusted automatically when the mirror function is on. In flip mode, the VREF starting line needs to be adjusted, then the ISP block will auto-detect whether the pixel is in red line or blue line and make necessary adjustments.

figure 4-1 mirror and flip samples

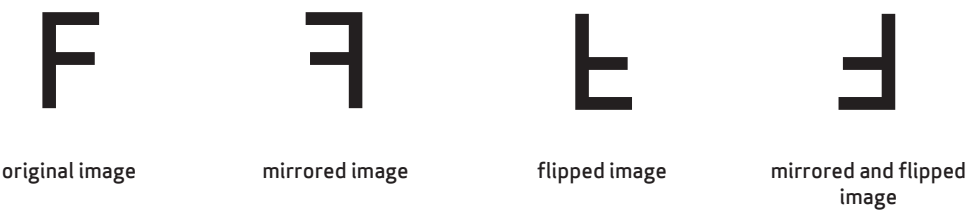


table 4-1 mirror and flip function control

function	register	description
mirror	0x300C	Bit[6]: mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0x300C	Bit[7]: flip ON/OFF select 0: flip OFF 1: flip ON

4.2 test pattern

For testing purposes, the OV7960/OV7461 offers one type of test pattern: color bar. There are 4 modes of the color bar (see **figure 4-2**). The modes of the color bar can be set with the register 0x5004[1:0]. In each mode the color bar can be moved from bottom to top if the bar rolling function is enabled by setting signal 0x5004[2] to 1. The moving step can be configured by setting the register 0x5051[3:1] (see **table 4-2**).

figure 4-2 test pattern

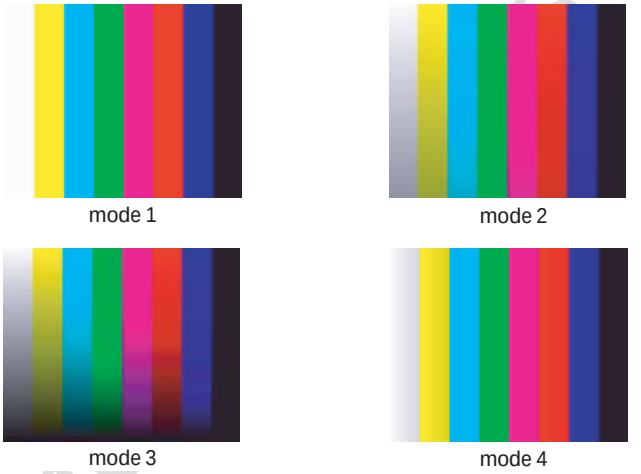


table 4-2 driving capability and direction control for I/O pads

function	register	description
color bar	0x5003	Bit[0]: color bar enable 0: normal image 1: color bar
color bar pattern select	0x5004	Bit[1:0]: four types of color bar patterns
color bar rolling selection	0x5004	Bit[2]: color bar rolling enable 0: still color bar 1: rolling color bar (from down to up)
color bar rolling step	0x5051	Bit[3:0]: color bar rolling step

4.3 AEC/AGC algorithms

4.3.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allow the image sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain for the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-3**.

table 4-3 AEC/AGC algorithms

function	register	description
AEC enable	0x3013	Bit[0]: AEC enable 0: manual 1: auto
AEC (exposure time)	{0x300F, 0x3010}	0x300F = AEC[15:8] 0x3010 = AEC[7:0]
AGC (gain)	{0x3015[1:0], 0x3000}	0x3015[1:0] = AGC[9:8] 0x3000 = AGC[7:0]
AGC enable	0x3013	Bit[2]: AGC enable 0: manual 1: auto

There are two different algorithms to tell whether the current frame is too bright or too dark and determine if the exposure time/gain should increase or decrease for the next frame. The Histogram algorithm is based on the statistics of the percentage of high/low luminance pixels. The other is based on the weighted average of a frame.

4.3.2 average-based algorithm

The average-based AEC controls image luminance using registers WPT (0x3024) and BPT (0x3025). In average-based mode the value of register WPT (0x3024) indicates the high threshold value, and the value of register BPT (0x3025) indicates the low threshold value. When the target image luminance average value YAVG (0x302F) is within the range specified by registers WPT (0x3024) and BPT (0x3025), the AEC keeps the image exposure. When register YAVG (0x302F) is greater than the value in register WPT (0x3024), the AEC will decrease the image exposure. When register YAVG (0x302F) is less than the value in register BPT (0x3025), the AEC will increase the image exposure. Accordingly, the value in register WPT (0x3024) should be greater than the value in register BPT (0x3025). The gap between the values of WPT (0x3024) and BPT (0x3025) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers WPT (0x3024) and BPT (0x3025). AEC set to normal mode will allow for single-step increase or decrease in the image exposure to maintain the specified range. A value of 0 in register FASTEN (0x3013[7]) will result in normal speed operation, and a 1 will result in fast speed operation.

Register VPT (0x3026) controls the fast AEC range. If the target image YAVG (0x302F) is greater than VPT[7:4] x 16, AEC will decrease by half the current exposure time. If register YAVG (0x302F) is less than VPT[3:0] x 16, AEC will increase to double the current exposure time.

As shown in **figure 4-3**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

outside control zone

step size: 2 × (AEC[15:0])

t_{STEP}: t_{ROW} × (2 × AEC[15:0])

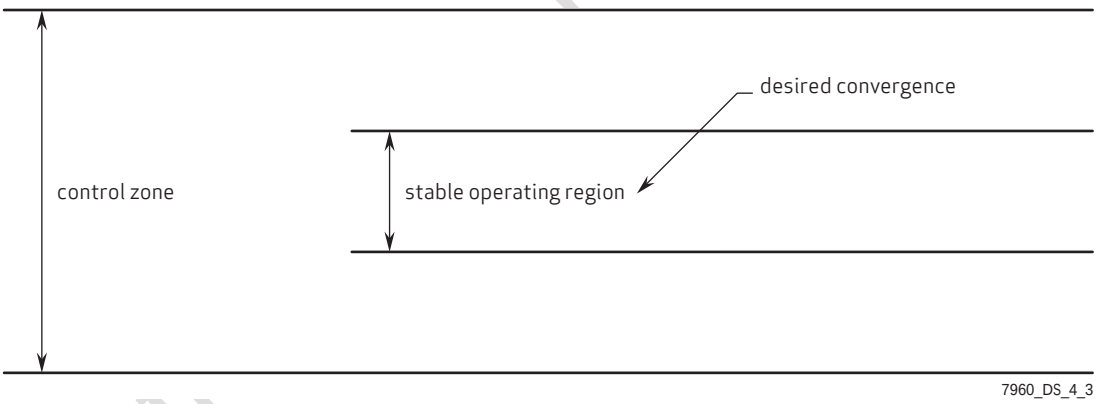
inside control zone

step size: 2 × (AEC[15:0]) ÷ 16)

t_{STEP}: t_{ROW} × (2 × AEC[15:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

figure 4-3 desired convergence



control zone upper limit: {VPT[7:4] (0x3026[7:4]), 4'b0000}

control zone lower limit: {VPT[3:0] (0x3026[3:0]), 4'b0000}

stable operating region upper limit: WPT[7:0] (0x3024)

stable operating region lower limit: BPT[7:0] (0x3025)

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided into sixteen (4 x 4) zones (see **figure 4-4**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.3.4,** average luminance (YAVG).

4.3.3 histogram-based algorithm

The histogram-based AEC controls image luminance using registers LVLB, LVLVB, LVLW, LVLVW, NUMB, NUMVB, NUMW and NUMVW. In histogram-based mode, the registers LVLB, LVLVB, LVLW and LVLVW indicate the luminance

level that a pixel is considered dark, very dark, bright, and very bright. NUMB indicates the low threshold value and NUMW indicates the high threshold value of the statistic. When the number of dark pixels is greater than the value specified by register NUMB, the AEC will increase the image exposure. When the number of bright pixels is greater than the value specified by the register NUMW, the AEC will decrease the image exposure.

The histogram-based algorithm supports both normal and fast speed selection in order to bring the image exposure into the proper level.

If the number of very dark pixels exceeds the value specified by register NUMVB, or the number of very bright pixels exceeds the value specified by register NUMVW, AEC will enter the fast mode if FASTEN (0x3013[7]) is set to 1. Otherwise the histogram-based algorithm works in normal mode.

table 4-4 AEC/AGC histogram algorithms

function	register	description
AEC enable	0x3013	Bit[0]: AEC enable 0: manual 1: auto
AEC (exposure time)	{0x300F, 0x3010}	0x300F = AEC[15:8] 0x3010 = AEC[7:0]
LAEC (less than 1 row exposure time)	{0x301F, 0x3030}	0x301F = LAEC[7:0] 0x3030 = LAEC[15:8]
AGC (gain)	{0x3015[1:0], 0x3000}	0x3015[1:0] = AGC[9:8] 0x3000 = AGC[7:0]
AGC enable	0x3013	Bit[2]: AGC enable 0: manual 1: auto

4.3.4 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. A 4x4 grid average window is defined. The average value is the weighted average of the 16 sections.

There are two window modes: auto window mode and sub window mode. In auto window mode (default mode), the 4x4 grid average window is defined by input image sizes (HW and VH) of the YAVG module. In the sub window mode (register 0x5690[7] set to 1), the window is defined by AVG_X_START, AVG_X_END, AVG_Y_START and AVG_Y_END registers. **figure 4-4** shows the sizes of definition window. **table 4-5** lists the corresponding registers.

figure 4-4 average-based window definition

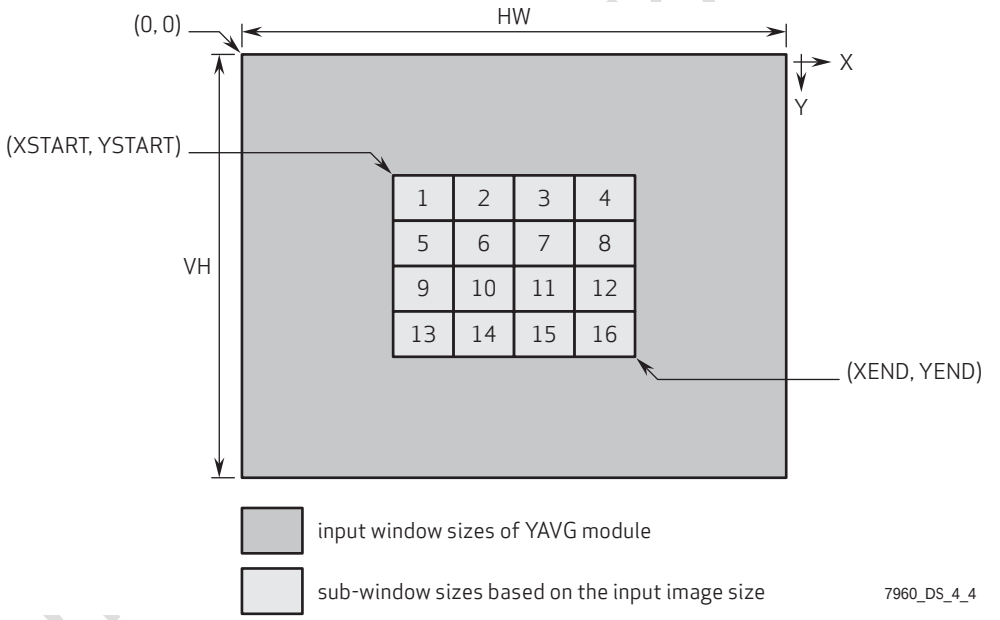


table 4-5 YAVG window and weight registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG XSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG XSTART	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window

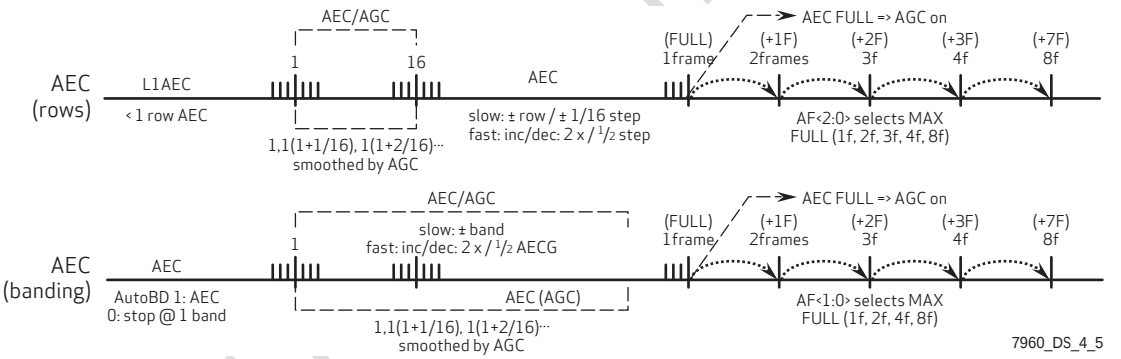
table 4-5 YAVG window and weight registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5682	AVG XEND	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG XEND	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG YSTART	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG YSTART	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window
0x5686	AVG YEND	0x06	RW	Bit[7:3]: Not used Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG YEND	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[7:4]: window1_weight Bit[3:0]: window0_weight
0x5689	AVG R9	0xFF	RW	Bit[7:4]: window3_weight Bit[3:0]: window2_weight
0x568A	AVG RA	0xFF	RW	Bit[7:4]: window5_weight Bit[3:0]: window4_weight
0x568B	AVG RB	0xFF	RW	Bit[7:4]: window7_weight Bit[3:0]: window6_weight
0x568C	AVG RC	0xFF	RW	Bit[7:4]: window9_weight Bit[3:0]: window8_weight
0x568D	AVG RD	0xFF	RW	Bit[7:4]: window11_weight Bit[3:0]: window10_weight
0x568E	AVG RE	0xFF	RW	Bit[7:4]: window13_weight Bit[3:0]: window12_weight
0x568F	AVG RF7	0xFF	RW	Bit[7:4]: window15_weight Bit[3:0]: window14_weight

4.4 AEC/AGC steps

figure 4-5 shows how the AEC and AGC work together to obtain adequate exposure/gain based on the current environment's illumination. The upper one illustrates the non-banding operation which time unit is based on Tline. The lower one shows exposure in banding. The x-axis represents the length of exposure in time scale. In normal light circumstances, the length of exposure will fall into a range from 1 Tline to 1 Tframe. In extremely bright or dark circumstances, exposure time less than 1 Tline/Tband or greater than 1 Tframe may be required accordingly. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred, rather than raising the analog gain, when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

figure 4-5 darker and brighter illumination situations



4.4.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

LAEC activates in extremely bright situations, allowing integration time to be less than one row. In extremely dark situations the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall within bands.

4.4.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to a minimum of 1/16 row or so. LAEC ON/OFF can be set in 0x5013[3].

4.4.1.2 banding filter

AC powered light sources usually have a frequency of 60Hz or 50Hz. When the sensor integration time is not an integer multiple to the light frequency, the image will flicker (horizontal banding). When auto detection mode is on,

the banding filter will automatically detect current light frequency and provide a rolling horizontal band eliminate function in auto exposure mode. The banding filter is deployed to filter out the banding effect caused by the 50/60 Hz lighting.

For a given operating frequency, band step can be expressed in terms of row timing.

In 50 or 60Hz flicker light, the exposure time must be multiple of the flicker interval to avoid the band shown on the image. For 50Hz light, the exposure time must be:

$t_{Exposure} = N \div 100$

For 60Hz light, the exposure time must be:

$t_{Exposure} = N \div 120$

where N is positive integer.

Since the exposure time, AEC[15:0], is based on row interval, it needs to be preset on how many rows is equal to 1/100 second and 1/120 second. Banding filter registers BD50ST and BD60ST, are used to set the number of rows of 1/100 and 1/120 second respectively. The banding filter can be calculated by:

BD60ST, 60Hz banding filter value = $1 \div (120 \times t_{row}$ interval)

= (frame rate × maximum exposure) ÷ 120

BD50ST, 50Hz banding filter value = $1 \div (100 \times t_{row}$ interval)

= (frame rate × maximum exposure) ÷ 100

where maximum exposure equals the number of line per frame, plus the number of dummy lines.

The band steps for 50Hz and 60Hz light sources can be set in registers 0x3052, 0x3054, and 0x3055.

Under strong brightness conditions, there is an option to allow the exposure time to go below the minimum banding filter value (1/120 or 1/100) to prevent overexposure. When the option is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If this option is disabled, the minimum integration time is one minimal band. The option can be set in register 0x3013[4].

4.4.1.2 automatic 50/60Hz banding detection

The OV7960/OV7461 supports automatic 50/60Hz banding detection function; current light frequency will be detected, and the exposure time will be automatically adjusted.

The auto mode can be enabled by setting 0x30EC[7].

4.4.1.3 banding mode OFF with AEC

When banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode, or becomes twice/half of the previous step in fast mode.

4.4.1.4 VAEC

In extremely dark situations, the integration time must be longer than one frame.

The OV7960/OV7461 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x3015[6:4]. VAEC can be disabled by setting register 0x3015[7] to 0.

table 4-6 AEC and banding filter registers

function	register	description
LAEC ON/OFF	0x3013	Bit[3]: LAEC ON/OFF select 0: OFF 1: ON
banding filter enable	0x3013	Bit[5]: banding filter enable 0: disable banding filter 1: enable banding filter
banding filter option	0x3013	Bit[4]: below banding step value enable 0: limit the minimum exposure time to 1/100 or 1/120 seconds under any light conditions when banding filter is enabled 1: allow exposure time to be less than 1/100 or 1/120 seconds under strong light conditions when banding filter is enabled
banding filter mode	0x30EC	Bit[7]: banding filter mode, effective when banding filter is enabled 0: manual mode 1: auto mode
banding filter manual mode	0x30EC	Bit[6]: light source frequency manual selection 0: 60Hz 1: 50Hz
banding filter step value (60Hz)	{0x3052, 0x3055}	banding filter step value for 60Hz light source (10 bits) 0x3052[7:6]: MSBs 0x3055[7:0]: LSBs
banding filter step value (50Hz)	{0x3052, 0x3054}	banding filter step value for 50Hz light source (10 bits) 0x3052[5:4]: MSBs 0x3054[7:0]: LSBs
maximum banding filter step (60Hz)	{0x3020, 0x3021}	banding filter maximum allowable number of steps for 60Hz light source (5 bits) 0x3052[6]: MSB 0x3055[3:0]: LSBs
maximum banding filter step (50 Hz)	{0x3020, 0x3021}	banding filter maximum allowable number of steps for 50Hz light source (5 bits) 0x3020[7]: MSB 0x3054[7:4]: LSBs

4.4.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases where adjacent AEC step changes are too large (>1/16), AGC step should be inserted in between; otherwise, the integration time will keep switching from two adjacent steps and the image flickers.

4.4.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.4.2.2 gain insertion between AEC banding steps

In banding ON mode, the minimum integration time change is the period of light intensity (10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.4.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

4.5 black level calibration (BLC)

The pixel array contains six optically shielded (black) rows. These rows are used to provide the data for offset cancellation algorithms (black level calibration).

Digital image processing starts with black level subtraction. The BLC algorithm estimates the offset of the black level from the data provided by black rows. These offsets of different color channels will be subtracted from values of the color pixels. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0. By default, BLC will be triggered when gain is changing.

table 4-7 BLC control functions (sheet 1 of 2)

function	register	description
target	0x3067	Bit[3:0]: 8-bit target black level value that is used in the algorithm. For 10-bit data, the target is {REG3067[3:0],0,0}
BLC_B, BLC_R	0x300E	Bit[6:5]: BLC_B, BLC_R 00: use all 4 channel offsets 01: use R/Gr channel offset for all channels 10: use B/Gb channel offset for all channels 11: use all 4 channel offsets
BLC always ON	0x3008	Bit[2]: BLC offsets be adjusted every frame
MBLC	0x3008	Bit[3]: trigger BLC manually for 64 frames

table 4-7 BLC control functions (sheet 2 of 2)

function	register	description
R offset	{0x309D[7:6], 0x309C}	BLC offset for R channel
B offset	{0x309D[5:4], 0x309B}	BLC offset for B channel
Gr offset	{0x309D[3:2], 0x309A}	BLC offset for Gr channel
Gb offset	{0x309D[1:0], 0x3099}	BLC offset for Gb channel

4.6 DIG GAIN / EVEN ODD

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-8 digital gain control functions

function	register	description
DGAIN	0x3015	Bit[1:0]: digital gain 00: 1x digital gain 01: 2x digital gain 10: 2x digital gain 11: 4x digital gain

4.7 one-time programmable (OTP) memory

The OV7960/OV7461 has a one-time programmable (OTP) memory to store chip identification and manufacturing information. This OTP memory is organized as 128-bit by 1 one-time programmable electrical fuse with random access interface. The main function is to store chip identification and manufacturing information.

The OTP has three operation modes: program (PGM), READ, and inactive. Normally, it is in inactive mode. By setting 0x30EF to 0xAA, it enters program mode, which will sequentially burn data into the OTP macro. By setting 0x30FE to 0x55, the OTP enters read mode, which will load the OTP data into registers. **table 4-9** summarizes the corresponding registers.

table 4-9 OTP registers

function	register	description
OTP program data	0x30F0~0x30FF	data to be programmed/read into/from OTP memory
OTP program/read enable	0x30EF	0x55: read OTP memory 0xAA: program OTP memory

5 image sensor processor digital functions

5.1 DSP_TOP

The main purposes of DSP_Top are:

- integrate all sub-modules
- create necessary control signals

table 5-1 DSP top registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0xDF	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[4]: Even odd removing enable 0: Disable 1: Enable Bit[3]: De-noise enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 5-1 DSP top registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x4F	RW	ISP Control 01 Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable Bit[3]: Auto contrast enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5002	ISP CTRL02	0xE0	RW	ISP Control 02 Reserved
0x5003	ISP CTRL03	0xA8	RW	ISP Control 03 Bit[7]: Pad in buffer control enable 0: Buffer control boundary padded external 1: Buffer control pad boundary internal Bit[6:4]: Reserved Bit[3]: YUV to YCbCr enable 0: Disable 1: Enable Bit[2:1]: Reserved Bit[0]: Color bar test pattern enable 0: Disable 1: Enable

table 5-1 DSP top registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5004	ISP CTRL04	0x08	RW	ISP Control 04 Bit[7:3]: Reserved Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style
0x5005	ISP CTRL05	0xDC	RW	SP Control 05 Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma Bit[5]: UV average old style enable 0: Disable 1: Enable Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction Bit[1:0]: Reserved

table 5-1 DSP top registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5024	ISP CTRL36	0x80	RW	ISP Control 36 Bit[7]: Reserved Bit[6]: Rgma manual mode 0: Use internal divider result for SLPH 1: Use register for SLPH Bit[5:0]: Reserved
0x5040	ISP CTRL64	0x00	RW	Bit[7:0]: isp_sccb_offset
0x5041	ISP CTRL65	0x16	RW	Bit[7:6]: Reserved Bit[5]: bcc_en Bit[4]: yavg_en Bit[3]: Reserved Bit[2]: isp_en Bit[1]: yclp_en Bit[0]: Reserved
0x5042	ISP CTRL66	0x03	RW	Bit[7]: old_lenc_mode Bit[6:4]: Reserved Bit[3]: out_size_mode Bit[2]: Reserved Bit[1:0]: yavg_source
0x5043	ISP CTRL67	0x00	RW	Bit[7:3]: Reserved Bit[2]: gma_off_man_en Bit[1]: awb_off_man_en Bit[0]: lenc_off_man_en
0x5044	ISP CTRL68	0x00	RW	Bit[7:0]: sensor_bias_man
0x5045	ISP CTRL69	0x00	RW	Bit[7:4]: Reserved Bit[3]: interlace_man Bit[2]: interlace_man_en Bit[1]: bw_man Bit[0]: bw_man_en
0x5046	ISP CTRL70	0x30	RW	Bit[7]: dpc_h_swap Bit[6]: Reserved Bit[5:0]: color_noise_alpha
0x5047	ISP CTRL71	0x01	RW	Bit[7:1]: Reserved Bit[0]: cont_cip_sync
0x5048	ISP CTRL72	0x00	RW	Bit[7:4]: lenc_ystart_adj Bit[3:0]: lenc_xstart_adj

5.2 DSP_PRE

The main purposes of the DSP_PRE module include:

- adjust HREF, valid, RBlue signals and data
- create color bar image
- determine the sizes of input image by removing redundant data
- create control signals

table 5-2 DSP_PRE registers

address	register name	default value	R/W	description
0x5003	ISP CTRL03	0x00	RW	Bit[0]: Color bar test pattern enable 0: Disable 1: Enable
0x5004	ISP CTRL04	0x08	RW	ISP Control 04 Bit[7:3]: Reserved Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style
0x5051	BAR STEP	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: bar_step

5.3 SYNC

The SYNC module merges two data paths into one data path to the ISP.

table 5-3 SYNC registers

address	register name	default value	R/W	description
0x5050	SYNC CTRL00	0x00	RW	Bit[7:4]: Reserved Bit[3]: rblue_rvs Bit[2]: first_pix_rmv Bit[1]: second_edge Bit[0]: neg_edge

5.4 EVENODD

The main function of EVENODD is to eliminate the different average values between even and odd columns, which may be caused by some electrical characteristics of the AD quantizer or other devices in the sensor. According to the sum and difference between the adjacent pixel, the module calculates the EVENODD offset for B, GB, GR, and R channels, and then corrects each pixel with it to compensate the pixel with the EVENODD effect. Some manual setting registers have been implemented to adjust this function.

table 5-4 EVENODD registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x1	RW	Bit[4]: Even odd removing enable 0: Disable 1: Enable
0x5080	EVEN THRE	0x40	RW	Bit[7:0]: Threshold for the difference between the adjacent pixel in the same channel. Value should be less than half of black level.
0x5081	EVEN CTRL01	0x00	RW	Bit[7:6]: Not used Bit[5:1]: Reserved Bit[0]: Manual mode enable
0x5082	EVEN CTRL02	0x00	RW	Bit[7:0]: Manual compensation on B pixel on left side of Gb pixel in 10-bit scale
0x5083	EVEN CTRL03	0x00	RW	Bit[7:0]: Manual compensation on B pixel on right side of Gb pixel in 10-bit scale
0x5084	EVEN CTRL04	0x00	RW	Bit[7:0]: Manual compensation on Gb pixel on left side of B pixel in 10-bit scale
0x5085	EVEN CTRL05	0x00	RW	Bit[7:0]: Manual compensation on Gb pixel on right side of B pixel in 10-bit scale
0x5086	EVEN CTRL06	0x00	RW	Bit[7:0]: Manual compensation on Gr pixel on left side of R pixel in 10-bit scale

table 5-4 EVENODD registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5087	EVEN CTRL07	0x00	RW	Bit[7:0]: Manual compensation on Gr pixel on right side of R pixel in 10-bit scale
0x5088	EVEN CTRL08	0x00	RW	Bit[7:0]: Manual compensation on R pixel on left side of Gr pixel in 10-bit scale
0x5089	EVEN CTRL09	0x00	RW	Bit[7:0]: Manual compensation on R pixel on right side of Gr pixel in 10-bit scale
0x508A	EVEN CTRL10	0x00	RW	Debug Mode Changing this value is not allowed
0x508B	EVEN MINNUM	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Pixel number[18:16] Threshold that triggers compensation update
0x508C	EVEN MINNUM	0x01	RW	Bit[7:0]: Pixel number[15:8] Threshold that triggers compensation update
0x508D	EVEN MINNUM	0x00	RW	Bit[7:0]: Pixel number[7:0] Threshold that triggers compensation update

5.5 lens correction (LENC)

The main purpose of LENC is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel. Correct each pixel with its gain calculated to compensate the light distribution due to lens curvature.

table 5-5 LENC registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x1	RW	Bit[7]: LENC correction enable 0: Disable 1: Enable
0x5005	ISP CTRL05	0x1 0x1	RW	Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction
0x5042	ISP CTRL66	0x0	RW	Bit[7]: old_lenc_mode
0x5043	ISP CTRL67	0x0	RW	Bit[0]: lenc_off_man_en
0x5048	ISP CTRL72	0x00	RW	Bit[7:4]: lenc_ystart_adj Bit[3:0]: lenc_xstart_adj
0x5100	LENC RED X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: red_x0[9:8] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5101	LENC RED X0	0x0C	RW	Bit[7:0]: red_x0[7:0] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047

table 5-5 LENC registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x5102	LENC RED Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: red_y0[9:8] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5103	LENC RED Y0	0x06	RW	Bit[7:0]: red_y0[7:0] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5104	LENC RED A1	0x22	RW	LENC Control 04 Bit[7]: Not used Bit[6:0]: red_a1[6:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5105	LENC RED A2	0x07	RW	LENC Control 05 Bit[7:4]: Not used Bit[3:0]: red_a2[3:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5106	LENC RED B1	0xC2	RW	LENC Control 06 Bit[7:0]: red_b1[7:0] Composed of the second group of factors used in the LENC correction of the red color channels
0x5107	LENC RED B2	0x08	RW	LENC Control 07 Bit[7:4]: Not used Bit[3:0]: red_b2[3:0] Composed of the second group of factors used in the LENC correction of the red color channels

table 5-5 LENC registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x5108	LENC GRN X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: green_x0[9:8] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5109	LENC GRN X0	0x0C	RW	Bit[7:0]: green_x0[7:0] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x510A	LENC GRN Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: green_y0[9:8] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x510B	LENC GRN Y0	0x06	RW	Bit[7:0]: green_y0[7:0] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x510C	LENC GRN A1	0x22	RW	LENC Control 12 Bit[7]: Not used Bit[6:0]: green_a1[6:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510D	LENC GRN A2	0x07	RW	LENC Control 13 Bit[7:4]: Not used Bit[3:0]: green_a2[3:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510E	LENC GRN B1	0xC2	RW	LENC Control 14 Bit[7:0]: green_b1[7:0] Composed of the second group of factors used in the LENC correction of the green color channels

table 5-5 LENC registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x510F	LENC GRN B2	0x08	RW	LENC Control 15 Bit[7:4]: Not used Bit[3:0]: green_b2[3:0] Composed of the second group of factors used in the LENC correction of the green color channels
0x5110	LENC BLU X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: blue_x0[9:8] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5111	LENC BLU X0	0x0C	RW	Bit[7:0]: blue_x0[7:0] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 2047
0x5112	LENC BLU Y0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: blue_y0[11:8] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5113	LENC BLU Y0	0x06	RW	Bit[7:0]: blue_y0[7:0] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image. Range is 0 ~ 1535
0x5114	LENC BLU A1	0x22	RW	LENC Control 20 Bit[7]: Not used Bit[6:0]: blue_a1[6:0] Composed of the first group of factors used in the LENC correction of the blue color channels

table 5-5 LENC registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x5115	LENC BLU A2	0x07	RW	LENC Control 21 Bit[7:4]: Not used Bit[3:0]: blue_a2[3:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5116	LENC BLU B1	0xC2	RW	LENC Control 22 Bit[7:0]: blue_b1[7:0] Composed of the second group of factors used in the LENC correction of the blue color channels
0x5117	LENC BLU B2	0x08	RW	LENC Control 23 Bit[7:4]: Not used Bit[3:0]: blue_b2[3:0] Composed of the second group of factors used in the LENC correction of the blue color channels
0x5118	LENC XSTART	0x00	RW	Bit[7:2]: Not used Bit[1:0]: X coordinate of the lens starting point high bit
0x5119	LENC XSTART	0x00	RW	Bit[7:0]: X coordinate of the lens starting point low bit
0x511A	LENC YSTART	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Y coordinate of the lens starting point high bit
0x511B	LENC YSTART	0x00	RW	Bit[7:0]: Y coordinate of the lens starting point low bit

table 5-5 LENC registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x511C	LENC CTRL24	0x80	RW	LENC Control 24 Bit[7]: round_en Determines whether or not to round off the last two bits of the LENC input data 0: Do not round off the last two bits 1: Round off the last two bits Bit[6]: Debug mode Changing this value is not allowed Bit[5]: Sensor gain coefficient manual control (only when 0x5118[4]=1) 0: Use 0x80 as lens correction coefficient threshold 1 1: Use register 0x511C as lens correction coefficient threshold 1 Bit[4]: Coefficient manual control 0: Manual control coefficients 1: Automatically compute coefficients Bit[3:2]: Horizontal skip mode Valid only when the image size is not full size 00: Does not skip a pixel 01: Skips 1 pixel every 2 pixels 10: Skips 3 pixels every 4 pixels 11: Skips 7 pixels every 8 pixels Bit[1:0]: Vertical skip mode 00: Does not skip line 01: Skips 1 line every 2 lines 10: Skips 3 lines every 4 lines 11: Skips 7 lines every 8 lines
0x511D	LENC CTRL25	0x00	RW	Bit[7:0]: Reserved

5.6 raw gamma (RGMA)

The main purpose of the raw gamma (RGMA) function is to compensate for the non-linear characteristics of the sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output under different light strengths. The non-linear gamma curve is approximately constructed with different linear functions. RAWGAMMA compensates the image in the RAW domain and shares the curve parameters with YUVGAM to save registers. RAWGAMMA should be turned OFF when YUVGAM is ON.

table 5-6 RGMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x0	RW	Bit[5]: RAW gamma enable 0: Disable 1: Enable
0x5005	ISP CTRL05	0x1 0x1	RW	Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma
0x5024	ISP CONTROL 36	0x80	RW	ISP Control 36 Bit[7]: Reserved Bit[6]: Rgma manual mode 0: Use internal divider result for SLPH 1: Use register for SLPH Bit[5:0]: Reserved
0x5043	ISP CTRL67	0x0	RW	Bit[2]: gma_off_man_en
0x5480	GAMMA CTRL00	0x1A	RW	Bit[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x28	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x3E	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1

table 5-6 RGMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5483	GAMMA CTRL03	0x5E	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x6B	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x77	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1
0x5486	GAMMA CTRL06	0x81	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1
0x5487	GAMMA CTRL07	0x8B	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x94	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1
0x5489	GAMMA CTRL09	0x9C	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0xAB	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xB8	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCE	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1
0x548D	GAMMA CTRL0D	0xDF	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEC	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0D	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3

5.7 auto white balance (AWB)

The main purpose of auto white balance (AWB) is the process of removing unrealistic colors so that objects which appear white in person are rendered white in the image or video. Thus, the AWB makes sure that the white color is consistent in different color temperatures. It supports manual white balance and auto white balance. For auto white balance, simple AWB and advanced AWB methods are supplied. Advance AWB takes into account the color temperature of a light source, which it relates to the relative warmth or coolness of white light.

table 5-7 AWB registers

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x1	RW	Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5005	ISP CTRL05	0x1	RW	Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain
0x5043	ISP CTRL67	0x0	RW	Bit[1]: awb_off_man_en
0x5180	AWB BBLOCK	0xFF	RW	Bit[7:0]: awb_b_block
0x5181	AWB CTRL00	0x58	RW	Bit[7:6]: step_local Bit[5:4]: step_fast Bit[3]: slop_8x Bit[2]: slop_4x Bit[1]: one_zone Bit[0]: avg_all
0x5182	AWB CTRL01	0x11	RW	Bit[7:4]: max_local_cnt Bit[3:0]: max_fast_cnt

5.8 defective pixel cancellation (DPC)

Due to processes and other reasons, pixel defects in the sensor array will occur, generating wrong color values when taking a picture. The main purpose of DPC is to remove the effect caused by these defective pixels. Also, some special functions are available for those pixels located at the image boundary. To remove the white/black pixel effect correctly, the proper threshold should first be determined.

table 5-8 DPC registers

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x1 0x1	RW	Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable
0x5045	ISP CTRL69	0x0 0x0	RW	Bit[1]: bw_man Bit[0]: bw_man_en
0x5046	ISP CTRL70	0x0	RW	Bit[7]: dpc_h_swap
0x5280	DPC CTRL00	0x77	RW	Bit[6]: detail_en 0: Disable detail detection method 1: Enable detail detection method Bit[5:4]: bd_sel[1:0] Boundary select options Bit[3]: man_en 0: Disable manual mode 1: Enable manual mode Bit[2]: smooth_en Enable using average G values when doing recovery Bit[1]: sc_en 0: Disable same channel detection 1: Enable same channel detection Bit[0]: dc_en 0: Disable different channel detection 1: Enable different channel detection

5.9 DNS

Noise in digital images is most visible in uniform surfaces, and increases with temperature, sensitivity and decreasing pixel size.The main purpose of the DNS function is to decrease this noise.

table 5-9 DNS registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x1	RW	Bit[3]: De-noise enable 0: Disable 1: Enable
0x5046	ISP CTRL70	0x30	RW	Bit[5:0]: color_noise_alpha
0x5290	DNS CTRL 00	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Coefficient of Y de-noise threshold with respect to Y
0x5291	DNS CTRL 01	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Coefficient of UV de-noise threshold with respect to Y
0x5292	DNS CTRL 02	0x00	RW	Bit[7:1]: Not used Bit[0]: De-noise and sharpness manual mode enable 0: Auto 1: Manual
0x5293	NOISE Y	0x02	RW	Bit[7:0]: noise_y De-noise weight for Y
0x5294	NOISE U	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise U high byte De-noise weight for UV
0x5295	NOISE U	0x02	RW	Bit[7:0]: Noise U low byte De-noise weight for UV
0x5296	NOISE V	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise V high byte De-noise weight for UV
0x5297	NOISE V	0x02	RW	Bit[7:0]: Noise V low byte De-noise weight for UV
0x5298	DNS EDGETHRE MAN	0x06	RW	Bit[7:0]: DNS edgethre Edge threshold for UV smoothing
0x5299	DNS GBGR EXTRA	0x04	RW	Bit[7:0]: DNS CbCr extra De-noise threshold adjustment for Cb and Cr

table 5-9 DNS registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x529A	NOISE YLIST0	0x02	RW	Bit[7:0]: Noise Y list0[7:0] Noise Y threshold at 1x sensor gain
0x529B	NOISE YLIST1	0x04	RW	Bit[7:0]: Noise Y list1[7:0] Noise Y threshold at 2x sensor gain
0x529C	NOISE YLIST2	0x08	RW	Bit[7:0]: Noise Y list2[7:0] Noise Y threshold at 4x sensor gain
0x529D	NOISE YLIST3	0x14	RW	Bit[7:0]: Noise Y list03[7:0] Noise Y threshold at 8x sensor gain
0x529E	NOISE YLIST4	0x1E	RW	Bit[7:0]: Noise Y list4[7:0] Noise Y threshold at 16x sensor gain
0x529F	NOISE YLIST5	0x28	RW	Bit[7:0]: Noise Y list5[7:0] Noise Y threshold at 32x sensor gain
0x52A0	NOISE YLIST6	0x32	RW	Bit[7:0]: Noise Y list6[7:0] Noise Y threshold at 64x sensor gain
0x52A1	NOISE YLIST7	0x32	RW	Bit[7:0]: Noise Y list7[7:0] Noise Y threshold at 64x sensor gain
0x52A2	NOISE UVLIST0	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list0[8] Noise UV threshold at 1x sensor gain
0x52A3	NOISE UVLIST0	0x02	RW	Bit[7:0]: Noise UV list0[7:0] Noise UV threshold at 1x sensor gain
0x52A4	NOISE UVLIST1	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list1[8] Noise UV threshold at 2x sensor gain
0x52A5	NOISE UVLIST1	0x04	RW	Bit[7:0]: Noise UV list1[7:0] Noise UV threshold at 2x sensor gain
0x52A6	NOISE UVLIST2	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list2[8] Noise UV threshold at 4x sensor gain

table 5-9 DNS registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x52A7	NOISE UVLIST2	0x0C	RW	Bit[7:0]: Noise UV list2[7:0] Noise UV threshold at 4x sensor gain
0x52A8	NOISE UVLIST3	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list3[8] Noise UV threshold at 8x sensor gain
0x52A9	NOISE UVLIST3	0x28	RW	Bit[7:0]: Noise UV list3[7:0] Noise UV threshold at 8x sensor gain
0x52AA	NOISE UVLIST4	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list4[8] Noise UV threshold at 16x sensor gain
0x52AB	NOISE UVLIST4	0x32	RW	Bit[7:0]: Noise UV list4[7:0] Noise UV threshold at 16x sensor gain
0x52AC	NOISE UVLIST5	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list5[8] Noise UV threshold at 32x sensor gain
0x52AD	NOISE UVLIST5	0x3C	RW	Bit[7:0]: Noise UV list5[7:0] Noise UV threshold at 32x sensor gain
0x52AE	NOISE UVLIST6	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list6[8] Noise UV threshold at 64x sensor gain
0x52AF	NOISE UVLIST6	0x4C	RW	Bit[7:0]: Noise UV list6[7:0] Noise UV threshold at 64x sensor gain
0x52B0	NOISE UVLIST7	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list7[8] Noise UV threshold at 64x sensor gain
0x52B1	NOISE UVLIST7	0x4C	RW	Bit[7:0]: Noise UV list7[7:0] Noise UV threshold at 64x sensor gain

5.10 color interpolation (CIP)

The main function of the color interpolation (CIP) is interpolation from raw data to YUV data. For edge enhancement, both manual and auto modes are provided. RAW format is used for the sensor source image data, which means only one of R, G and B can be used for each pixel. CIP is needed to get the other two color values. CIP calculates those two color values using the neighboring same pixel (such as a real B pixel) to get the full RGB information for each pixel. YUV information can also be supported. The CIP functions include de-noising of raw images, RAW to RGB interpolation, and edge enhancement. CIP functions work in both manual and auto modes.

table 5-10 CIP registers

address	register name	default value	RW	description
0x5000	ISP CTRL00	0x1	RW	Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable
0x5045	ISP CTRL69	0x00	RW	Bit[7:4]: Reserved Bit[3]: interlace_man Bit[2]: interlace_man_en Bit[1]: bw_man Bit[0]: bw_man_en

5.11 CMX

The main purpose of Color Matrix (CMX) is converting the image from RGB domain to YUV domain. For different color temperature, the parameters in the transmitting function will be changed.

table 5-11 CMX registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x1	RW	Bit[1]: Color matrix enable 0: Disable 1: Enable
0x5380	CMX00	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: cmx00[9:8]
0x5381	CMX00	0x00	RW	Bit[7:0]: cmx00[7:0]
0x5382	CMX01	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx01[9:8]
0x5383	CMX01	0x17	RW	Bit[7:0]: cmx01[7:0]

table 5-11 CMX registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5384	CMX02	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx02[9:8]
0x5385	CMX02	0x01	RW	Bit[7:0]: cmx02[7:0]
0x5386	CMX10	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx10[9:8]
0x5387	CMX10	0x00	RW	Bit[7:0]: cmx10[7:0]
0x5388	CMX11	0x01	RW	Bit[7:2]: Reserved Bit[1:0]: cmx11[9:8]
0x5389	CMX11	0x35	RW	Bit[7:0]: cmx11[7:0]
0x538A	CMX12	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx12[9:8]
0x538B	CMX12	0x3E	RW	Bit[7:0]: cmx12[7:0]
0x538C	CMX20	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx20[9:8]
0x538D	CMX20	0x00	RW	Bit[7:0]: cmx20[7:0]
0x538E	CMX21	0x0A	RW	Bit[7:2]: Reserved Bit[1:0]: cmx21[9:8]
0x538F	CMX21	0x00	RW	Bit[7:0]: cmx21[7:0]
0x5390	CMX22	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: cmx22[9:8]
0x5391	CMX22	0xCD	RW	Bit[7:0]: cmx22[7:0]
0x5392	CMX SIGN	0x00	RW	Bit[7:1]: Reserved Bit[0]: cmx_sign[8]
0x5393	CMX SIGN	0x20	RW	Bit[7:0]: cmx_sign[7:0]
0x5394	CMX SHIFT	0x08	RW	Bit[7:4]: Reserved Bit[3:0]: cmx_shift

5.12 CONTRAST

The auto-contrast module is designed to stretch the image linearly to adjust the contrast according to the statistics results. According to the chosen parameters, the function can automatically calculate the maximum and minimum levels. Thus, the image will be adjusted to the correct brightness in different scenes which are implemented using the statistic information of each frame.

table 5-12 contrast registers

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x1	RW	Bit[3]: Auto contrast enable 0: Disable 1: Enable
0x5400	CONTRAST MAX HIGH LEVEL	0x3F	RW	Bit[7]: Not used Bit[6:0]: Maximum high level[14:8] Maximum high level threshold Changing this value is not recommended
0x5401	CONTRAST MAX HIGH LEVEL	0xFF	RW	Bit[7:0]: Maximum high level[7:0] Maximum high level threshold Changing this value is not recommended
0x5402	CONTRAST MIN HIGH LEVEL	0x3C	RW	Bit[7]: Not used Bit[6:0]: Minimum high level[14:8] Minimum high level threshold in 15-bit scale
0x5403	CONTRAST MIN HIGH LEVEL	0x00	RW	Bit[7:0]: min_high_level[7:0]
0x5404	CONTRAST MAX LOW LEVEL	0x02	RW	Bit[7]: Not used Bit[6:0]: Maximum low level[14:8] Maximum low level threshold in 15-bit scale
0x5405	CONTRAST MAX LOW LEVEL	0x00	RW	Bit[7:0]: Maximum low level[7:0] Maximum low level threshold in 15-bit scale
0x5406	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7]: Not used Bit[6:0]: Minimum low level[14:8] Minimum low level threshold in 15-bit data range
0x5407	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7:0]: Minimum low level[7:0] Minimum low level threshold in 15-bit data range

5.13 YUV gamma (YGMA)

For the YUVGAMMA function, UV gamma is separated from Y gamma. The UV gamma curve has a special relationship with Y gamma. Also, some special functions related to UV and H processing in dark and bright conditions are available.

When RGMA is enabled, all parameters of YGMA will be fixed.

table 5-13 YGMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5000	ISP CTRL00	0x1	RW	Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable
0x5480	GAMMA CTRL00	0x1A	RW	it[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x28	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x3E	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1
0x5483	GAMMA CTRL03	0x5E	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x6B	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x77	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1
0x5486	GAMMA CTRL06	0x81	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1

table 5-13 YGMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5487	GAMMA CTRL07	0x8B	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x94	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1
0x5489	GAMMA CTRL09	0x9C	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0xAB	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xB8	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCE	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1
0x548D	GAMMA CTRL0D	0xDF	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEC	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0D	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3

5.14 UV average (UVAVG)

The main purpose of the UVAVG module is to smooth UV by averaging.

table 5-14 UVAVG registers

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x1	RW	Bit[2]: UV average enable 0: Disable 1: Enable
0x5005	ISP CTRL05	0x0	RW	Bit[5]: UV average old style enable 0: Disable 1: Enable

5.15 UV adjust (UVADJ)

The main purposes of the UVADJ module is to adjust UV according to the sensor gain and register parameters.

table 5-15 VAP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x1	RW	Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable
0x5500	UV UVADJUST CONTROL 0	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Auto color saturation offset UV ADJUST IN value minimum threshold
0x5501	UV UVADJUST CONTROL 3	0x1F	RW	Bit[7:6]: Not used Bit[5]: Color saturation manual adjustment enable 0: Automatically adjust color saturation according to sensor gain 1: Manual set color saturation by register 0x5501[4:0] Bit[4:0]: UV ADJUST IN manual setting Manual color saturation setting

table 5-15 VAP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5502	UV ADJ TH1	0x00	RW	Bit[7:1]: Not used Bit[0]: UV ADJ TH1[8] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, the UV ADJUST IN will be limited to 31
0x5503	UV ADJ TH1	0x00	RW	Bit[7:0]: UV ADJ TH1[7:0] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, the UV ADJUST IN will be limited to 31.
0x5504	UV ADJ TH2	0x01	RW	Bit[7:1]: Reserved Bit[0]: UV ADJ TH2[8] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).
0x5505	UV ADJ TH2	0xFF	RW	Bit[7:0]: UV adj th2[7:0] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).

5.16 special digital effect (SDE)

The main purpose of Special Digital Effect (SDE) is making special digital effects such as hue/saturation etc.

Use SDE_Ctrl to use the following effects:

- calculate the new U and V based on Hue Cos, Hue Sin and sign of the parameters; if the hue angle is enabled, calculation will be based on hue angle
- fix U and V values
- saturate U and V according to Sat_u and Sat_v
- calculate Y from Y offset, Y gain, and Y bright
- set Y to be a fixed value
- invert Y, U, and V values to get a negative image
- fix U and V to 128 (8-bit data) resulting in a gray image

table 5-16 SDE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5001	ISP CTRL01	0x0	RW	Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable
0x5580	SDE CONTROL0	0x00	RW	Bit[7]: Fixed Y enable - works with register 0x5587[7:0] 0: Fixed Y disable 1: Fixed Y enable Bit[6]: Negative Y enable 0: Negative Y disable 1: Negative Y enable Bit[5]: Gray image enable 0: Gray image disable 1: Gray image enable Bit[4]: Fixed V enable - works with register 0x5586[7:0] 0: Fixed V disable 1: Fixed V enable Bit[3]: Fixed U enable - works with register 0x5585[7:0] 0: Fixed U disable 1: Fixed U enable Bit[2]: Contrast enable - works with registers 0x5587[7:0], 0x5588[7:0], and 0x5589[7:0] 0: Contrast disable 1: Contrast enable Bit[1]: Saturation enable - works with registers 0x5583[7:0] and 0x5584[7:0] 0: Saturation disable 1: Saturation enable Bit[0]: Hue enable 0: Hue disable 1: Hue enable

table 5-16 SDE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: hue_cos When register 0x558A[6] = 0, this register is hue_cos. When register 0x558A[6] = 1, this register is angle[7:0].
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: hue_sin When register 0x558A[6] = 0, this register is hue_sin. When register 0x558A[6] = 1, this register is angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL10	0x01	RW	Bit[7]: Yoffset manual mode enable 0: Auto mode for Yoffset in contrast 1: Manual mode for Yoffset in contrast Bit[6]: Hue angle enable Bit[5]: COS sign for Cr Bit[4]: COS sign for Cb Bit[3]: Offset sign for contrast Bit[2]: Bright sign for contrast Bit[1]: SIN sign for Cb Bit[0]: SIN sign for Cr

5.17 VarioPixel™ (VAP)

The main purposes of the VarioPixel module is to do horizontal sub-sampling.

table 5-17 VAP registers

address	register name	default value	R/W	description
0x3064	SCTRL39	0x0	RW	Bit[3]: h_vap_en
0x5052	VAP CTRL00	0x04	RW	Bit[7:3]: Reserved Bit[2]: Mean Bit[1:0]: Drop

5.18 background color correction (BCC)

The main purpose of the background color correction module is to apply the gain to other two channels according to the current light type.

table 5-18 BCC registers

address	register name	default value	R/W	description
0x5041	ISP CTRL65	0x00	RW	Bit[5]: bcc_en
0x5057	BCC BG GAIN	0x00	RW	Bit[7:0]: bg_gain[7:0]
0x5058	BCC BG GAIN	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: bg_gain[11:8]
0x5059	BCC GR GAIN	0x00	RW	Bit[7:0]: gr_gain[7:0]
0x505A	BCC GR GAIN	0x04	RW	Bit[7:4]: Reserved Bit[3:0]: gr_gain[11:8]
0x505B	BCC COLOR TYPE	0x00	RW	Bit[7:2]: Reserved Bit[1:0]: color_type

5.19 CLIP

The main purpose of the CLIP module is to clip the Y and UV data with Y threshold and C threshold

table 5-19 CLIP registers

address	register name	default value	R/W	description
0x5041	ISP CTRL65	0x1	RW	Bit[1]: yclp_en
0x5053	CLIP YTHREH	0xFF	RW	Bit[7:0]: y_thre_h
0x5054	CLIP YTHREL	0x00	RW	Bit[7:0]: y_thre_l
0x5055	CLIP CTHREH	0xFF	RW	Bit[7:0]: c_thre_h
0x5056	CLIP CTHREL	0x00	RW	Bit[7:0]: c_thre_l

5.20 16-zone luminance average (YAVG)

The main purposes of the YAVG module are:

- calculate Y average based on selected window
- output one average of window each time
- output Y data

table 5-20 YAVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5041	ISP CTRL65	0x1	RW	Bit[4]: yavg_en
0x5042	ISP CTRL66	0x0 0x11	RW	Bit[3]: out_size_mode Bit[1:0]: yavg_source
0x5680	AVG XSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG XSTART	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG XEND	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG XEND	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG YSTART	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG YSTART	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window
0x5686	AVG YEND	0xFF	RW	Bit[7:3]: Not used Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG YEND	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[7:4]: window1_weight Bit[3:0]: window0_weight

table 5-20 YAVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5689	AVG R9	0xFF	RW	Bit[7:4]: window3_weight Bit[3:0]: window2_weight
0x568A	AVG RA	0xFF	RW	Bit[7:4]: window5_weight Bit[3:0]: window4_weight
0x568B	AVG RB	0xFF	RW	Bit[7:4]: window7_weight Bit[3:0]: window6_weight
0x568C	AVG RC	0xFF	RW	Bit[7:4]: window9_weight Bit[3:0]: window8_weight
0x568D	AVG RD	0xFF	RW	Bit[7:4]: window11_weight Bit[3:0]: window10_weight
0x568E	AVG RE	0xFF	RW	Bit[7:4]: window13_weight Bit[3:0]: window12_weight
0x568F	AVG RF	0xFF	RW	Bit[7:4]: window15_weight Bit[3:0]: window14_weight
0x5690	AVG CTRL08	0x00	RW	Bit[7]: win_man Bit[6:4]: Reserved Bit[3:0]: yavg_mnr
0x5691	AVG BLK THRESH	0x00	RW	Bit[7:0]: blk_thresh
0x5692	AVG WHT THRESH	0xFF	RW	Bit[7:0]: wht_thresh

5.21 TV encoder

table 5-21 TV encoder registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x6400	WHITE LEVEL	0xC8	RW	Bit[7:0]: White level
0x6401	NORMAL LEVEL	0x46 (NTSC) 0x3F (PAL)	RW	Bit[7:0]: Normal level
0x6402	BLANK LEVEL	0x3C (NTSC) 0x3F (PAL)	RW	Bit[7:0]: Blank level
0x6403	SYNC LEVEL	0x04	RW	Bit[7:0]: Sync level
0x6404	BURST LEVEL	0x23	RW	Bit[7:0]: Burst level
0x6405	MAX LEVEL	0xFF	RW	Bit[7:0]: Maximum level
0x6406	CHROMA SAT	0x7F	RW	Bit[7]: Reserved Bit[6:0]: Chroma saturation
0x6407	MOD SHIFT	0x25 (NTSC) 0x26 (PAL)	RW	Bit[7:0]: Mode shift[23:16] for burst frequency adjust
0x6408	MOD SHIFT	0x57 (NTSC) 0x79 (PAL)	RW	Bit[7:0]: Mode shift[15:8] For burst frequency adjust
0x6409	MOD SHIFT	0x75 (NTSC) 0x8C (PAL)	RW	Bit[7:0]: Mode shift[7:0] For burst frequency adjust
0x640A	SCUSER	0x80	RW	Bit[7:0]: Sub-carrier clock option Manually set by user
0x640B	SCACT NTSC	0x00	RW	Bit[7:0]: Sub-carrier clock option NTSC default
0x640C	SCACT PAL	0x20	RW	Bit[7:0]: Sub-carrier clock option PAL default
0x640D	TEST MOD	0x00	RW	Bit[7:1]: Reserved Bit[0]: Test mode
0x640E	SIN INS	0x00 (NTSC) 0x0F (PAL)	RW	Bit[7:0]: Sine parameter for burst
0x640F	COS INS	0x00 (NTSC) 0xF3 (PAL)	RW	Bit[7:0]: Cosine parameter for burst
0x6410	MIN LEVEL	0x00 (NTSC) 0x03 (PAL)	RW	Bit[7:0]: Minimum level
0x6411	COEF Y HIGH	0x52 (NTSC) 0x57 (PAL)	RW	Bit[7:0]: Coefficient Y high

table 5-21 TV encoder registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x6412	COEF U HIGH	0x54 (NTSC) 0x59 (PAL)	RW	Bit[7:0]: Coefficient U high
0x6413	COEF V HIGH	0x54 (NTSC) 0x59 (PAL)	RW	Bit[7:0]: Coefficient V high
0x6414	COEF YUV LOW	0x02	RW	Bit[7:0]: Coefficient Y low
0x6415	Y OFFSET	0x00	RW	Bit[7:1]: Reserved Bit[0]: Y offset
0x6416	CBAR EN	0x00	RW	Bit[7:1]: Reserved Bit[0]: Encoder color bar enable
0x6417	FILTER CTRL	0x05 (NTSC) 0x85 (PAL)	RW	Bit[7:0]: Encoder low pass filter control
0x6418	HSYNC LENGTH	0x74 (NTSC) 0x8C (PAL)	RW	Bit[7:0]: HSYNC length
0x6419	BURST LENG	0x40 (NTSC) 0x42 (PAL)	RW	Bit[7]: Reserved Bit[6:0]: Burst length
0x641A	FPORCH LENG	0x28	RW	Bit[7:6]: Reserved Bit[5:0]: Fporch length
0x641B	BPORCH LENG	0x0E (NTSC) 0x1C (PAL)	RW	Bit[7:6]: Reserved Bit[5:0]: Bporch length

6 image sensor output interface digital functions

6.1 TV mode

6.1.1 timing diagrams

figure 6-1 NTSC timing diagram

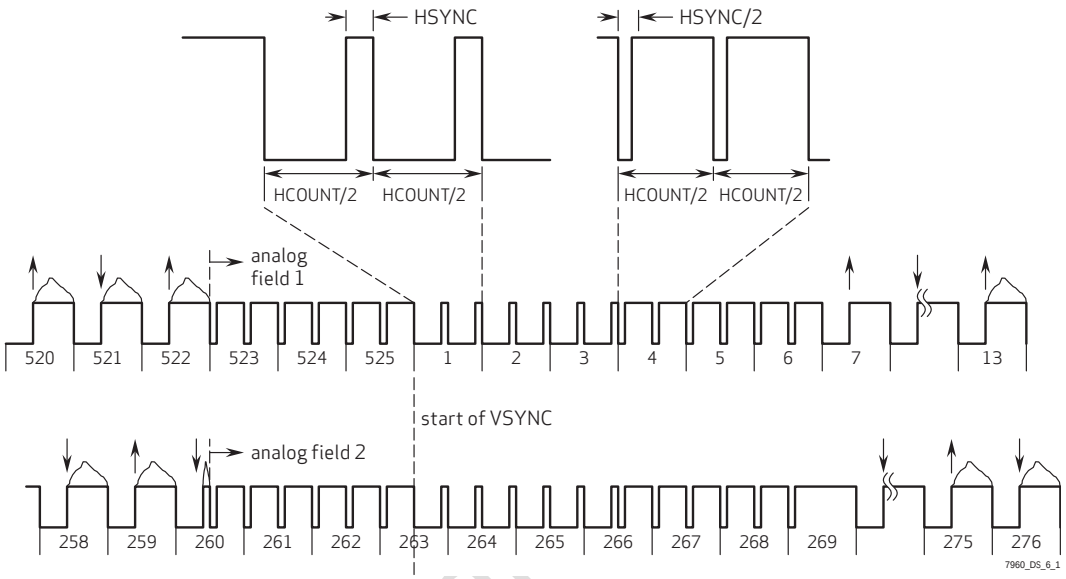
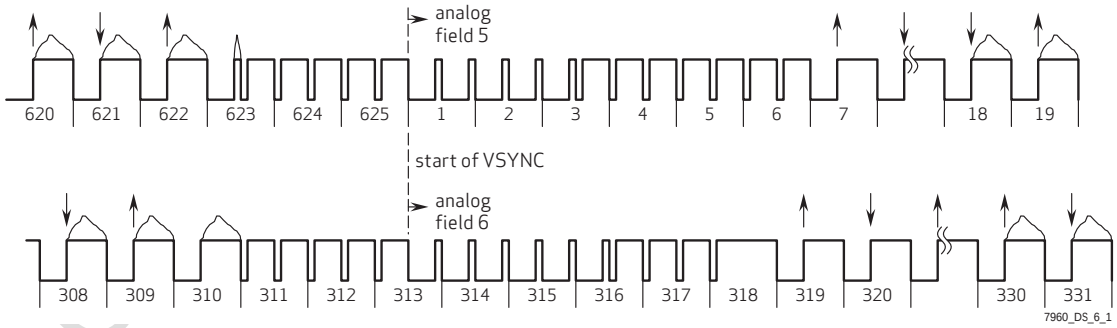


figure 6-2 PAL timing diagram



6.1.2 composite video signals

figure 6-3 NTSC composite video signal

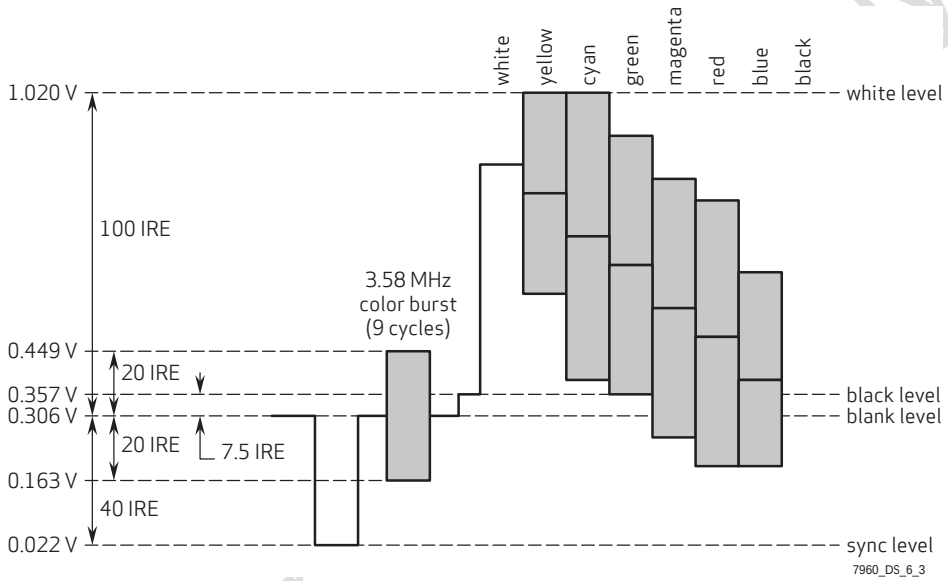
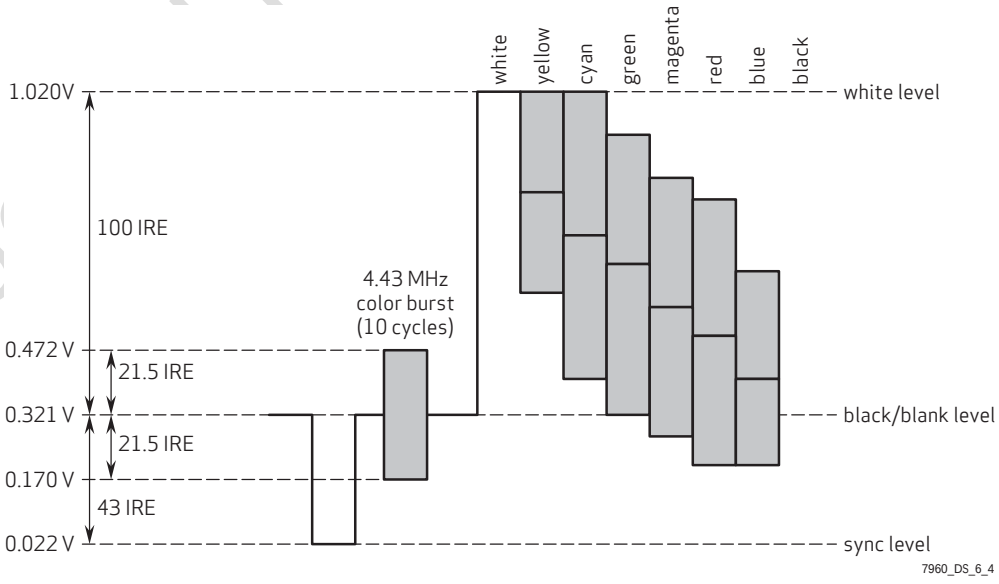


figure 6-4 PAL composite video signal



6.2 digital video port (DVP)

6.2.1 overview

DVP supports RAW, RGB565, RGB666 and YUV422 data formats. It also supports HREF mode, HSYNC mode and ITU656 timing.

The VSYNC, HREF and PCLK have programmable polarity. The DVP data can be clipped by a programmable low boundary and high boundary. Also, the DVP data bits can be switched from 9:0 to 0:9 and from 9:2 to 2:9. The DVP data has options to right shift 1 and 2 bits while high bits will be set to low. For blackout video, the DVP data has an option to output all 0.

HSYNC mode supports maximum 8 dummy pixels in front of each line and 8 dummy pixels at the end of each line.

HSYNC and ITU656 timing is only available at full resolution and sub-sample mode. As long as scaling is enabled, HSYNC and ITU656 mode should be disabled.

The period of the horizontal blank prior to the first valid line may be different from other horizontal blank periods in HSYNC timing.

The horizontal blanking time may be different from line to line during the whole frame when scaling function is enabled. In full or sub-sample mode, all the horizontal and vertical blanking times are the same for every frame.

ITU656 timing needs to support external TV encoder chip for both NTSC and PAL.

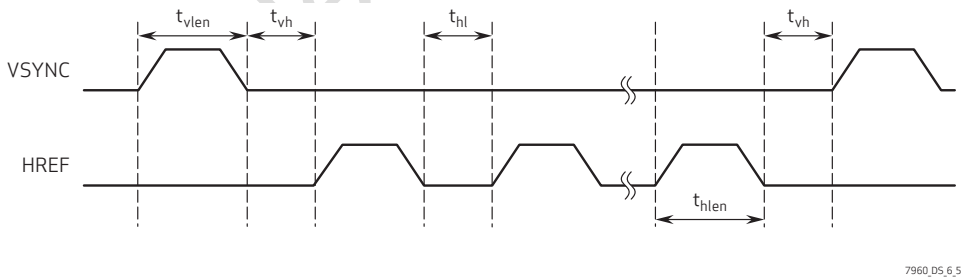
The DVP pins will be tri-state after power on. Users need to set registers to enable normal DVP function. Power down direction and output value are register programmable. VSYNC and HREF can be programmed to GPIO.

DVP supports master and slave mode.

6.2.2 HREF mode

HREF mode is the default mode of DVP. Every VSYNC indicates a frame start and data is valid when HREF is high.

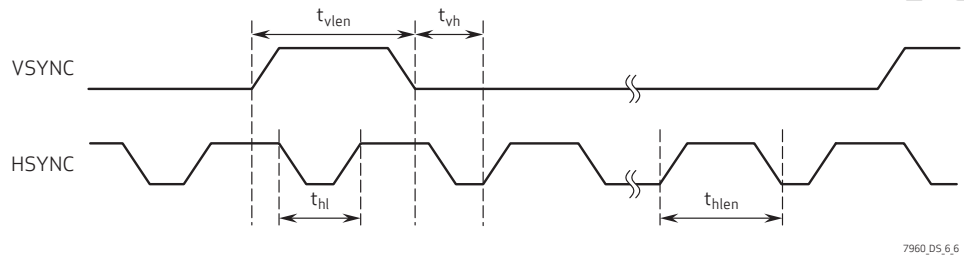
figure 6-5 HREF mode



note t_{vh}, t_{hv}, t_{hlen}, t_{vlen}, and t_{hl} are fixed every frame at full resolution or sensor sub-sample mode, with arbitrary windowing.
t_{vh} could be different by different ISP setting.
t_{hl} could be different in the same frame if scaling function is enabled.

6.2.3 HSYNC mode

figure 6-6 HSYNC mode

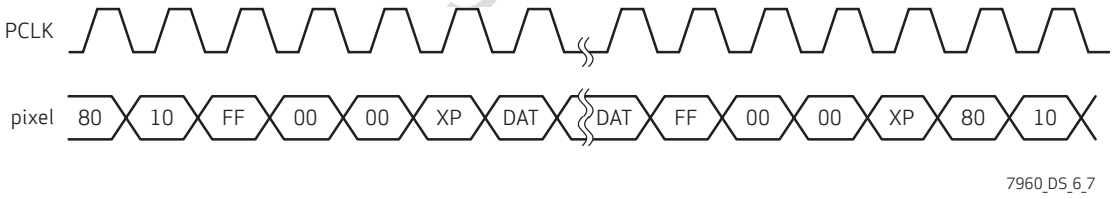


note t_{vh}, t_{heln}, t_{vlen}, and t_{hl} are fixed every frame at full resolution or sensor sub-sample mode, with arbitrary windowing.

6.2.4 CCIR656 mode

The OV7960/OV7461 supports standard CCIR656. Write to register 0x4720[0] to enable CCIR656 mode.

figure 6-7 CCIR656 timing



note XP: {1, F, V, H, P[3:0]}

	1	F	V	H	P3	P2	P1	P0		1	F	V	H	P3	P2	P1	P0
F: 0 is field1, 1 is field 2	1	0	0	0	0	0	0	0		1	1	0	0	0	1	1	1
V: 1 for field blanking, 0 for else	1	0	0	1	1	1	0	1		1	1	0	1	1	0	1	0
H: 0 in SAV, 1 in EAV	1	0	1	0	1	0	1	1		1	1	1	0	1	1	0	0
P[3:0]: protect bits	1	0	1	1	0	1	1	0		1	1	1	1	0	0	0	1

figure 6-8 DVP timing diagram

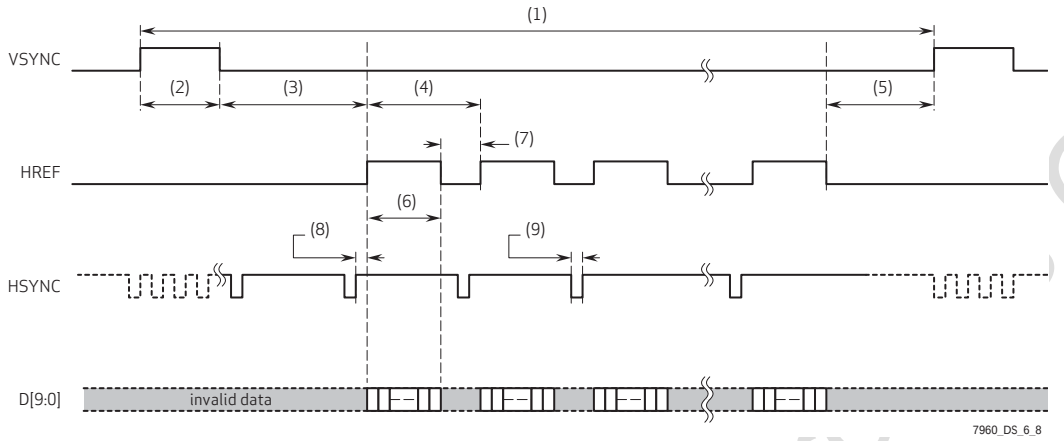


table 6-1 DVP timing specifications

mode	timing
WVGA 752x480	(1) 449072 tp (508 lines) (2) 1768 tp (2 lines) (3) 14424 tp (4) 884 tp (5) 8692 tp (6) 752 tp (7) 132 tp (8) 25 tp (9) 64 tp
VGA 640x480	(1) 400336 tp (524 lines) (2) 1528 tp (2 lines) (3) 14032 tp (4) 764 tp (5) 18180 tp (6) 640 tp (7) 124 tp (8) 25 tp (9) 64 tp
QVGA 320x240	(1) 100084 tp (262 lines) (2) 764 tp (2 lines) (3) 3578 tp (4) 382 tp (5) 4124 tp (6) 320 tp (7) 62 tp (8) 77 tp (9) 16 tp

note
The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-2 DVP registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4700	SHP MAN	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: sh_p_man[11:8]
0x4701	SHP MAN	0x00	RW	Bit[7:0]: sh_p_man[7:0]
0x4702	SHL MAN	0x00	RW	Bit[7]: Reserved Bit[6:0]: sh_l_man[14:8]
0x4703	SVL MAN	0x02	RW	Bit[7:0]: sv_l_man[7:0]
0x4704	SVP MAN	0x00	RW	Bit[7:4]: Reserved Bit[3:0]: sv_p_man[11:8]
0x4705	SVP MAN	0x00	RW	Bit[7:0]: sv_p_man[7:0]
0x4706	HVP MAN	0x02	RW	Bit[7:4]: Reserved Bit[3:0]: hv_p_man[11:8]
0x4707	HVP MAN	0x88	RW	Bit[7:0]: hv_p_man[7:0]
0x4708	HVL MAN	0x0F	RW	Bit[7:0]: hv_l_man
0x4709	VSL MAN	0x04	RW	Bit[7:0]: vs_l_man
0x470A	LL VSP MAN	0x00	RW	Bit[7:5]: Reserved Bit[4]: ll_man[16] Bit[3:0]: vs_p_man[11:8]
0x470B	VSP MAN	0x01	RW	Bit[7:0]: vs_p_man[7:0]
0x470C	LL MAN	0x03	RW	Bit[7:0]: ll_man[15:8]
0x470D	LL MAN	0x0C	RW	Bit[7:0]: ll_man[7:0]
0x470E	CCIR CTRL	0x04	RW	Bit[7]: ccir_f_sel Bit[6]: ccir_v_sel Bit[5:0]: ccir_f_num
0x470F	VREF OFFSET	0x01	RW	Bit[7:4]: vref_end_offset Bit[3:0]: vref_offset
0x4710	VREF ADJ	0x00	RW	Bit[7:4]: vref_end_adj Bit[3:0]: vref_st_adj
0x4711	PADL CNT	0x00	RW	Bit[7:0]: padl_cnt
0x4712	PADR CNT	0x00	RW	Bit[7:0]: padr_cnt
0x4713	VREF ST	0x0A	RW	Bit[7:0]: vref_st[7:0]
0x4714	VREF END	0x00	RW	Bit[7:0]: vref_end[7:0]
0x4715	VREF ENDST	0x10	RW	Bit[7:4]: vref_end[11:8] Bit[3:0]: vref_st[11:8]

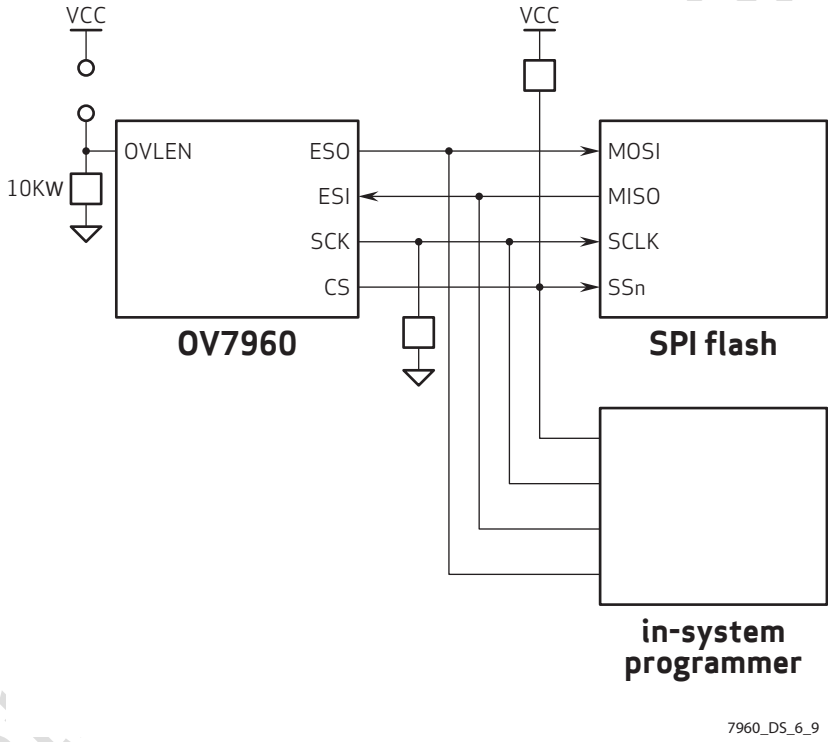
table 6-2 DVP registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4716	FREF ST	0x00	RW	Bit[7:0]: fref_st[7:0]
0x4717	FIELDVST FREFST	0x11	RW	Bit[7:4]: field_vst[11:8] Bit[3:0]: fref_st[11:8]
0x4718	FIELD VST	0x00 (NTSC) 0x2C (PAL)	RW	Bit[7:0]: field_vst[7:0]
0x4719	FIELD HST	0x21 (NTSC) 0x3F (PAL)	RW	Bit[7:0]: field_hst[7:0]
0x471A	FIELD HST	0x02	RW	Bit[7:0]: field_hst[15:8]

6.3 overlay

6.3.1 hardware connection

figure 6-9 in-system programmer



On the hardware level, the connection from OV7960/OV7461 to serial flash is simply standard SPI. The OV7960/OV7461 supports in-system programming of SPI flash. Pull down pin 43 (OVLEN) and all four pins on the SPI port will be tri-stated, thus enabling an external downloader to program the flash.

6.3.2 internal overlay structure

The overlay image is read-in from SPI flash on a line-by-line, on-demand basis. Once inside, it is decompressed and mixed with pixel data. Up to four overlay images can be mixed in succession to produce the final output.

figure 6-10 overlay channels

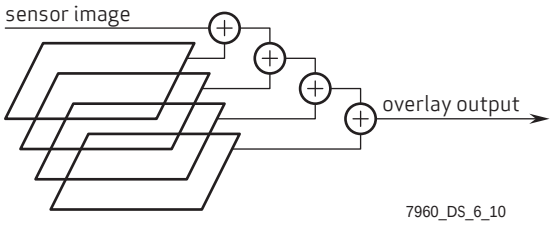
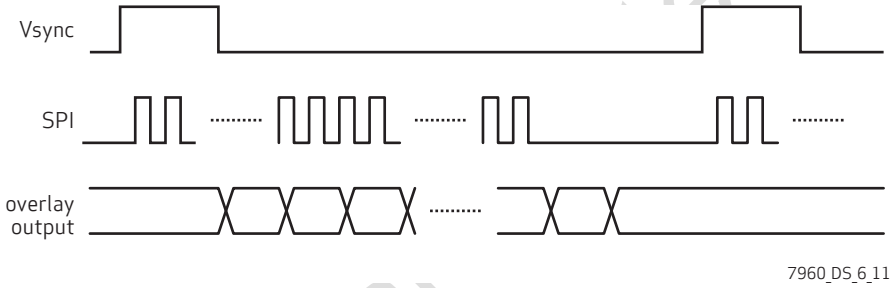


figure 6-11 relative timing



6.3.3 flash memory structure

The memory structure supports compressed overlay images in a proprietary 7-bit RLE format. It also supports the storage of boot ROM, application firmware, and register settings. The total number of images + boot ROM + register settings cannot exceed 1024.

table 6-3 overlay registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x6200	OSD_CTRL00	0x80	RW	Bit[7:6]: r_addr_byte 00: 1 byte address space of SPI EEPROM 01: 2 byte address space of SPI EEPROM 10: 3 byte address space of SPI EEPROM 11: 4 byte address space of SPI EEPROM Bit[5]: sclk_pol 0: Do not reverse spi_sclk_o 1: Reverse spi_sclk_o Bit[4:0]: spi_spd 0: Set SCK as system clock speed 1: Two clock is one spi_sck....
0x6201	OSD_CTRL01	0x02	RW	Bit[7]: eof_clr 0: Use EOF to reset the whole module 1: Use SOF to reset the whole module Bit[6]: grp_hld 0: Registers will take effect 1: Registers will hold Bit[5]: Reserved Bit[4:0]: spi_dly SPI delay for every command, unit is system clock cycle
0x6202	OSD_CTRL02	0x3F	RW	Bit[7]: sccb_acc 0: SCCB does not access SPI bus 1: SCCB access SPI bus Bit[6]: r_wr_en 0: sccb_wdata is not output 1: sccb_wdata is output Bit[5]: r_fast_rd Bit[4:0]: r_seq_nu OSD_SEQ number

table 6-3 overlay registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x6203	OSD_CTRL03	0x0B	RW	Bit[7:0]: Fast read instruction
0x6204	OSD_CTRL04	0x03	RW	Bit[7:0]: Normal read instruction
0x6205	OSD_CTRL05	0x03	RW	Bit[7:0]: index_l for layer 0
0x6206	OSD_CTRL06	0x04	RW	Bit[7:0]: index_l for layer 1
0x6207	OSD_CTRL07	0x03	RW	Bit[7:0]: index_l for layer 2
0x6208	OSD_CTRL08	0x04	RW	Bit[7:0]: index_l for layer 3
0x6209	OSD_CTRL09	0x00	RW	Bit[7:6]: index_h for layer 3 Bit[5:4]: index_h for layer 2 Bit[3:2]: index_h for layer 1 Bit[1:0]: index_h for layer 0
0x620A	OSD_CTRL0A	0x01	RW	Bit[7:6]: Resolution for layer 3 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[5:4]: Resolution for layer 2 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[3:2]: Resolution for layer 1 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay Bit[1:0]: Resolution for layer 0 00: No overlay 01: 1x1 overlay 10: 2x2 overlay 11: 4x4 overlay
0x620B	OSD_CTRL0B	0x00	RW	Bit[7:0]: x_start_add_l for layer 0
0x620C	OSD_CTRL0C	0x00	RW	Bit[7:0]: y_start_add_l for layer 0

table 6-3 overlay registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x620D	OSD_CTRL0D	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 0 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 0 Bit[3]: Sign bit of y_start_addr for layer 0 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 0
0x620E	OSD_CTRL0E	0x00	RW	Bit[7:0]: x_start_add_l for layer 1
0x620F	OSD_CTRL0F	0x00	RW	Bit[7:0]: y_start_add_l for layer 1
0x6210	OSD_CTRL10	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 1 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 1 Bit[3]: Sign bit of y_start_addr for layer 1 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 1
0x6211	OSD_CTRL11	00x0	RW	Bit[7:0]: x_start_add_l for layer 2
0x6212	OSD_CTRL12	0x00	RW	Bit[7:0]: y_start_add_l for layer 2
0x6213	OSD_CTRL13	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 2 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 2 Bit[3]: Sign bit of y_start_addr for layer 2 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 2
0x6214	OSD_CTRL14	0x00	RW	Bit[7:0]: x_start_add_L for layer 3
0x6215	OSD_CTRL15	0x00	RW	Bit[7:0]: y_start_add_L for layer 3

table 6-3 overlay registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x6216	OSD_CTRL16	0x00	RW	Bit[7]: Sign bit of x_start_addr for layer 3 0: Positive 1: Negative Bit[6:4]: High bits of x_start_addr for layer 3 Bit[3]: Sign bit of y_start_addr for layer 3 0: Positive 1: Negative Bit[2:0]: High bits of y_start_addr for layer 3
0x6217	OSD_CTRL17	0x00	RW	Bit[7:0]: sccb_wdata
0x6218	OSD_CTRL18	0xE4	RW	Bit[7:6]: lay3_sel Bit[5:4]: lay2_sel Bit[3:2]: lay1_sel Bit[1:0]: lay0_sel
0x6219	OSD_CTRL19	0x00	RW	Bit[7:0]: r_ld_index
0x621A	OSD_CTRL1A	0x00	RW	Bit[7]: r_automovy_en3 Bit[6]: r_automovy_en2 Bit[5]: r_automovy_en1 Bit[4]: r_automovy_en0 Bit[3]: r_automovx_en3 Bit[2]: r_automovx_en2 Bit[1]: r_automovx_en1 Bit[0]: r_automovx_en0
0x621B	OSD_CTRL1B	0x00	RW	Bit[7]: r_automovy_wrap_en3 Bit[6]: r_automovy_wrap_en2 Bit[5]: r_automovy_wrap_en1 Bit[4]: r_automovy_wrap_en0 Bit[3]: r_automovx_wrap_en3 Bit[2]: r_automovx_wrap_en2 Bit[1]: r_automovx_wrap_en1 Bit[0]: r_automovx_wrap_en0
0x621C	OSD_CTRL1C	0x02	RW	Bit[7]: r_automv_step_sel Bit[6]: r_field_pol Bit[5]: r_spi_seln Bit[4]: r_ld_pad_dis Bit[3]: r_pon_ld_dis Bit[2]: r_fo_empty_clr Bit[1:0]: r_retry
0x621D	OSD_CTRL1D	0x10	RW	Bit[7:0]: r_tog_cnt
0x621E	OSD_CTRL1E	0xFF	RW	Bit[7:0]: r_seq_nu

table 6-3 overlay registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x621F	OSD_CTRL1F	0x04	RW	Bit[7]: r_read_once0 Bit[6]: r_read_once1 Bit[5]: r_read_once2 Bit[4]: r_read_once3 Bit[3]: Reserved Bit[2]: r_retry_pon Bit[1]: r_interlace_dis Bit[0]: r_ld_blank
0x6220	OSD_CTRL20	0x00	RW	Bit[7]: r_autochg_wrap_en3 Bit[6]: r_autochg_wrap_en2 Bit[5]: r_autochg_wrap_en1 Bit[4]: r_autochg_wrap_en0 Bit[3]: r_autochg_en3 Bit[2]: r_autochg_en2 Bit[1]: r_autochg_en1 Bit[0]: r_autochg_en0
0x6221	OSD_CTRL21	0x00	RW	Bit[7:0]: r_autochg_stidx0[7:0]
0x6222	OSD_CTRL22	0x00	RW	Bit[7:0]: r_autochg_edidx0[7:0]
0x6223	OSD_CTRL23	0x00	RW	Bit[7:0]: r_autochg_stidx1[7:0]
0x6224	OSD_CTRL24	0x00	RW	Bit[7:0]: r_autochg_edidx1[7:0]
0x6225	OSD_CTRL25	0x00	RW	Bit[7:0]: r_autochg_stidx2[7:0]
0x6226	OSD_CTRL26	0x00	RW	Bit[7:0]: r_autochg_edidx2[7:0]
0x6227	OSD_CTRL27	0x00	RW	Bit[7:0]: r_autochg_stidx3[7:0]
0x6228	OSD_CTRL28	0x00	RW	Bit[7:0]: r_autochg_edidx3[7:0]
0x6229	OSD_CTRL29	0x00	RW	Bit[7:6]: r_autochg_edidx1[9:8] Bit[5:4]: r_autochg_stidx1[9:8] Bit[3:2]: r_autochg_edidx0[9:8] Bit[1:0]: r_autochg_stidx0[9:8]
0x622A	OSD_CTRL2A	0x00	RW	Bit[7:6]: r_autochg_edidx3[9:8] Bit[5:4]: r_autochg_stidx3[9:8] Bit[3:2]: r_autochg_edidx2[9:8] Bit[1:0]: r_autochg_stidx2[9:8]
0x622B	OSD_CTRL2B	0x00	RW	Bit[7:0]: r_autochg_step[7:0]
0x622C	OSD_CTRL2C	0x00	RW	Bit[7:0]: r_autochg_step[15:8]

7 register tables

The following table provides a preliminary description of the device control registers contained in the OV7960/OV7461. Descriptions of additional registers will be released at a later date.

table 7-1 ISP control (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	ISP CONTROL 00	0xDF	RW	ISP Control 00 Bit[7]: LENC correction enable 0: Disable 1: Enable Bit[6]: Gamma (in YUV domain) enable 0: Disable 1: Enable Bit[5]: RAW gamma enable 0: Disable 1: Enable Bit[4]: Even odd removing enable 0: Disable 1: Enable Bit[3]: De-noise enable 0: Disable 1: Enable Bit[2]: Black pixel cancellation enable 0: Disable 1: Enable Bit[1]: White pixel cancellation enable 0: Disable 1: Enable Bit[0]: Color interpolation (CIP) enable 0: Disable 1: Enable

table 7-1 ISP control (sheet 2 of 4)

address	register name	default value	R/W	description
0x5001	ISP CONTROL 01	0x4F	RW	ISP Control 01 Bit[7]: Special digital effects (SDE) enable 0: Disable 1: Enable Bit[6]: Auto color saturation adjust enable 0: Disable 1: Enable Bit[5]: Vertical scaling enable 0: Disable 1: Enable Bit[4]: Horizontal scaling enable 0: Disable 1: Enable Bit[3]: Auto contrast enable 0: Disable 1: Enable Bit[2]: UV average enable 0: Disable 1: Enable Bit[1]: Color matrix enable 0: Disable 1: Enable Bit[0]: Auto white balance (AWB) enable 0: Disable 1: Enable
0x5002	ISP CONTROL 02	0xE0	RW	ISP Control 02 Reserved
0x5003	ISP CONTROL 03	0xA8	RW	ISP Control 03 Bit[7]: Pad in buffer control enable 0: Buffer control boundary padded external 1: Buffer control pad boundary internal Bit[6:4]: Reserved Bit[3]: YUV to YCbCr enable 0: Disable 1: Enable Bit[2:1]: Reserved Bit[0]: Color bar test pattern enable 0: Disable 1: Enable
0x5004	ISP CONTROL 04	0x08	RW	ISP Control 04 Bit[7:3]: Reserved Bit[2]: Bar move enable 0: Disable 1: Enable Bit[1:0]: Color bar style

table 7-1 ISP control (sheet 3 of 4)

address	register name	default value	R/W	description
0x5005	ISP CONTROL 05	0xDC	RW	ISP Control 05 Bit[7]: Raw gamma option 1 0: Does not add back BLC bias after raw gamma correction 1: Adds back BLC bias after raw gamma correction Bit[6]: Raw gamma option 2 0: Raw gamma applied on input data directly regardless of the black level 1: Subtract black level before applying raw gamma Bit[5]: UV average old style enable 0: Disable 1: Enable Bit[4]: Advanced AWB option 1 0: Do not subtract black level 1: Subtract black level before statistics and apply gain Bit[3]: Lens correction option 1 0: Does not add back BLC bias after lens correction 1: Adds back BLC bias after lens correction Bit[2]: Lens correction option 2 0: Lens correction applied on input data directly regardless of the black level 1: Subtract black level before applying lens correction Bit[1:0]: Reserved
0x5006~ 0x5023	RSVD	–	–	Reserved
0x5024	ISP CONTROL 36	0x80	RW	ISP Control 36 Bit[7]: Reserved Bit[6]: Rgma manual mode 0: Use internal divider result for SLPH 1: Use register for SLPH Bit[5:0]: Reserved
0x5025~ 0x507F	RSVD	–	–	Reserved
0x5080	EVEN CONTROL 00	0x40	RW	Bit[7:0]: Threshold for the difference between the adjacent pixel in the same channel. Value should be less than half of black level.

table 7-1 ISP control (sheet 4 of 4)

address	register name	default value	R/W	description
0x5081	EVEN CONTROL 01	0x00	RW	Bit[7:6]: Not used Bit[5:1]: Reserved Bit[0]: Manual mode enable
0x5082	EVEN CONTROL 02	0x00	RW	Bit[7:0]: Manual compensation on B pixel on left side of Gb pixel in 10-bit scale
0x5083	EVEN CONTROL 03	0x00	RW	Bit[7:0]: Manual compensation on B pixel on right side of Gb pixel in 10-bit scale
0x5084	EVEN CONTROL 04	0x00	RW	Bit[7:0]: Manual compensation on Gb pixel on left side of B pixel in 10-bit scale
0x5085	EVEN CONTROL 05	0x00	RW	Bit[7:0]: Manual compensation on Gb pixel on right side of B pixel in 10-bit scale
0x5086	EVEN CONTROL 06	0x00	RW	Bit[7:0]: Manual compensation on Gr pixel on left side of R pixel in 10-bit scale
0x5087	EVEN CONTROL 07	0x00	RW	Bit[7:0]: Manual compensation on Gr pixel on right side of R pixel in 10-bit scale
0x5088	EVEN CONTROL 08	0x00	RW	Bit[7:0]: Manual compensation on R pixel on left side of Gr pixel in 10-bit scale
0x5089	EVEN CONTROL 09	0x00	RW	Bit[7:0]: Manual compensation on R pixel on right side of Gr pixel in 10-bit scale
0x508A	EVEN CONTROL 10	0x00	RW	Debug Mode Changing this value is not allowed
0x508B	EVEN MINIMAL NUMBER MANUAL SETTING	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Pixel number[18:16] threshold that triggers compensation update
0x508C	EVEN MINIMAL NUMBER MANUAL SETTING	0x01	RW	Bit[7:0]: Pixel number[15:8] threshold that triggers compensation update
0x508D	EVEN MINIMAL NUMBER MANUAL SETTING	0x00	RW	Bit[7:0]: Pixel number[7:0] threshold that triggers compensation update
0x508E~ 0x5095	EVEN DEBUG INFO	–	R	Debug Information

table 7-2 LENC control (sheet 1 of 4)

address	register name	default value	R/W	description
0x5100	LENC RED X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: red_x0[9:8] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5101	LENC RED X0	0x0C	RW	Bit[7:0]: red_x0[7:0] X coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5102	LENC RED Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: red_y0[9:8] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5103	LENC RED Y0	0x06	RW	Bit[7:0]: red_y0[7:0] Y coordinate of the lens optical center for red channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5104	LENC RED A1	0x22	RW	LENC Control 04 Bit[7]: Not used Bit[6:0]: red_a1[6:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5105	LENC RED A2	0x07	RW	LENC Control 05 Bit[7:4]: Not used Bit[3:0]: red_a2[3:0] Composed of the first group of factors used in the LENC correction of the red color channels
0x5106	LENC RED B1	0xC2	RW	LENC Control 06 Bit[7:0]: red_b1[7:0] Composed of the second group of factors used in the LENC correction of the red color channels
0x5107	LENC RED B2	0x08	RW	LENC Control 07 Bit[7:4]: Not used Bit[3:0]: red_b2[3:0] Composed of the second group of factors used in the LENC correction of the red color channels

table 7-2 LENC control (sheet 2 of 4)

address	register name	default value	R/W	description
0x5108	LENC GREEN X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: green_x0[9:8] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5109	LENC GREEN X0	0x0C	RW	Bit[7:0]: green_x0[7:0] X coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x510A	LENC GREEN Y0	0x03	RW	Bit[7:2]: Not used Bit[1:0]: green_y0[9:8] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x510B	LENC GREEN Y0	0x06	RW	Bit[7:0]: green_y0[7:0] Y coordinate of the lens optical center for green channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x510C	LENC GREEN A1	0x22	RW	LENC Control 12 Bit[7]: Not used Bit[6:0]: green_a1[6:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510D	LENC GREEN A2	0x07	RW	LENC Control 13 Bit[7:4]: Not used Bit[3:0]: green_a2[3:0] Composed of the first group of factors used in the LENC correction of the green color channels
0x510E	LENC GREEN B1	0xC2	RW	LENC Control 14 Bit[7:0]: green_b1[7:0] Composed of the second group of factors used in the LENC correction of the green color channels
0x510F	LENC GREEN B2	0x08	RW	LENC Control 15 Bit[7:4]: Not used Bit[3:0]: green_b2[3:0] Composed of the second group of factors used in the LENC correction of the green color channels

table 7-2 LENC control (sheet 3 of 4)

address	register name	default value	R/W	description
0x5110	LENC BLUE X0	0x04	RW	Bit[7:2]: Not used Bit[1:0]: blue_x0[9:8] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5111	LENC BLUE X0	0x0C	RW	Bit[7:0]: blue_x0[7:0] X coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 2047
0x5112	LENC BLUE Y0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: blue_y0[11:8] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5113	LENC BLUE Y0	0x06	RW	Bit[7:0]: blue_y0[7:0] Y coordinate of the lens optical center for blue channel relative to the left-top corner of the ISP input image Range is 0 ~ 1535
0x5114	LENC BLUE A1	0x22	RW	LENC Control 20 Bit[7]: Not used Bit[6:0]: blue_a1[6:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5115	LENC BLUE A2	0x07	RW	LENC Control 21 Bit[7:4]: Not used Bit[3:0]: blue_a2[3:0] Composed of the first group of factors used in the LENC correction of the blue color channels
0x5116	LENC BLUE B1	0xC2	RW	LENC Control 22 Bit[7:0]: blue_b1[7:0] Composed of the second group of factors used in the LENC correction of the blue color channels
0x5117	LENC BLUE B2	0x08	RW	LENC Control 23 Bit[7:4]: Not used Bit[3:0]: blue_b2[3:0] Composed of the second group of factors used in the LENC correction of the blue color channels

table 7-2 LENC control (sheet 4 of 4)

address	register name	default value	R/W	description
0x5118	LENC XSTARTH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: X coordinate of the lens starting point high bit
0x5119	LENC XSTARTL	0x00	RW	Bit[7:0]: X coordinate of the lens starting point low bit
0x511A	LENC YSTARTH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Y coordinate of the lens starting point high bit
0x511B	LENC YSTARTL	0x00	RW	Bit[7:0]: Y coordinate of the lens starting point low bit
0x511C	LENC CONTROL 24	0x80	RW	LENC Control 24 Bit[7]: round_en Determines whether or not to round off the last two bits of the LENC input data 0: Do not round off the last two bits 1: Round off the last two bits Bit[6]: Debug mode Changing this value is not allowed Bit[5]: Sensor gain coefficient manual control (only when 0x5118[4]=1) 0: Use 0x80 as lens correction coefficient threshold 1 1: Use register 0x511C as lens correction coefficient threshold 1 Bit[4]: Coefficient manual control 0: Manual control coefficients 1: Automatically compute coefficients Bit[3:2]: Horizontal skip mode Valid only when the image size is not full size 00: Does not skip a pixel 01: Skips 1 pixel every 2 pixels 10: Skips 3 pixels every 4 pixels 11: Skips 7 pixels every 8 pixels Bit[1:0]: Vertical skip mode 00: Does not skip line 01: Skips 1 line every 2 lines 10: Skips 3 lines every 4 lines 11: Skips 7 lines every 8 lines
0x511D	LENC CONTROL 25	0x00	RW	Bit[7:0]: Reserved

table 7-3 WBC control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5290	DNS CONTROL 00	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Coefficient of Y de-noise threshold with respect to Y
0x5291	DNS CONTROL 01	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Coefficient of UV de-noise threshold with respect to Y
0x5292	DNS CONTROL 02	0x00	RW	Bit[7:1]: Not used Bit[0]: De-noise and sharpness manual mode enable 0: Auto 1: Manual
0x5293	NOISE Y	0x02	RW	Bit[7:0]: noise_y De-noise weight for Y
0x5294	NOISE U	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise U high byte De-noise weight for UV
0x5295	NOISE U	0x02	RW	Bit[7:0]: Noise U low byte De-noise weight for UV
0x5296	NOISE V	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise V high byte De-noise weight for UV
0x5297	NOISE V	0x02	RW	Bit[7:0]: Noise V low byte De-noise weight for UV
0x5298	DNS EDGETHRE	0x06	RW	Bit[7:0]: DNS edgethre Edge threshold for UV smoothing
0x5299	DNS GBGR EXTRA	0x04	RW	Bit[7:0]: DNS CbCr extra De-noise threshold adjustment for Cb and Cr
0x529A	NOISE Y LIST 0	0x02	RW	Bit[7:0]: Noise Y list0[7:0] Noise Y threshold at 1x sensor gain
0x529B	NOISE Y LIST 1	0x04	RW	Bit[7:0]: Noise Y list1[7:0] Noise Y threshold at 2x sensor gain
0x529C	NOISE Y LIST 2	0x08	RW	Bit[7:0]: Noise Y list2[7:0] Noise Y threshold at 4x sensor gain
0x529D	NOISE Y LIST 3	0x14	RW	Bit[7:0]: Noise Y list03[7:0] Noise Y threshold at 8x sensor gain
0x529E	NOISE Y LIST 4	0x1E	RW	Bit[7:0]: Noise Y list4[7:0] Noise Y threshold at 16x sensor gain

table 7-3 WBC control (sheet 2 of 3)

address	register name	default value	R/W	description
0x529F	NOISE Y LIST 5	0x28	RW	Bit[7:0]: Noise Y list5[7:0] Noise Y threshold at 32x sensor gain
0x52A0	NOISE Y LIST 6	0x32	RW	Bit[7:0]: Noise Y list6[7:0] Noise Y threshold at 64x sensor gain
0x52A1	NOISE Y LIST 7	0x32	RW	Bit[7:0]: Noise Y list7[7:0] Noise Y threshold at 64x sensor gain
0x52A2	NOISE UV LIST 0	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list0[8] Noise UV threshold at 1x sensor gain
0x52A3	NOISE UV LIST 0	0x02	RW	Bit[7:0]: Noise UV list0[7:0] Noise UV threshold at 1x sensor gain
0x52A4	NOISE UV LIST 1	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list1[8] Noise UV threshold at 2x sensor gain
0x52A5	NOISE UV LIST 1	0x04	RW	Bit[7:0]: Noise UV list1[7:0] Noise UV threshold at 2x sensor gain
0x52A6	NOISE UV LIST 2	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list2[8] Noise UV threshold at 4x sensor gain
0x52A7	NOISE UV LIST 2	0x0C	RW	Bit[7:0]: Noise UV list2[7:0] Noise UV threshold at 4x sensor gain
0x52A8	NOISE UV LIST 3	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list3[8] Noise UV threshold at 8x sensor gain
0x52A9	NOISE UV LIST 3	0x28	RW	Bit[7:0]: Noise UV list3[7:0] Noise UV threshold at 8x sensor gain
0x52AA	NOISE UV LIST 4	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list4[8] Noise UV threshold at 16x sensor gain
0x52AB	NOISE UV LIST 4	0x32	RW	Bit[7:0]: Noise UV list4[7:0] Noise UV threshold at 16x sensor gain
0x52AC	NOISE UV LIST 5	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list5[8] Noise UV threshold at 32x sensor gain
0x52AD	NOISE UV LIST 5	0x3C	RW	Bit[7:0]: Noise UV list5[7:0] Noise UV threshold at 32x sensor gain
0x52AE	NOISE UV LIST 6	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list6[8] Noise UV threshold at 64x sensor gain

table 7-3 WBC control (sheet 3 of 3)

address	register name	default value	R/W	description
0x52AF	NOISE UV LIST 6	0x4C	RW	Bit[7:0]: Noise UV list6[7:0] Noise UV threshold at 64x sensor gain
0x52B0	NOISE UV LIST 7	0x00	RW	Bit[7:1]: Not used Bit[0]: Noise UV list7[8] Noise UV threshold at 64x sensor gain
0x52B1	NOISE UV LIST 7	0x4C	RW	Bit[7:0]: Noise UV list7[7:0] Noise UV threshold at 64x sensor gain

table 7-4 CIP control (sheet 1 of 3)

address	register name	default value	R/W	description
0x5300	CIP MIN GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cip_mingain[9:8] Minimum real gain for calculation of CIP parameters normalized by 0x10
0x5301	CIP MIN GAIN	0x10	RW	Bit[7:0]: cip_mingain[7:0] Minimum real gain for calculation of CIP parameters normalized by 0x10
0x5302	CIP MAX GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cip_maxgain[9:8] Maximum real gain for calculation of CIP parameters normalized by 0x10
0x5303	CIP MAX GAIN	0x80	RW	Bit[7:0]: cip_maxgain[7:0] Maximum real gain for calculation of CIP parameters normalized by 0x10
0x5304	CIP MIN INTNOISE	0x00	RW	Bit[7:2]: Not used Bit[1:0]: cip_min_intnoise[8] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5305	CIP MIN INTNOISE	0x30	RW	Bit[7:0]: cip_min_intnoise[7:0] CIP de-noise at CIP MIN GAIN. The larger the value, the blurrier the image.
0x5306	CIP MAX INTNOISE	0x01	RW	Bit[7:2]: Not used Bit[1:0]: cip_max_intnoise[8] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.
0x5307	CIP MAX INTNOISE	0x20	RW	Bit[7:0]: cip_max_intnoise[7:0] CIP de-noise at CIP MAX GAIN. The larger the value, the blurrier the image.

table 7-4 CIP control (sheet 2 of 3)

address	register name	default value	R/W	description
0x5308	CIP SHARPEN MASK 0	0x10	RW	Bit[7:0]: cip punsharpen mask0[7:0] (sign + abs) Weight for position 0 and 4 in the 5-point filter when evaluating edge effect
0x5309	CIP SHARPEN MASK 1	0x30	RW	Bit[7:0]: cip punsharpen mask1[7:0] (sign + abs) Weight for position 1 and 3 in the 5-point filter when evaluating edge effect
0x530A	CIP CONTROL 10	0x01	RW	Bit[7:4]: Not used Bit[3]: Manual sharpen and de-noise enable 0: Auto 1: Manual Bit[2:1]: Debug mode Changing this value is not allowed Bit[0]: Anti-aliasing enable 0: Anti-aliasing mode disable 1: Anti-aliasing mode enable
0x530B	CIP CONTROL 11	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Anti-aliasing parameter The larger the value, the stronger the color alias. Changing this value is not recommended.
0x530C	CIP CONTROL 12	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Minimum sharpen[4:0] Sharpening at CIP MAX GAIN
0x530D	CIP CONTROL 13	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: Maximum sharpen[5:0] Sharpening at CIP MIN GAIN
0x530E	CIP CONTROL 14	0x20	RW	Bit[7:6]: Not used Bit[5:0]: Minimum positive edge threshold[5:0] Positive edge threshold for sharpening at CIP MIN GAIN
0x530F	CIP CONTROL 15	0x60	RW	Bit[7:0]: Maximum positive edge threshold[7:0] Positive edge threshold for sharpening at CIP MAX GAIN
0x5310	CIP CONTROL 16	0x20	RW	Bit[7:6]: Not used Bit[5:0]: Minimum negative edge threshold[5:0] Negative edge threshold for sharpening at CIP MIN GAIN
0x5311	CIP CONTROL 17	0x60	RW	Bit[7:0]: Maximum negative edge threshold[7:0] Negative edge threshold for sharpening at CIP MAX GAIN
0x5312	CIP CONTROL 18	0x40	RW	Bit[7:0]: Coefficient of edge threshold with respect to Y

table 7-4 CIP control (sheet 3 of 3)

address	register name	default value	R/W	description
0x5313	CIP CONTROL 19	0x10	RW	Bit[7:5]: Not used Bit[4:0]: Sharpening ratio of negative edge to positive edge normalized by 0x10
0x5314~ 0x5319	CIP CONTROL	–	RW	Color Interpolation Parameters Changing these values is not recommended
0x531A~ 0x5321	CIP CONTROL	–	RW	Manual Sharpness and De-noise Control

table 7-5 contrast control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5400	CONTRAST MAX HIGH LEVEL	0x3F	RW	Bit[7]: Not used Bit[6:0]: Maximum high level[14:8] Maximum high level threshold Changing this value is not recommended
0x5401	CONTRAST MAX HIGH LEVEL	0xFF	RW	Bit[7:0]: Maximum high level[7:0] Maximum high level threshold Changing this value is not recommended
0x5402	CONTRAST MIN HIGH LEVEL	0x3C	RW	Bit[7]: Not used Bit[6:0]: Minimum high level[14:8] Minimum high level threshold in 15-bit scale
0x5403	CONTRAST MIN HIGH LEVEL	0x00	RW	Bit[7:0]: Minimum high level[7:0] Minimum high level threshold in 15-bit scale
0x5404	CONTRAST MAX LOW LEVEL	0x02	RW	Bit[7]: Not used Bit[6:0]: Maximum low level[14:8] Maximum low level threshold in 15-bit scale
0x5405	CONTRAST MAX LOW LEVEL	0x00	RW	Bit[7:0]: Maximum low level[7:0] Maximum low level threshold in 15-bit scale
0x5406	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7]: Not used Bit[6:0]: Minimum low level[14:8] Minimum low level threshold in 15-bit data range
0x5407	CONTRAST MIN LOW LEVEL	0x00	RW	Bit[7:0]: Minimum low level[7:0] Minimum low level threshold in 15-bit data range

table 7-5 contrast control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5408	CONTRAST CURLOWLEVEL	0x01	RW	Bit[7]: Not used Bit[6:0]: Current lowlevel[14:8] Current low level manual setting
0x5409	CONTRAST CURLOWLEVEL	0x00	RW	Bit[7:0]: Current lowlevel[7:0] Current low level manual setting
0x540A	CONTRAST CURHIGHLEVEL	0x3F	RW	Bit[7]: Not used Bit[6:0]: Current highlevel[14:8] Current high level manual setting
0x540B	CONTRAST CURHIGHLEVEL	0xFF	RW	Bit[7:0]: Current highlevel[7:0] Current high level manual setting
0x540C~ 0x540D	NOT USED	–	–	Not Used
0x540E	CONTRAST THRES1	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres1[22:16] Dark pixel number threshold used to determine low level threshold
0x540F	CONTRAST THRES1	0x3A	RW	Bit[7:0]: Thres1[15:8] Dark pixel number threshold used to determine low level threshold
0x5410	CONTRAST THRES1	0x98	RW	Bit[7:0]: Thres1[7:0] Dark pixel number threshold used to determine low level threshold
0x5411	NOT USED	–	–	Not Used
0x5412	CONTRAST THRES2	0x00	RW	Bit[7]: Not used Bit[6:0]: Thres2[22:16] Bright pixel number threshold used to determine high level threshold
0x5413	CONTRAST THRES2	0x3A	RW	Bit[7:0]: Thres2[15:8] Bright pixel number threshold used to determine high level threshold
0x5414	CONTRAST THRES2	0x98	RW	Bit[7:0]: Thres2[7:0] Bright pixel number threshold used to determine high level threshold
0x5415~ 0x541C	DEBUG MODE	–	–	Debug Mode Changing these values is not allowed
0x541D	CONTRAST STEP	0x20	RW	Bit[7:0]: Step[7:0] Step for low and high level adjustment in 15-bit scale
0x541E~ 0x5426	DEBUG MODE	–	–	Debug Mode Changing these values is not allowed

table 7-6 gamma control (sheet 1 of 4)

address	register name	default value	R/W	description
0x5480	GAMMA CTRL00	0x1A	RW	Bit[7:0]: y_list_00 Output at 0x10 (10-bit scale) when register 0x5000[5] = 1
0x5481	GAMMA CTRL01	0x28	RW	Bit[7:0]: y_list_01 Output at 0x20 (10-bit scale) when register 0x5000[5] = 1
0x5482	GAMMA CTRL02	0x3E	RW	Bit[7:0]: y_list_02 Output at 0x40 (10-bit scale) when register 0x5000[5] = 1
0x5483	GAMMA CTRL03	0x5E	RW	Bit[7:0]: y_list_03 Output at 0x80 (10-bit scale) when register 0x5000[5] = 1
0x5484	GAMMA CTRL04	0x6B	RW	Bit[7:0]: y_list_04 Output at 0xA0 (10-bit scale) when register 0x5000[5] = 1
0x5485	GAMMA CTRL05	0x77	RW	Bit[7:0]: y_list_05 Output at 0xC0 (10-bit scale) when register 0x5000[5] = 1
0x5486	GAMMA CTRL06	0x81	RW	Bit[7:0]: y_list_06 Output at 0xE0 (10-bit scale) when register 0x5000[5] = 1
0x5487	GAMMA CTRL07	0x8B	RW	Bit[7:0]: y_list_07 Output at 0x100 (10-bit scale) when register 0x5000[5] = 1
0x5488	GAMMA CTRL08	0x94	RW	Bit[7:0]: y_list_08 Output at 0x120 (10-bit scale) when register 0x5000[5] = 1
0x5489	GAMMA CTRL09	0x9C	RW	Bit[7:0]: y_list_09 Output at 0x140 (10-bit scale) when register 0x5000[5] = 1
0x548A	GAMMA CTRL0A	0xAB	RW	Bit[7:0]: y_list_10 Output at 0x180 (10-bit scale) when register 0x5000[5] = 1
0x548B	GAMMA CTRL0B	0xB8	RW	Bit[7:0]: y_list_11 Output at 0x1C0 (10-bit scale) when register 0x5000[5] = 1
0x548C	GAMMA CTRL0C	0xCE	RW	Bit[7:0]: y_list_12 Output at 0x240 (10-bit scale) when register 0x5000[5] = 1

table 7-6 gamma control (sheet 2 of 4)

address	register name	default value	R/W	description
0x548D	GAMMA CTRL0D	0xDF	RW	Bit[7:0]: y_list_13 Output at 0x2C0 (10-bit scale) when register 0x5000[5] = 1
0x548E	GAMMA CTRL0E	0xEC	RW	Bit[7:0]: y_list_14 Output at 0x340 (10-bit scale) when register 0x5000[5] = 1
0x548F	GAMMA CTRL0F	0x0D	RW	Bit[7:0]: y_list_15 Slope in range of (0x341, 0x3FF) which should be 2 x (255 - register 0x548E) / 3
0x5490	GAMMA GAIN LIST00	0x07	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 00[11:8] UV output at 0x10 (10-bit scale)
0x5491	GAMMA GAIN LIST00	0x81	RW	Bit[7:0]: Gain list 00[7:0] UV output at 0x10 (10-bit scale)
0x5492	GAMMA GAIN LIST01	0x05	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 01[11:8] UV output at 0x20 (10-bit scale)
0x5493	GAMMA GAIN LIST01	0xF5	RW	Bit[7:0]: Gain list 01[7:0] UV output at 0x20 (10-bit scale)
0x5494	GAMMA GAIN LIST02	0x04	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 02[11:8] UV output at 0x40 (10-bit scale)
0x5495	GAMMA GAIN LIST02	0xC8	RW	Bit[7:0]: Gain list 02[7:0] UV output at 0x40 (10-bit scale)
0x5496	GAMMA GAIN LIST03	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 03[11:8] UV output at 0x80 (10-bit scale)
0x5497	GAMMA GAIN LIST03	0x96	RW	Bit[7:0]: Gain list 03[7:0] UV output at 0x80 (10-bit scale)
0x5498	GAMMA GAIN LIST04	0x03	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 04[11:8] UV output at 0xA0 (10-bit scale)
0x5499	GAMMA GAIN LIST04	0x3B	RW	Bit[7:0]: Gain list 04[7:0] UV output at 0xA0 (10-bit scale)
0x549A	GAMMA GAIN LIST05	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 05[11:8] UV output at 0xC0 (10-bit scale)
0x549B	GAMMA GAIN LIST05	0xF5	RW	Bit[7:0]: Gain list 05[7:0] UV output at 0xC0 (10-bit scale)

table 7-6 gamma control (sheet 3 of 4)

address	register name	default value	R/W	description
0x549C	GAMMA GAIN LIST06	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 06[11:8]] UV output at 0xE0 (10-bit scale)
0x549D	GAMMA GAIN LIST06	0xB9	RW	Bit[7:0]: Gain list 06[7:0] UV output at 0xE0 (10-bit scale)
0x549E	GAMMA GAIN LIST07	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 07[11:8]] UV output at 0x100 (10-bit scale)
0x549F	GAMMA GAIN LIST07	0x84	RW	Bit[7:0]: Gain list 07[7:0] UV output at 0x100 (10-bit scale)
0x54A0	GAMMA GAIN LIST08	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 08[11:8]] UV output at 0x120 (10-bit scale)
0x54A1	GAMMA GAIN LIST08	0x59	RW	Bit[7:0]: Gain list 08[7:0] UV output at 0x120 (10-bit scale)
0x54A2	GAMMA GAIN LIST09	0x02	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 09[11:8]] UV output at 0x140 (10-bit scale)
0x54A3	GAMMA GAIN LIST09	0x31	RW	Bit[7:0]: Gain list 09[7:0] UV output at 0x140 (10-bit scale)
0x54A4	GAMMA GAIN LIST10	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 10[11:8]] UV output at 0x180 (10-bit scale)
0x54A5	GAMMA GAIN LIST10	0xED	RW	Bit[7:0]: Gain list 10[7:0] UV output at 0x180 (10-bit scale)
0x54A6	GAMMA GAIN LIST11	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 11[11:8]] UV output at 0x1C0 (10-bit scale)
0x54A7	GAMMA GAIN LIST11	0xB3	RW	Bit[7:0]: Gain list 11[7:0] UV output at 0x1C0 (10-bit scale)
0x54A8	GAMMA GAIN LIST12	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 12[11:8]] UV output at 0x240 (10-bit scale)
0x54A9	GAMMA GAIN LIST12	0x59	RW	Bit[7:0]: Gain list 12[7:0] UV output at 0x240 (10-bit scale)
0x54AA	GAMMA GAIN LIST13	0x01	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 13[11:8]] UV output at 0x2C0 (10-bit scale)
0x54AB	GAMMA GAIN LIST13	0x11	RW	Bit[7:0]: Gain list 13[7:0] UV output at 0x2C0 (10-bit scale)

table 7-6 gamma control (sheet 4 of 4)

address	register name	default value	R/W	description
0x54AC	GAMMA GAIN LIST14	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 14[11:8]] UV output at 0x340 (10-bit scale)
0x54AD	GAMMA GAIN LIST14	0xD4	RW	Bit[7:0]: Gain list 14[7:0] UV output at 0x340 (10-bit scale)
0x54AE	GAMMA GAIN LIST15	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Gain list 15[11:8]] Slope in range of (0x341, 0x3FF) which should be 2 x (255 - {0x54AC[3:0], 0x54AD[7:0]}) / 3
0x54AF	GAMMA GAIN LIST15	0x1D	RW	Bit[7:0]: Gain list 15[7:0] Slope in range of (0x341, 0x3FF) which should be 2 x (255 - {0x54AC[3:0], 0x54AD[7:0]}) / 3
0x54B0	GAMMA CTRL30	0x01	RW	Bit[7:2]: Not used Bit[1]: Debug mode Changing this value is not allowed Bit[0]: Dark area color saturation reduction enable 0: Do not reduce color saturation in dark area 1: Reduce color saturation in area where luminance level is less than 0x54B1[7:0]
0x54B1	GAMMA CTRL31	0x20	RW	Bit[7:0]: Dark threshold for color saturation reduction
0x54B2	GAMMA CTRL32	0x01	RW	Bit[7:1]: Not used Bit[0]: Dark area noise reduction enable 0: Do not reduce noise in dark area 1: Reduce noise in area where luminance level is less than 0x54B3[7:0]
0x54B3	GAMMA CTRL33	0x40	RW	Bit[7:0]: Dark threshold for noise reduction
0x54B4	GAMMA CTRL34	0x00	RW	Bit[7:1]: Not used Bit[0]: Bright area color saturation reduction enable 0: Do not reduce color saturation in bright area 1: Reduce color saturation in area where luminance level is greater than 0x54B5[7:0]
0x54B5	GAMMA CTRL35	0xF0	RW	Bit[7:0]: Bright threshold for color saturation reduction
0x54B6	GAMMA CTRL36	0x01	RW	Bit[7:1]: Not used Bit[0]: Bright area noise reduction enable 0: Do not reduce noise in bright area 1: Reduce noise in area where luminance level is greater than 0x54B7[7:0]
0x54B7	GAMMA CTRL37	0xDF	RW	Bit[7:0]: Bright threshold for noise reduction

table 7-7 autocolor saturation

address	register name	default value	R/W	description
0x5500	UV UVADJUST CONTROL 0	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Auto color saturation offset UV ADJUST IN value minimum threshold
0x5501	UV UVADJUST CONTROL 3	0x1F	RW	Bit[7:6]: Not used Bit[5]: Color saturation manual adjustment enable 0: Automatically adjust color saturation according to sensor gain 1: Manual set color saturation by register 0x5501[4:0] Bit[4:0]: UV ADJUST IN manual setting Manual color saturation setting
0x5502	UV ADJ TH1	0x00	RW	Bit[7:1]: Not used Bit[0]: UV ADJ TH1[8] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, the UV ADJUST IN will be limited to 31.
0x5503	UV ADJ TH1	0x00	RW	Bit[7:0]: UV ADJ TH1[7:0] Real gain threshold 1 for UV ADJUST IN. When real gain is smaller than UV ADJ TH1, the UV ADJUST IN will be limited to 31.
0x5504	UV ADJ TH2	0x01	RW	Bit[7:1]: Reserved Bit[0]: UV ADJ TH2[8] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).
0x5505	UV ADJ TH2	0xFF	RW	Bit[7:0]: UV adj th2[7:0] Real gain threshold 2 for UV ADJUST IN. When real gain is larger than UV ADJ TH1, UV ADJUST IN will be limited to UV offset (0x5500[4:0]).

table 7-8 SDE control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580	SDE CONTROL0	0x00	RW	Bit[7]: Fixed Y enable - works with register 0x5587[7:0] 0: Fixed Y disable 1: Fixed Y enable Bit[6]: Negative Y enable 0: Negative Y disable 1: Negative Y enable Bit[5]: Gray image enable 0: Gray image disable 1: Gray image enable Bit[4]: Fixed V enable - works with register 0x5586[7:0] 0: Fixed V disable 1: Fixed V enable Bit[3]: Fixed U enable - works with register 0x5585[7:0] 0: Fixed U disable 1: Fixed U enable Bit[2]: Contrast enable - works with registers 0x5587[7:0], 0x5588[7:0], and 0x5589[7:0] 0: Contrast disable 1: Contrast enable Bit[1]: Saturation enable - works with registers 0x5583[7:0] and 0x5584[7:0] 0: Saturation disable 1: Saturation enable Bit[0]: Hue enable 0: Hue disable 1: Hue enable
0x5581	SDE CONTROL1	0x80	RW	Bit[7:0]: hue_cos When register 0x558A[6] = 0, this register is hue_cos. When register 0x558A[6] = 1, this register is angle[7:0].
0x5582	SDE CONTROL2	0x00	RW	Bit[7:0]: hue_sin When register 0x558A[6] = 0, this register is hue_sin. When register 0x558A[6] = 1, this register is angle[8]
0x5583	SDE CONTROL3	0x40	RW	Bit[7:0]: Saturation U
0x5584	SDE CONTROL4	0x40	RW	Bit[7:0]: Saturation V
0x5585	SDE CONTROL5	0x80	RW	Bit[7:0]: Ureg for fixed U
0x5586	SDE CONTROL6	0x80	RW	Bit[7:0]: Vreg for fixed V
0x5587	SDE CONTROL7	0x00	RW	Bit[7:0]: Yoffset for contrast or Y value for fixed Y

table 7-8 SDE control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5588	SDE CONTROL8	0x20	RW	Bit[7:0]: Ygain for contrast
0x5589	SDE CONTROL9	0x00	RW	Bit[7:0]: Ybright for contrast
0x558A	SDE CONTROL10	0x01	RW	Bit[7]: Yoffset manual mode enable 0: Auto mode for Yoffset in contrast 1: Manual mode for Yoffset in contrast Bit[6]: Hue angle enable Bit[5]: COS sign for Cr Bit[4]: COS sign for Cb Bit[3]: Offset sign for contrast Bit[2]: Bright sign for contrast Bit[1]: SIN sign for Cb Bit[0]: SIN sign for Cr

table 7-9 AVG control (sheet 1 of 2)

address	register name	default value	R/W	description
0x5680	AVG X START	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Avg x start[11:8] Horizontal start position for average window
0x5681	AVG X START	0x00	RW	Bit[7:0]: Avg x start[7:0] Horizontal start position for average window
0x5682	AVG X END	0x08	RW	Bit[7:4]: Not used Bit[3:0]: Avg x end[11:8] Horizontal end position for average window
0x5683	AVG X END	0x00	RW	Bit[7:0]: Avg x end[7:0] Horizontal end position for average window
0x5684	AVG Y START	0x00	RW	Bit[7:3]: Not used Bit[2:0]: Avg y start[10:8] Vertical start position for average window
0x5685	AVG Y START	0x00	RW	Bit[7:0]: Avg y start[7:0] Vertical start position for average window

table 7-9 AVG control (sheet 2 of 2)

address	register name	default value	R/W	description
0x5686	AVG Y END	0x06	RW	Bit[7:3]: Not used Bit[2:0]: Avg y end[10:8] Vertical end position for average window
0x5687	AVG Y END	0x00	RW	Bit[7:0]: Avg y end[7:0] Vertical end position for average window
0x5688	AVG R8	0xFF	RW	Bit[7:4]: Window1 weight Bit[3:0]: Window0 weight
0x5689	AVG R9	0xFF	RW	Bit[7:4]: Window3 weight Bit[3:0]: Window2 weight
0x568A	AVG RA	0xFF	RW	Bit[7:4]: Window5 weight Bit[3:0]: Window4 weight
0x568B	AVG RB	0xFF	RW	Bit[7:4]: Window7 weight Bit[3:0]: Window6 weight
0x568C	AVG RC	0xFF	RW	Bit[7:4]: Window9 weight Bit[3:0]: Window8 weight
0x568D	AVG RD	0xFF	RW	Bit[7:4]: Window11 weight Bit[3:0]: Window10 weight
0x568E	AVG RE	0xFF	RW	Bit[7:4]: Window13 weight Bit[3:0]: Window12 weight
0x568F	AVG RF	0xFF	RW	Bit[7:4]: Window15 weight Bit[3:0]: Window14 weight

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
operating temperature range[b]		-20°C to +70°C
stable image temperature range[c]		0°C to +50°C
supply voltage (with respect to ground)	V_{DD-A}	3.3V
	V_{DD-IO}	1.8V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range

table 8-2 DC characteristics

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current	TBD	TBD	TBD	mA
I_{DD-IO}		TBD	TBD	TBD	mA
$I_{DDS-SCCB}$	standby current	TBD	TBD	TBD	mA
$I_{DDS-PWDN}$		TBD	TBD	TBD	µA
digital inputs (typical conditions: AVDD = 3.3V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW	TBD	TBD	0.54	V
V_{IH}	input voltage HIGH	1.26	TBD	TBD	V
C_{IN}	input capacitor	TBD	TBD	10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62	TBD	TBD	V
V_{OL}	output voltage LOW	TBD	TBD	0.18	V
serial interface inputs					
V_{IL}[a]	SCL and SDA	-0.5	0.0	0.54	V
V_{IH}[a]	SCL and SDA	1.26	1.8	2.3	V

a. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		TBD		MHz
DLE	DC differential linearity error		<0.5		LSB
ILE	DC integral linearity error		<0.5		LSB
	settling time for software reset			<1	ms
	settling time for resolution mode change			<1	ms
	settling time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XI)	6	12.27	29.5	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

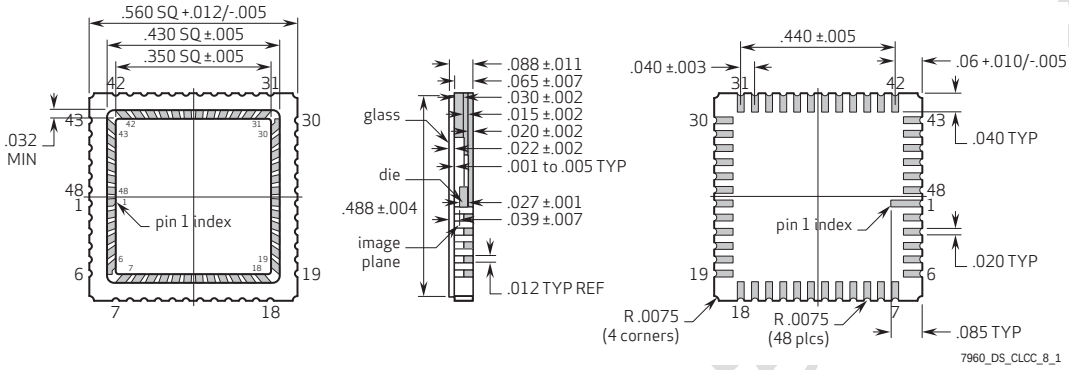


table 9-1 package dimensions

dimensions	millimeters	inches
package size	14.22 + 0.30 / -0.13 sq	.560 + .012 / - .005 sq
package height	2.23 ± 0.28	.088 ± .011
substrate base height	0.51 ± 0.05	.020 ± .002
cavity size	8.89 ± 0.13 sq	.350 ± .005 sq
castellation height	1.14 ± 0.13	.045 ± .005
pin #1 pad size	0.51 x 2.16	.020 x .085
pad size	0.51 x 1.02	.020 x .040
pad pitch	1.02 ± 0.08	.040 ± .003
package edge to first lead center	1.524 + 0.25 / -0.13	.06 + .010 / - .005
end-to-end pad center-center	11.18 ± 0.13	.440 ± .005
glass size	12.40 ± 0.10 sq / 13.00 ± 0.10 sq	.488 ± .004 sq / .512 ± .004 sq
glass height	0.55 ± 0.05	.022 ± .002
die thickness	0.733 ± 0.015	.029 ± .001
top of glass to image plane	0.95 ± 0.18	.037 ± .007
substrate height	1.65 ± 0.18	.065 ± .007

9.2 IR reflow specifications

note
The OV7960/OV7461 uses a lead free package.

figure 9-2 IR reflow ramp rate requirements

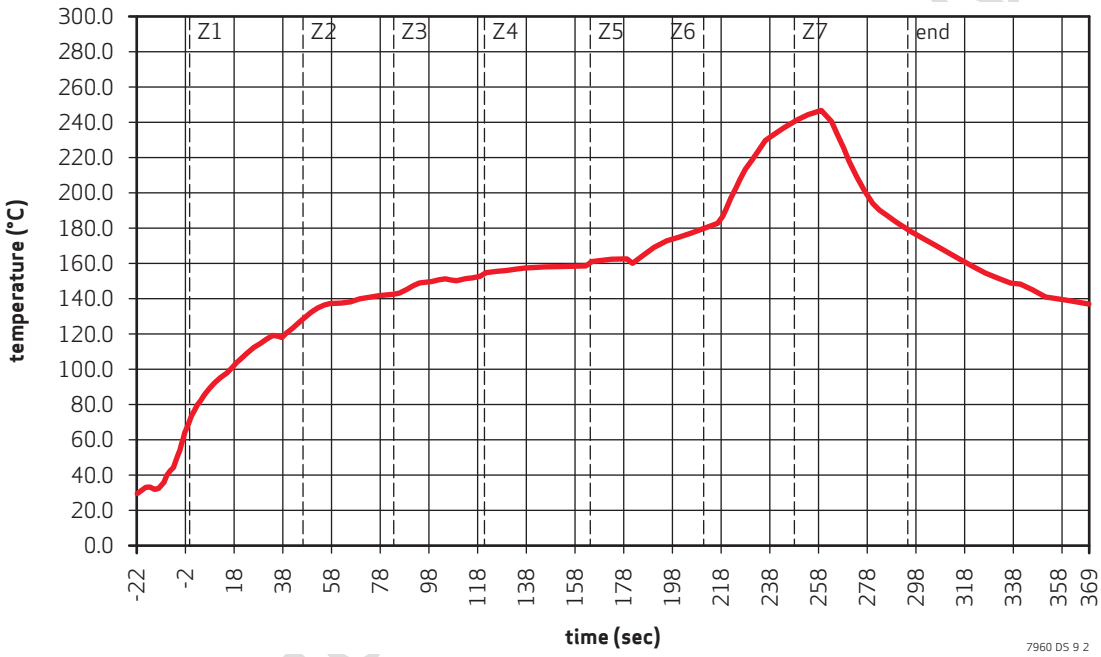


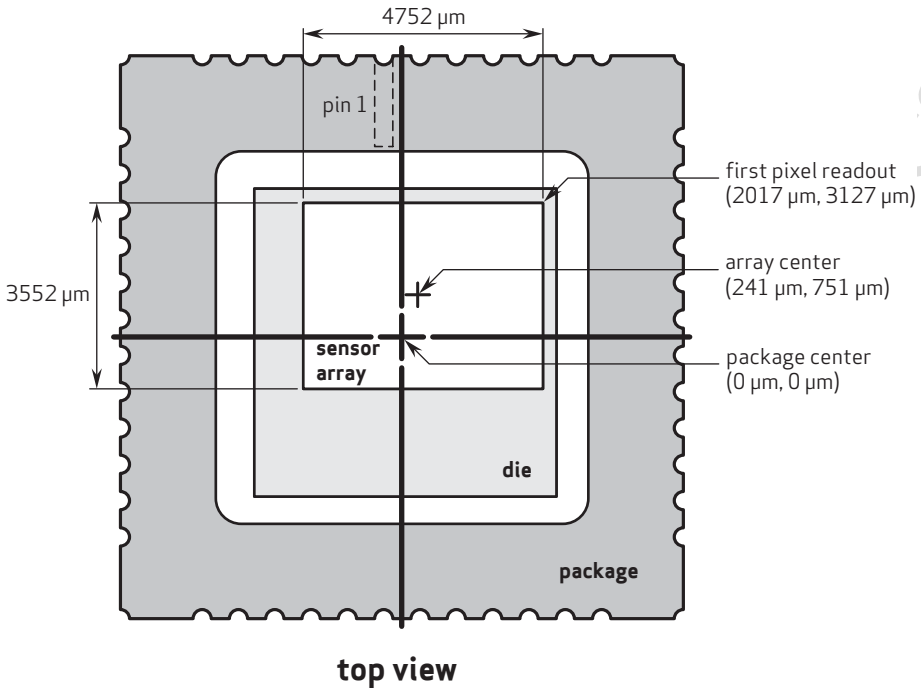
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pin 1 (AGND) oriented down as shown.

7960CLCC_DS_9_1

revision history

version 1.0 11.13.2008

- initial release

version 1.1 12.05.2008

- in section 4.2, changed first sentence to "... with the register 0x5004[1:0]."
- in table 4-5, changed bit description for registers, 0x5680, 0x5681, 0x5682, 0x5683, 0x5684, 0x5685, 0x5686, 0x5687
- in table 4-5, changed register name for registers 0x5688, 0x5689, 0x568A, 0x568B, 0x568C, 0x568D, 0x568E, 0x568F
- in table 5-1, changed default value and bit description for registers 0x5002, 0x5003, 0x5004, and 0x5024
- in table 5-1, changed bit description for register 0x5004
- in table 5-1, changed bit description for register 0x5003
- in table 5-2, changed default value and bit description for register 0x5004
- in table 5-4, changed bit description for registers 0x5000, 0x5080
- in table 5-4, changed register name and bit description for registers 0x5081, 0x5082, 0x5083, 0x5084, 0x5085, 0x5086,0x5087, 0x5088, 0x5089, 0x508A, 0x508B
- in table 5-4, changed bit description for registers 0x508C, 0x508D
- in table 5-5, changed bit description for registers 0x5000, 0x5005, 0x5100, 0x5101, 0x5102, 0x5103, 0x5104, 0x5105, 0x5106, 0x5107, 0x5108, 0x5109, 0x510A,0x510B, 0x510C, 0x510D, 0x510E, 0x510F, 0x5110, 0x5111, 0x5112, 0x5113, 0x5114, 0x5115, 0x5116, 0x5117, 0x5118, 0x5119, 0x511A, 0x511B
- in table 5-5, changed register name and bit description for register 0x511C
- in table 5-5, changed register name for register 0x511D
- in table 5-6, changed bit description for registers 0x5000, 0x5005
- in table 5-6, changed register name, default value r/w and bit description for register 0x5005
- in table 5-6, changed register name and bit description for registers 0x5480, 0x5481, 0x5482, 0x5483, 0x5484, 0x5485, 0x5486, 0x5487, 0x5488, 0x5489, 0x548A, 0x548B, 0x548C, 0x548D, 0x548E, 0x548F
- in table 5-7, changed bit description for registers 0x5001, 0x5005
- in table 5-8, changed bit description for register 0x5000
- in table 5-9, changed bit description for registers 0x5000, 0x5293, 0x5295, 0x5296, 0x5297, 0x5298, 0x5299, 0x529A, 0x529B, 0x529C, 0x529D, 0x529E, 0x529F, 0x52A0, 0x52A2, 0x52A3, 0x52A4, 0x52A5, 0x52A6, 0x52A7, 0x52A8, 0x52A9, 0x52AA, 0x52AB, 0x52AC, 0x52AD, 0x52AE, 0x52AF,0x52B0
- in table 5-9, changed register name and bit description for registers 0x5290, 0x5291, 0x5292, 0x5294
- in table 5-9, changed default value and bit description for registers 0x52A1, 0x52B1
- in table 5-10, changed bit description for register 0x5000

- in table 5-11, changed bit description for register 0x5001
- in table 5-12, changed bit description for register 0x5001
- in table 5-12, changed bit description for registers, 0x5400, 0x5401, 0x5402, 0x5403, 0x5404, 0x5405, 0x5406, 0x5407
- in table 5-12, changed default value and bit description 0x5403
- in table 5-13, changed bit description for register 0x5000
- in table 5-13, changed register name and bit description for registers 0x5480, 0x5481, 0x5482, 0x5483, 0x5484, 0x5485, 0x5486, 0x5487, 0x5488, 0x5489, 0x548A, 0x548B, 0x548C, 0x548D, 0x548E, 0x548F
- in table 5-14, changed bit description for registers 0x5001 and 0x5005
- changed bit description for register 0x5001 in table 5-15 and table 5-16
- in table 5-15, changed register name and bit description for registers 0x5500, 0x5501
- in table 5-15, changed bit description for registers, 0x5502, 0x5503, 0x5504, 0x5505
- in table 5-16, changed register name and bit description for registers 0x5580, 0x5581, 0x5582, 0x5583, 0x5584, 0x5585, 0x5586, 0x5587, 0x5588, 0x5588, 0x558A
- in table 5-20, changed bit description for registers, 0x5680, 0x5681, 0x5682, 0x5683, 0x5684, 0x5685, 0x5686, 0x5687
- in table 5-20, changed register name for registers 0x5688, 0x5689, 0x568A, 0x568B, 0x568C, 0x568D, 0x568E, 0x568F
- added new register tables to chapter 7

version 1.11 **04.15.2009**

- in key specifications on page iii, changed operating temperature range to -20°C to +70°C
- in table 8-1, changed operating temperature range (first row) to -20°C to +70°C

the clear advantage™

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